MAX4016ExA Rev. B

RELIABILITY REPORT

FOR

# MAX4016ExA

PLASTIC ENCAPSULATED DEVICES

July 26, 2001

# **MAXIM INTEGRATED PRODUCTS**

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## Conclusion

The MAX4016 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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## I. Device Description

#### A. General

The MAX4016 dual op amp is a unity-gain-stable device that combines high-speed performance with Rail-to-Rail® output. This device operates from a +3.3V to +10V single supply or from  $\pm 1.65V$  to  $\pm 5V$  dual supplies. The common-mode input voltage range extends beyond the negative power-supply rail (ground in single-supply applications).

The MAX4016 requires only 5.5mA of quiescent supply current while achieving a 200MHz -3dB bandwidth and a  $600 \text{ V/}\mu\text{s}$  slew rate. This part is an excellent solution in low-power/low-voltage systems that require wide bandwidth, such as video, communications, and instrumentation. In addition, when disabled, their high output impedance makes them ideal for multiplexing applications.

#### B. Absolute Maximum Ratings

Item	Rating
Supply Voltage ( $V_{CC}$ to $V_{EE}$ )	+12V
IN, IN_+, OUT_, EN_	$(V_{EE} - 0.3V)$ to $V_{CC} + 0.3V)$
Output Short-Circuit Duration to $V_{CC}$ or $V_{EE}$	Continuous
Operating Temperature Range	-40°C to +85°C
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
8 Lead SO	471mW
8 Lead uMax	330mW
Derates above +70°C	
8 Lead SO	5.9mW/°C
8 Lead uMax	4.1mW/°C

#### **II. Manufacturing Information**

- A. Description/Function: Low-Cost, High Speed, Single-Supply Op Amp with Rail-to-Rail Output
- B. Process: CB2 (Complementary Bipolar Process)
- C. Number of Device Transistors: 190
- D. Fabrication Location: Oregon, USA
- E. Assembly Location: Philippines, Malaysia, or Thailand
- F. Date of Initial Production: October, 1997

## **III.** Packaging Information

A. Package Type:	8 Lead SO	8 Lead uMax
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-3001-0036	Buildsheet # 05-3001-0037
H. Flammability Rating:	Class UL94-V0	Class UL94-V0

#### **IV. Die Information**

- A. Dimensions: 81 x 51 mils
- B. Passivation:  $Si_3N_4/SiO_2$  (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 2 microns (as drawn)
- F. Minimum Metal Spacing: 2 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric: SiO<sub>2</sub>
- I. Die Separation Method: Wafer Saw

#### V. Quality Assurance Information

A. Quality Assurance Contacts:	Jim Pedicord	(Reliability Lab Manager)
	Bryan Preeshl	(Executive Director)
	Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

#### **VI.** Reliability Evaluation

## A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

 $\lambda = \frac{1}{\text{MTTF}} = \frac{1.83 \quad (\text{Chi} \text{ square value for MTTF upper limit})}{192 \text{ x } 4389 \text{ x } 240 \text{ x } 2}$ Temperature Acceleration factor assuming an activation energy of 0.8eV

 $\lambda = 4.52 \text{ x } 10^{-9}$ 

 $\lambda = 4.52$  F.I.T. (60% confidence level @ 25°C)

This bw failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. The attached Burn-In Schematic shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1L**).

## B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

## C. E.S.D. and Latch-Up Testing

The OP06 die type has been found to have all pins able to withstand a transient pulse of  $\pm$  2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm$ 250mA and/or  $\pm$ 20V.

# Table 1Reliability Evaluation Test ResultsMAX4016ExA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (N	Note 1)			
	$Ta = 135^{\circ}C$ Biased Time = 192 hrs.	DC Parameters & functionality	240	0
Moisture Testing	(Note 2)			
Pressure Pot	$Ta = 121^{\circ}C$ P = 15 psi. RH= 100% Time = 96 hrs.	DC Parameters & functionality	940 80	1 0
85/85	$Ta = 85^{\circ}C$ RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stres	s (Note 2)			
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Small Outline package.

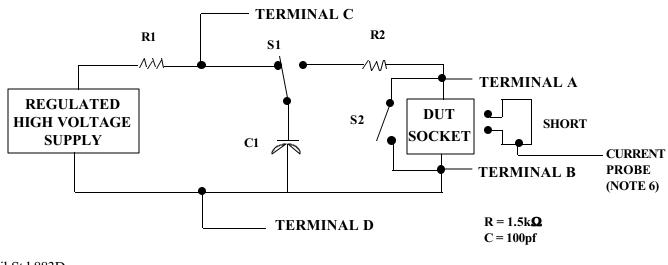
Note 2: Generic process/package data

# Attachment #1

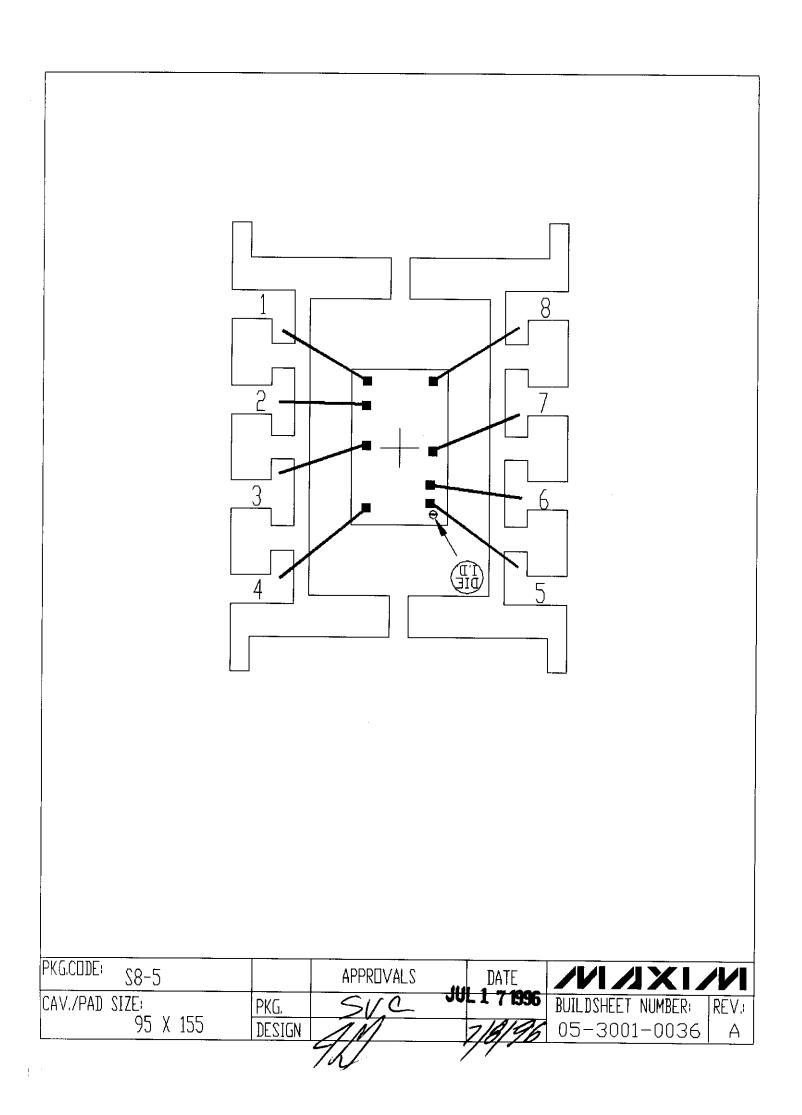
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

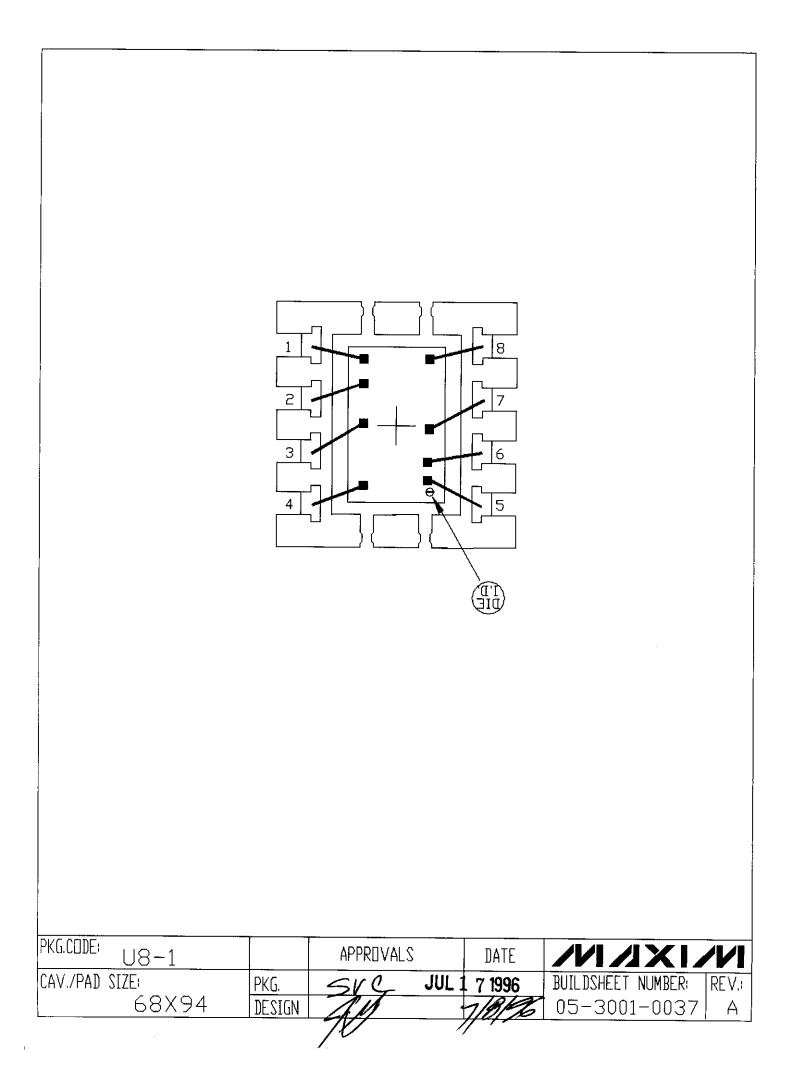
# TABLE II. <u>Pin combination to be tested.</u> 1/2/

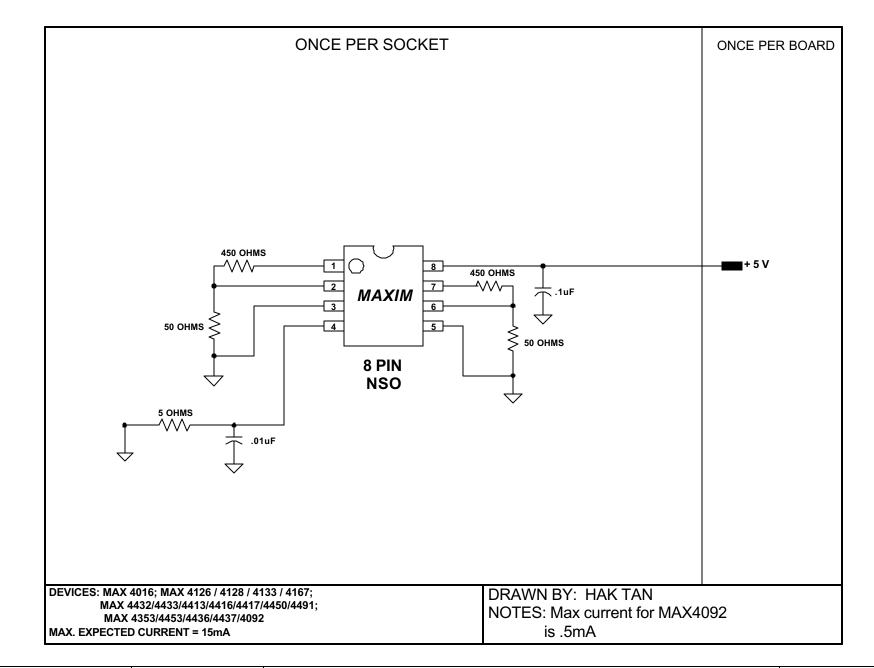
- <u>1/</u> Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- $\overline{3/}$  Repeat pin combination I for each named Power supply and for ground (e.g., where V<sub>PS1</sub> is V<sub>DD</sub>, V<sub>CC</sub>, V<sub>SS</sub>, V<sub>BB</sub>, GND, +V<sub>S</sub>, -V<sub>S</sub>, V<sub>REF</sub>, etc).
- 3.4 <u>Pin combinations to be tested.</u>
  - a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
  - b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
  - c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D Method 3015.7 Notice 8







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		6/4437/4092)	