19-2086; Rev 0; 7/01

+3.3V, 10.3Gbps Limiting Amplifier

General Description

The MAX3971 is a compact, low-power, 10.3Gbps limiting amplifier. It accepts signals over a wide range of input voltage levels and provides constant-level output voltages with controlled edge speeds. It functions as a data quantizer. The output of the amplifier is a 250mVp-p differential CML signal with a 100Ω differential termination.

The MAX3971 is designed to work with the MAX3970, a 10.3Gbps transimpedance amplifier (TIA). The limiting amplifier operates on a single +3.3V supply and consumes only 155mW. The part functions over a 0°C to +85°C temperature range. It also has a disable function that allows the outputs to be squelched if required by the application.

The MAX3971 is offered in either die form or in a compact 4mm x 4mm, 20-pin QFN plastic package.

Features

- **Single +3.3V Power Supply**
- **155mW Power Consumption**
- **9.5mVp-p Input Sensitivity**
- **800mVp-p Input Overload**
- **3.4psp-p Deterministic Jitter**
- **Dice and 4mm x 4mm QFN Package Availability**
- **Output Disable Feature**

Applications

10Gigabit Ethernet Optical Receivers

VSR OC-192 Receivers

10Gigabit Fibre Channel Receivers

Ordering Information

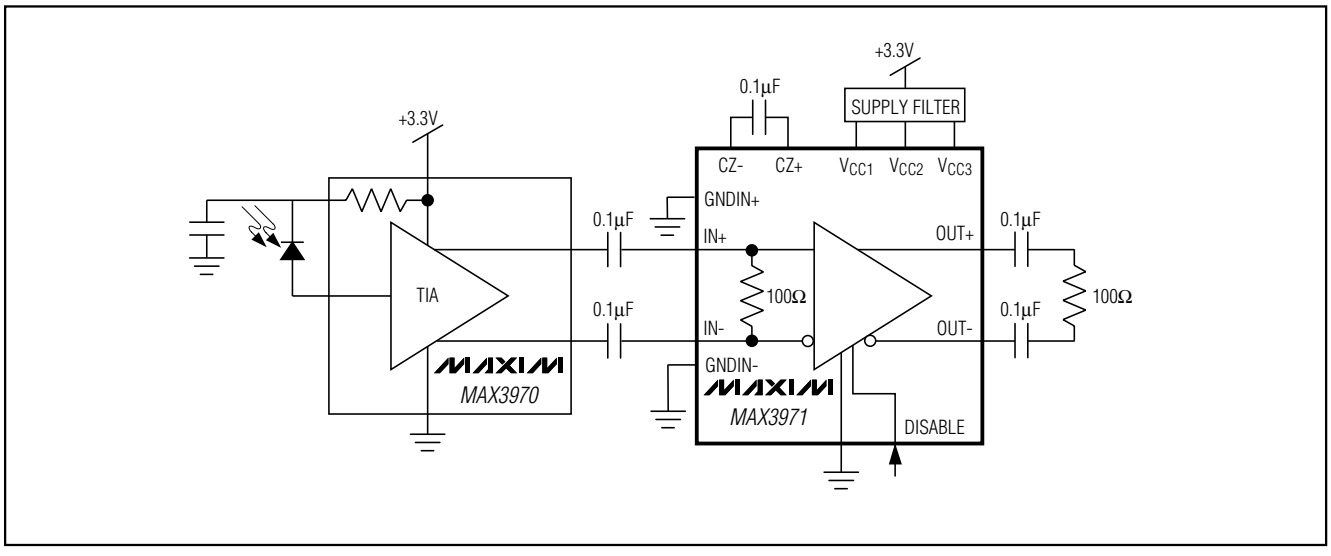
PART	TEMP. RANGE	PIN-PACKAGE
MAX3971UGP	0°C to +85°C	20 QFN*
MAX3971U/D	0°C to +85°C	Dice**

**Exposed pad*

***Dice are designed to operate over a 0°C to +110°C junction temperature (T_J) range, but are tested and guaranteed at T_A = +25°C.*

Pin Configuration appears at end of data sheet.

Typical Application Circuit



+3.3V, 10.3Gbps Limiting Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC1}, V_{CC2}, V_{CC3} .....-0.5V to +5.0 V
Voltage at IN+, IN-, DISABLE,
CZ+, CZ-, OUT+, OUT-.....+0.5V to (V_{CC} + 0.5V)
Differential Voltage Between CZ+ and CZ- .....±1V
Differential Voltage Between IN+ and IN-.....±2.5V
Continuous Power Dissipation (T_A = +85°C)
20-Pin QFN (derate 20mW/°C above +85°C) 1.3W
Operating Ambient Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +150°C
Die Attach Temperature.....+400°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V, output load = 50Ω to V_{CC}, T_A = +25°C, unless otherwise noted. Data mark density is 50%.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}			47	85	mA
Small-Signal Bandwidth	BW			10		GHz
Low-Frequency Cutoff		CZ = 0.1µF		40	160	kHz
Data Rate				10		Gbps
Deterministic Jitter		10mVp-p input, K28.5 pattern at 10.3Gbps (Note 1)		8		psp-p
		20mVp-p input, K28.5 pattern at 10.3Gbps (Note 1)		4.7	14	
		800mVp-p input, K28.5 pattern at 10.3Gbps (Note 1)		3.4	7	
Random Jitter		20mVp-p to 800mVp-p (Note 2)		0.7	1.0	ps_{RMS}
Transition Time, Output	t_r, t_f	20% to 80%, OUT+, OUT-		20	30	ps
Input Sensitivity	V_{IN-min}	BER = 1E-12, 2^{23} - 1PRBS, 10.3Gbps			9.5	mVp-p
Input Overload	V_{IN-max}		800			mVp-p
Data Input Resistance	R_{IN}	Single-ended	42	52	58	Ω
Differential Data Output-Voltage Swing	V_{OD1}	DISABLE high		1	50	mVp-p
	V_{OD2}	DISABLE low	190	250	400	
Data Output Common-Mode Voltage	V_{CM}			V_{CC} - 0.75		V
Output Resistance	R_{OUT}	Single-ended	42	52	58	Ω
Data Output Offset when DISABLE is High				75		mVp-p
DISABLE Input Current		High = V_{CC}, low = GND		0.05	1	mA
DISABLE INPUT High Voltage			2.8			V
DISABLE INPUT Low Voltage					1.4	V

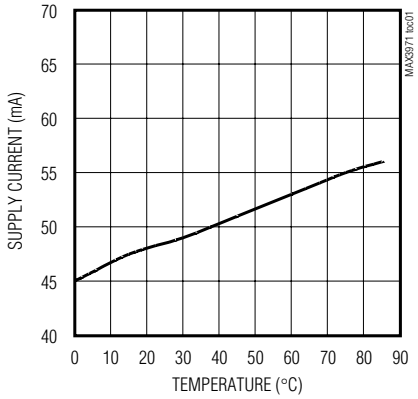
Note 1: Deterministic jitter is measured with a K28.5 pattern (0011 1110 1011 0000 0101). It is the peak-to-peak deviation from the ideal time crossings, measured at the zero-level crossings of the differential output.

Note 2: Random jitter is measured with the minimum input signal applied. To achieve a bit error rate of 10^{-12}, the peak-to-peak random jitter is 14.1 times the RMS random jitter.

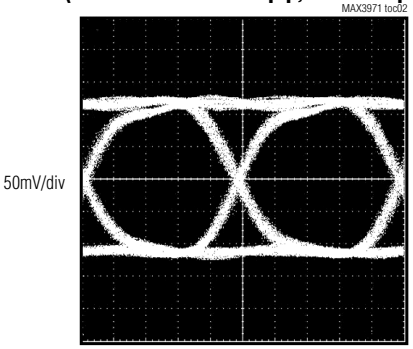
Typical Operating Characteristics

(V_{CC} = +3.3V, output load = 50Ω to V_{CC}, T_A = +25°C, unless otherwise noted.)

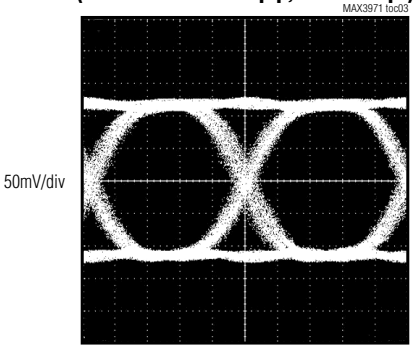
SUPPLY CURRENT vs. TEMPERATURE



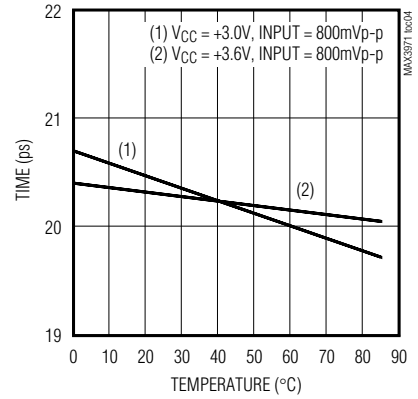
OUTPUT EYE DIAGRAM (INPUT SIGNAL = 800mVp-p, AT 10.3Gbps)



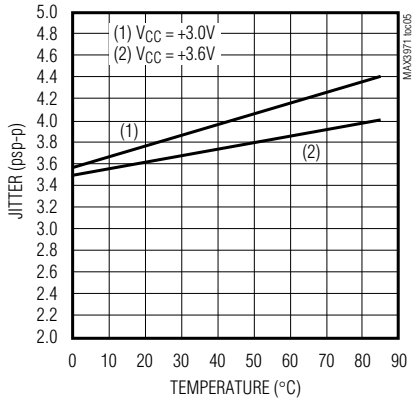
OUTPUT EYE DIAGRAM (INPUT SIGNAL = 9mVp-p, AT 10.3Gbps)



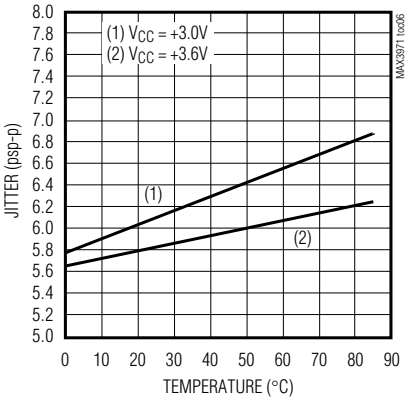
TRANSITION TIME vs. TEMPERATURE (20%–80%)



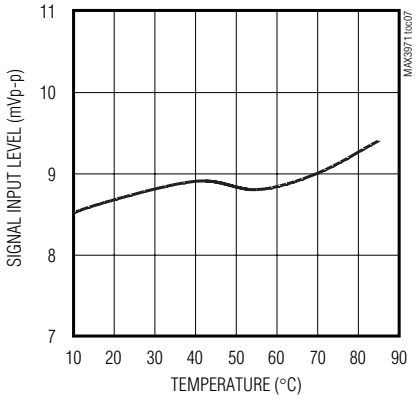
DETERMINISTIC JITTER vs. TEMPERATURE (800mVp-p INPUT K28.5 PATTERN AT 10.3Gbps)



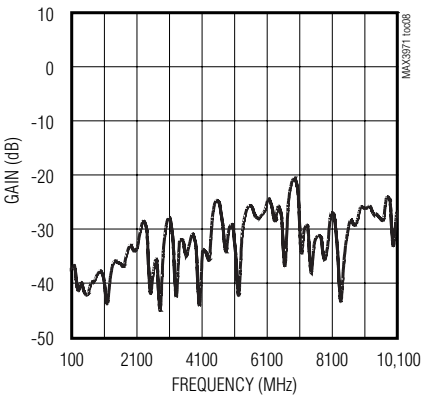
DETERMINISTIC JITTER vs. TEMPERATURE (10mVp-p INPUT K28.5 PATTERN AT 10.3Gbps)



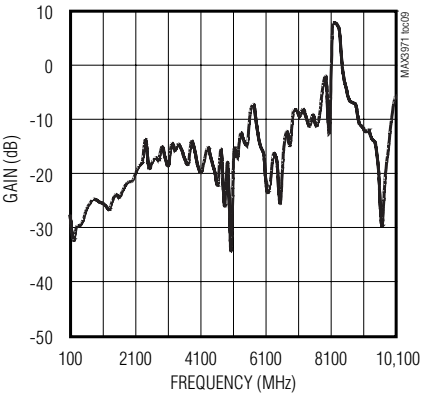
INPUT SENSITIVITY vs. TEMPERATURE (FOR BIT ERROR RATIO OF 1E-12)



INPUT RETURN (S11) INPUT SIGNAL = -20dBm



OUTPUT RETURN (S22) INPUT SIGNAL = -20dBm

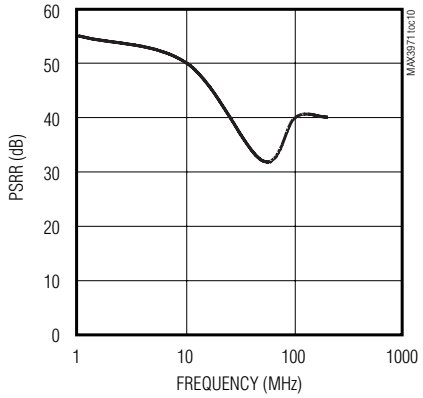


+3.3V, 10.3Gbps Limiting Amplifier

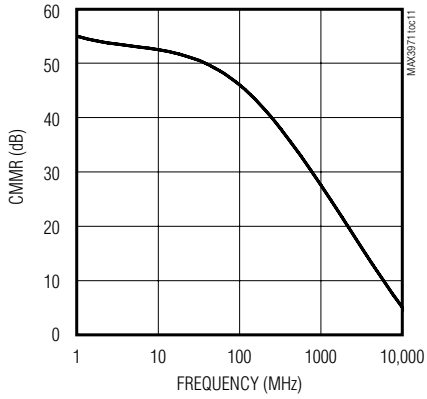
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, output load = 50Ω to V_{CC}, T_A = +25°C, unless otherwise noted.)

POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



COMMON-MODE REJECTION RATIO vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	GNDIN+	Input Ground for Shielding Input Signal IN+. Not connected internally.
2	IN+	Noninverting Input Signal
3	IN-	Inverting Input Signal
4	GNDIN-	Input Ground for Shielding Input Signal IN-. Not connected internally.
5, 7, 9, 10	N.C.	No Connection. Leave unconnected.
6, 8, 11	GND	Ground
12, 15	V_{CC3}	Output Circuitry Power Supply
13	OUT-	Inverting Output of Amplifier
14	OUT+	Noninverting Output of Amplifier
16	DISABLE	When High, the Outputs are Disabled
17	V_{CC2}	Power Supply to Circuitry Other than Input and Output Circuits
18	CZ+	Filter Capacitor for Offset Correction. Attach other side of a capacitor to pin 19. See *Detailed Description*.
19	CZ-	See pin 18.
20	V_{CC1}	Input Circuitry Power Supply
CP	CORNER PIN	Ground. The corner pins are connected to the exposed pad through the lead frame. If the corner pins are not soldered to the same node as the exposed pad, ensure that the solder mask is located below them so that unintentional connections do not occur.
EP	EXPOSED PAD	Exposed Pad. Must be soldered to supply ground for proper electrical and thermal operation.

Detailed Description and Applications Information

Figure 1 is a functional diagram of the MAX3971 limiting amplifier.The signal path consists of an input buffer followed by a gain stage and output amplifier. A feedback loop provides offset correction by driving the average value of the differential output to zero.

Gain Stage and Offset Correction

The limiting amplifier provides approximately 50dB gain. This large gain makes the amplifier susceptible to small DC offsets, which cause deterministic jitter. A low-frequency loop is integrated into the limiting amplifier to reduce output offset, typically to less than 2mV.

The external capacitor CZ is required to set the low-frequency cutoff for the offset correction loop and for stability. The time constant of the loop is set by the product of an equivalent 20kΩ on-chip resistor and the value of the off-chip capacitor, CZ. For stable operation, the minimum value of CZ is 0.01µF. To minimize pattern-dependent jitter, CZ should be as large as possible. For 10Gigabit Ethernet applications, the typical value of CZ is 0.1µF. Keep CZ as close to the package as possible.

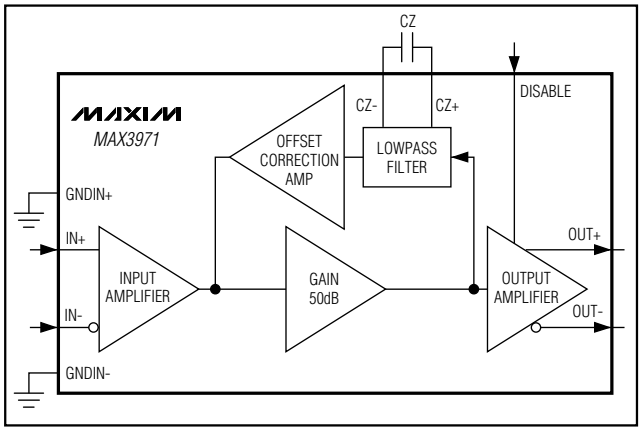


Figure 1. Functional Diagram

CML Input Circuit

The input buffer is designed to accept CML input signals such as the output from the MAX3970 transimpedance amplifier. An equivalent circuit for the input is shown in Figure 2. DC-coupling the inputs is not recommended since this will prevent the part's offset correction circuitry from working properly. Thus, AC-coupling capacitors are required on the input.

CML Output Circuit

An equivalent circuit for the output network is shown in Figure 3. It consists of a pair of 50Ω resistors connected to V_{CC} driven by the collectors of an output differential transistor pair (Q1 and Q2). The differential output signals are clamped by transistors Q3 and Q4 when the DISABLE input is high.

Disable Function

A logic signal can be applied to the DISABLE pin to squelch the output signal. When the output is disabled, an offset is added to the output, preventing the following stage from oscillating (if DC-coupled).

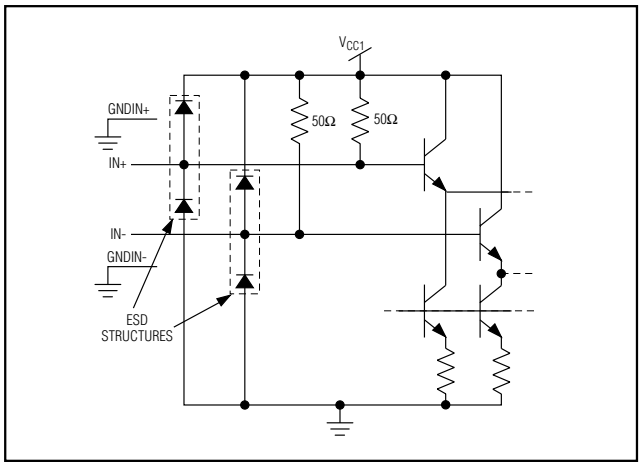


Figure 2. CML Input Equivalent Circuit

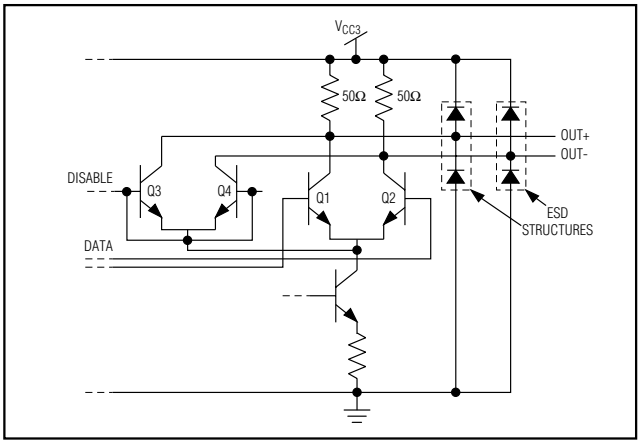


Figure 3. CML Input Equivalent Circuit Showing Clamping Circuit for Squelching the Output Signal

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Layout Considerations

Circuit board layout and design can significantly affect the MAX3971's performance. Use good high-frequency techniques, including fixed-impedance transmission lines for the high-frequency data signal. Use a multilayer board with solid ground plane. Minimize the inductance between MAX3971 and the ground plane.

The MAX3971 uses three power supply pins, V_{CC1}, V_{CC2}, and V_{CC3}. The input circuitry of the MAX3971 is supplied by V_{CC1}. The output drivers have a separate supply V_{CC3}, which usually has large pulsing currents. All other circuitry is powered by V_{CC2}. It is possible to simply connect the three pins together. However, better isolation of the input circuitry is ensured by using a supply filter. For optimal isolation, Figure 4 shows a possible supply filtering circuit. Element L, a ferrite bead, provides isolation between a noisy V_{CC3} and the sensitive V_{CC1}.

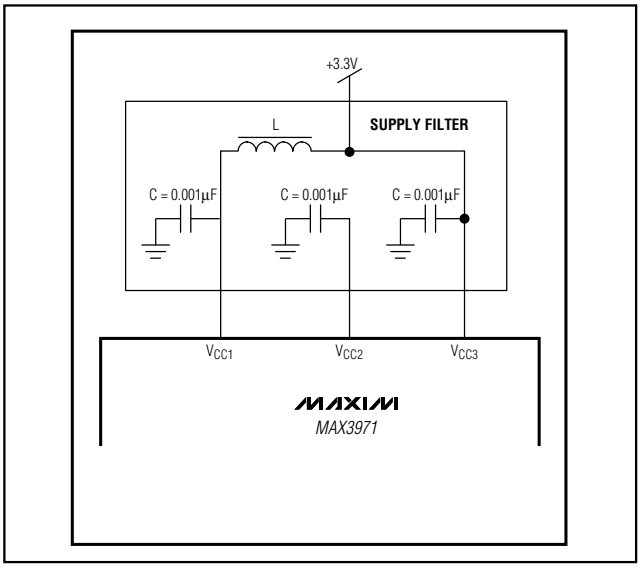
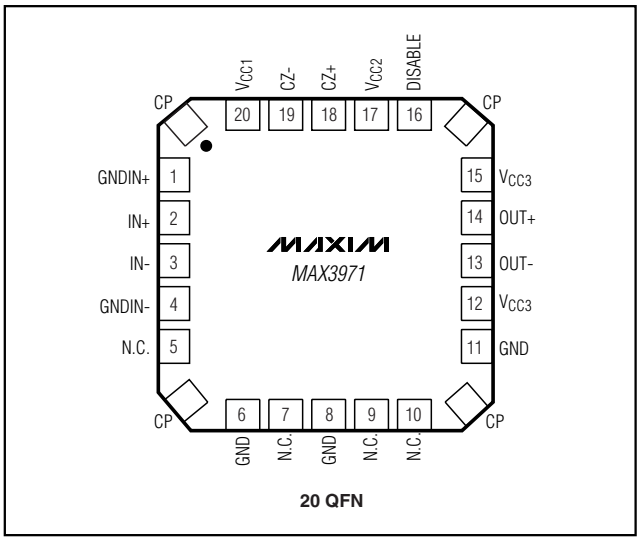


Figure 4. Power-Supply Filter

Pin Configuration



20 QFN

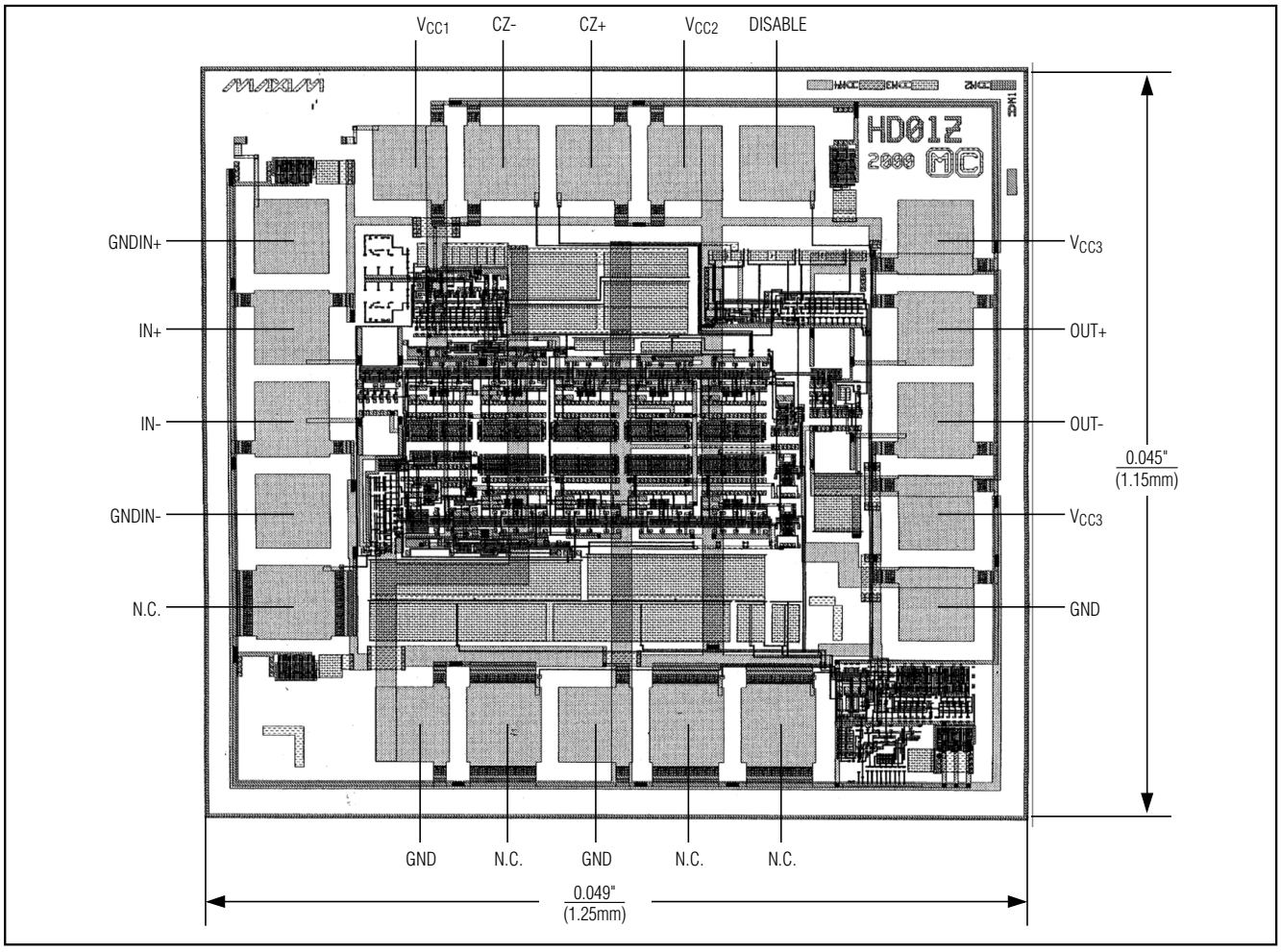
Chip Information

TRANSISTOR COUNT: 1803

PROCCESS: SiGe Bipolar

SUBSTRATE: Electrically Isolated

Chip Topography



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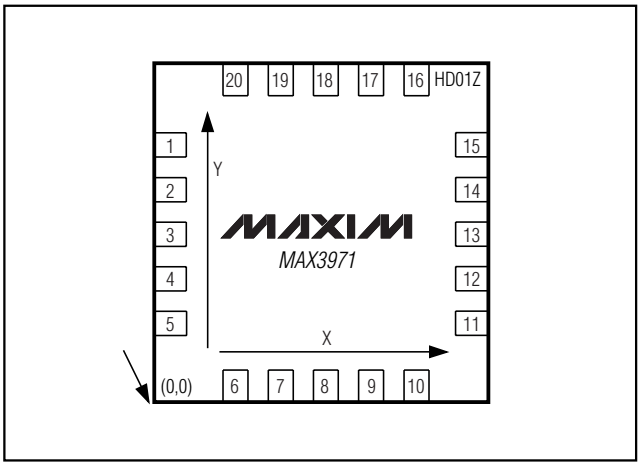
Chip Topography (continued)

MAX3971		
PIN NUMBER	**X DIMENSION (MICRONS)**	**Y DIMENSION (MICRONS)**
1	0	672
2	0	546
3	0	420
4	0	294
5	0	168
6	163.8	0
7	289.8	0
8	415.8	0
9	541.8	0
10	667.8	0
11	884.8	168
12	884.8	294
13	884.8	420
14	884.8	546
15	884.8	672
16	667.8	772.8
17	541.8	772.8
18	415.8	772.8
19	289.8	772.8
20	163.8	772.8

- All dimensions are in microns.
- Pad dimensions:

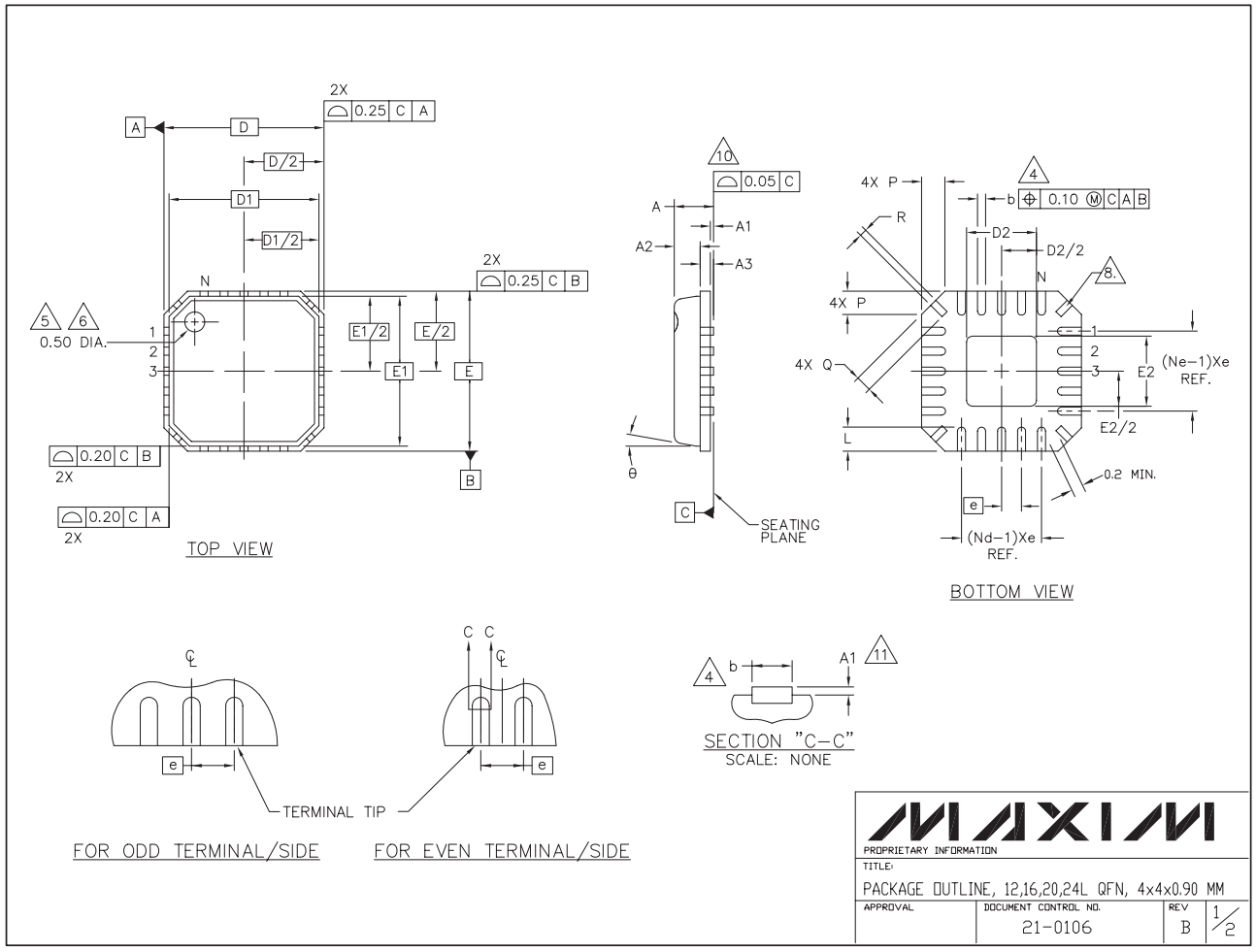
  PASSIVATION OPENING: 94.4microns × 94.4microns

  METAL: 102.4microns × 102.4microns
- All measurements specify the lower left corner of the pad



Package Information

12, 16,20, 24L QFN.EPS



+3.3V, 10.3Gbps Limiting Amplifier

Package Information (continued)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM MUST TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.
12. MEETS JEDEC MO220.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.85	1.00	
A1	0.00	0.01	0.05	11
A2	–	0.65	0.80	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ			12°	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	

SYMBOL	PITCH VARIATION A			NOTE	PITCH VARIATION B			NOTE	PITCH VARIATION C			NOTE	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.		MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
e	0.80 BSC				0.65 BSC				0.50 BSC				0.50 BSC			
N	12			3	16			3	20			3	24			3
Nd	3			3	4			3	5			3	6			3
Ne	3			3	4			3	5			3	6			3
L	0.50	0.60	0.75		0.50	0.60	0.75		0.50	0.60	0.75		0.30	0.40	0.55	
b	0.28	0.33	0.40	4	0.23	0.28	0.35	4	0.18	0.23	0.30	4	0.18	0.23	0.30	4
Q	0.30	0.40	0.65		0.30	0.40	0.65		0.30	0.40	0.65		0.00	0.20	0.45	
D2	SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: A			
E2	SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: A			

SYMBOLS		D2			E2			NOTE
		MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD VARIATIONS	A	1.95	2.10	2.25	1.95	2.10	2.25	
	B	1.55	1.70	1.85	1.55	1.70	1.85	

EXAMPLE: WE CAN CALL VARIATION "BB" FOR 16 TERMINAL QFN WITH 1.70x1.70 mm NOMINAL EXPOSED PAD DIMENSION. THE FORMER ONE IN VARIATION IS FOR PITCH VARIATION AND THE LATTER ONE IS FOR EXPOSED PAD VARIATION.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 12,16,20,24L QFN, 4x4x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0106	B	2/2