198-2710; Rev 0; 2/03

EVALUATION KIT AVAILABLE

MAXIM

2.488Gbps/2.667Gbps Clock and Data Recovery with Limiting Amplifier

MAX3874

General Description

The MAX3874 is a compact, dual-rate clock and data recovery with limiting amplifier for OC-48 and OC-48 with FEC SONET/SDH applications. Without using an external reference clock, the fully integrated phase-locked loop (PLL) recovers a synchronous clock signal from the serial NRZ data input. The input data is then retimed by this recovered clock, providing a clean data output. An additional serial input (SLBI±) is available for system-loopback diagnostic testing. Alternatively, this input can be connected to a reference clock to maintain a valid clock output in the absence of data transitions. The device also includes a loss-of-lock ($\overline{LOL}$) output.

The MAX3874 contains a vertical threshold control to compensate for optical noise due to EDFAs in DWDM transmission systems. The recovered data and clock outputs are CML with on-chip 50Ω back termination on each line. Its jitter performance exceeds all SONET/SDH specifications. The MAX3874A is the MAX3874 with a voltage-controlled oscillator (VCO) centered at 2.0212GHz.

The MAX3874 operates from a single +3.3V supply and typically consumes 580mW. It is available in a 5mm × 5mm 32-pin QFN with exposed pad package and operates over the -40°C to +85°C temperature range.

Applications

- SONET/SDH Receivers and Regenerators
- Add/Drop Multiplexers
- Digital Cross-Connects
- SONET/SDH Test Equipment
- DWDM Transmission Systems
- Access Networks

Features

- ♦ **2.488Gbps and 2.667Gbps Input Data Rates**
- ♦ **Reference Clock Not Required for Data Acquisition**
- ♦ **Exceeds ANSI, ITU, and Bellcore SONET/SDH Jitter Specifications**
- ♦ **2.7mUI$_{RMS}$ Clock Jitter Generation**
- ♦ **10mV$_{P-P}$ Input Sensitivity Without Threshold Adjust**
- ♦ **0.65UI$_{P-P}$ High-Frequency Jitter Tolerance**
- ♦ **±170mV Wide Input Threshold Adjust Range**
- ♦ **Clock Holdover Capability Using Frequency-Selectable Reference Clock**
- ♦ **Serial Loopback Input Available for System Diagnostic Testing**
- ♦ **Loss-of-Lock ($\overline{LOL}$) Indicator**
- ♦ **Small 5mm × 5mm 32-Pin QFN Package**

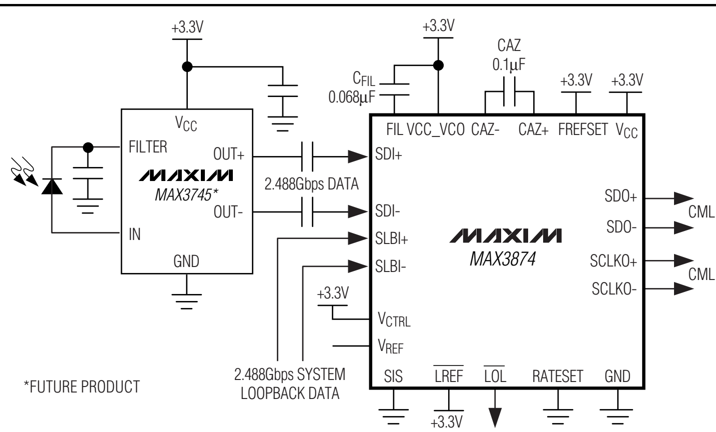
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3874EGJ	-40°C to +85°C	32 QFN-EP*	G3255-1
MAX3874AEGJ**	-40°C to +85°C	32 QFN-EP*	G3255-1

*EP = Exposed pad.
**Contains a VCO centered at 2.0212GHz.

Pin Configuration appears at end of data sheet.

Typical Application Circuit



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ....-0.5V to +5.0V
Input Voltage Levels (SDI+, SDI-, SLBI+, SLBI-) ....(V_{CC} - 1.0V) to (V_{CC} + 0.5V)
Input Current Levels (SDI+, SDI-, SLBI+, SLBI-).............±20mA
CML Output Current (SDO+, SDO-, SCLKO+, SCLKO-) ...±22mA
Voltage at $\overline{LOL}$, $\overline{LREF}$, SIS, FIL, RATESET, FREFSET, V_{CTRL}, V_{REF}, CAZ+, CAZ-.......................-0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
32-Pin QFN (derate 21.3mW/°C above +85°C) 1384mW
Operating Junction Temperature ....-55°C to +150°C
Storage Temperature Range ....-55°C to +150°C
Processing Temperature (die) ....+400°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Note 2)		175	215	mA
INPUT SPECIFICATION (SDI±, SLBI±)						
Single-Ended Input Voltage Range	V_{IS}	Figure 1	V_{CC} - 0.8		V_{CC} + 0.4	V
Input Common-Mode Voltage		Figure 1	V_{CC} - 0.4		V_{CC}	V
Input Termination to V_{CC}	R_{IN}		42.5	50	57.5	Ω
THRESHOLD-SETTING SPECIFICATION (SDI±)						
Differential Input Voltage Range (SDI±)		Threshold adjust enabled	50		600	mV_{P-P}
Threshold Adjustment Range	V_{TH}	Figure 2	-170		+170	mV
Threshold Control Voltage	V_{CTRL}	Figure 2 (Note 3)	0.3		2.1	V
Threshold Control Linearity				±5		%
Threshold Setting Accuracy		Figure 2	-18		+18	mV
Threshold Setting Stabiliity		15mV ≤ $\|V_{TH}\|$ ≤ 80mV	-6		+6	mV
		80mV < $\|V_{TH}\|$ ≤ 170mV	-12		+12	
Maximum Input Current	I_{CTRL}		-10		+10	µA
Reference Voltage Output	V_{REF}		2.14	2.2	2.24	V
CML OUTPUT SPECIFICATION (SDO±, SCLKO±)						
CML Differential Output Impedance	R_O		85	100	115	Ω
CML Output Common-Mode Voltage		(Note 4)		V_{CC} - 0.2		V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVTTL INPUT/OUTPUT SPECIFICATION ($\overline{LOL}$, $\overline{LREF}$, RATESET, FREFSET)						
LVTTL Input High Voltage	V_{IH}		2.0			V
LVTTL Input Low Voltage	V_{IL}				0.8	V
LVTTL Input Current			-10		+10	µA
LVTTL Output High Voltage	V_{OH}	I_{OH} = +20µA	2.4			V
LVTTL Output Low Voltage	V_{OL}	I_{OL} = -1mA			0.4	V

Note 1: At -40°C, DC characteristics are guaranteed by design and characterization.
Note 2: CML outputs open.
Note 3: Voltage applied to V_{CTRL} pin is from 0.3V to 2.1V when input threshold is adjusted from +170mV to -170mV.
Note 4: R_L = 50Ω to V_{CC}.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Input Data Rate		MAX3874 (RATESET = GND)		2.488		Gbps
		MAX3874 (RATESET = VCC)		2.667		
		MAX3874A		2.0212		
Differential Input Voltage (SDI±)	V_{ID}	Threshold adjust disabled, Figure 1 (Note 6)	10		1600	mV_{P-P}
Differential Input Voltage (SLBI±)		BER ≤ 10^{-10}	50		800	mV_{P-P}
Jitter Transfer Bandwidth	J_{BW}	MAX3874		1.5	2.0	MHz
		MAX3874A		0.75		
Jitter Peaking	J_P	f ≤ J_{BW}			0.1	dB
Sinusoidal Jitter Tolerance MAX3874		f = 100kHz	3.1	8.0		UI_{P-P}
		f = 1MHz	0.62	0.93		
		f = 10MHz	0.44	0.65		
Sinusoidal Jitter Tolerance (MAX3874A)		f = 1MHz (Note 7)		>0.5		UI_{P-P}
		f = 10MHz (Note 7)		>0.3		
Sinusoidal Jitter Tolerance with Threshold Adjust Enabled (Note 8)		f = 100kHz		7.1		UI_{P-P}
		f = 1MHz		0.82		
		f = 10MHz		0.54		
Jitter Generation	J_{GEN}	(Note 9)		2.7	4.0	mUI_{RMS}
Differential Input Return Loss (SDI±, SLBI±)	-20log $\lvert S_{11} \rvert$	100kHz to 2.5GHz		16		dB
		2.5GHz to 4GHz		15		
CML OUTPUT SPECIFICATION (SDO ±, SCLKO±)						
Output Edge Speed	t_r, t_f	20% to 80%			110	ps
CML Output Differential Swing		R_L = 100Ω differential	600	800	1000	mV_{P-P}
Clock-to-Q Delay	t_{CLK-Q}	(Note 10)	-40		+40	ps

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AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PLL ACQUISITION/LOCK SPECIFICATION						
Tolerated Consecutive Identical Digits		BER ≤ 10^{-10}		2000		Bits
Acquisition Time		Figure 4 (Note 11)			1.0	ms
$\overline{LOL}$ Assert Time		Figure 4	2.3		10.0	µs
Low-Frequency Cutoff for DC-Offset Cancellation Loop		CAZ = 0.1µF		4		kHz
CLOCK HOLDOVER SPECIFICATION						
Reference Clock Frequency				Table 4		
Maximum VCO Frequency Drift		(Note 12)			400	ppm

Note 5: Minimum and maximum AC characteristics are guaranteed by design and characterization using the MAX3874. Specifications apply to the MAX3874A only when noted.
Note 6: Jitter tolerance is guaranteed (BER ≤ 10^{-10}) within this input voltage range. Input threshold adjust is disabled with V_{CTRL} connected to V_{CC}.
Note 7: Measurements limited by equipment capability.
Note 8: Measured using a 100mV_{P-P} differential swing with a 20mVDC offset and an edge speed of 145ps (4th-order Bessel filter with f_{3dB} = 1.8GHz).
Note 9: Measured with 10mV_{P-P} differential input, 2^{23} - 1 PRBS pattern at OC-48 with bandwidth from 12kHz to 20MHz.
Note 10: Relative to the falling edge of the SCLKO+ (Figure 3).
Note 11: Measured at OC-48 data rate using a 0.068µF loop filter capacitor initialized to +3.6V.
Note 12: Measured at OC-48 data rate under $\overline{LOL}$ condition with the CDR clock output set by the external reference clock.

Timing Diagrams

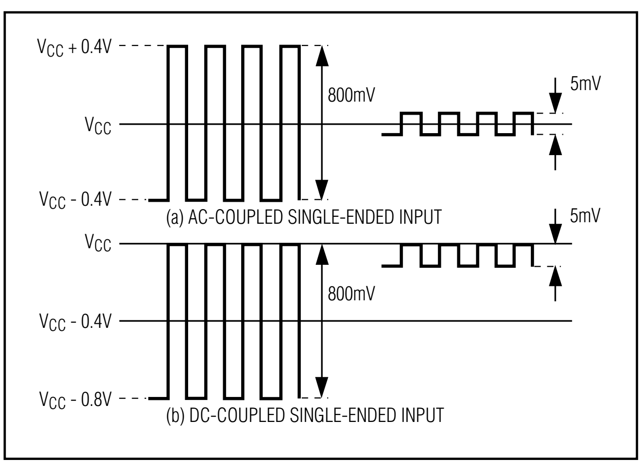


Figure 1. Definition of Input Voltage Swing

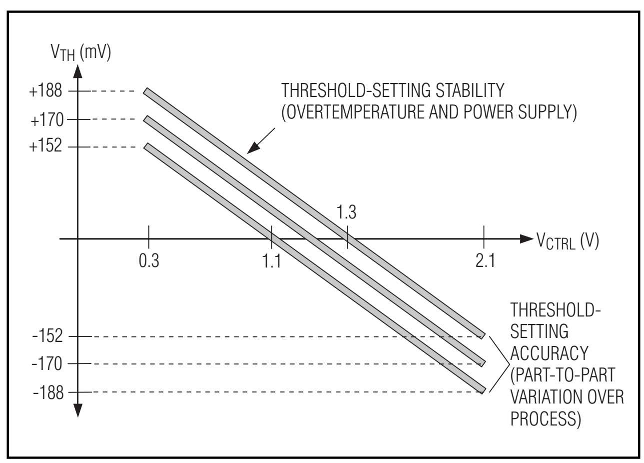


Figure 2. Relationship Between Control Voltage and Threshold Voltage

Timing Diagrams (continued)

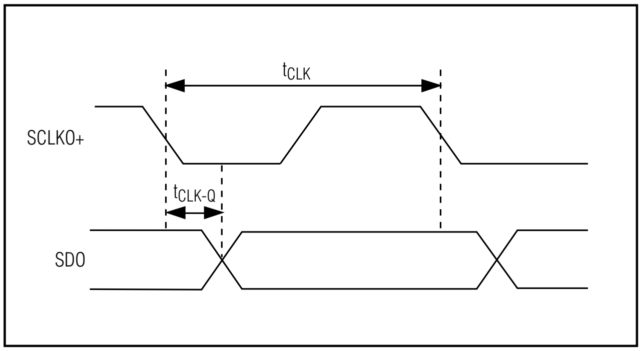


Figure 3. Definition of Clock-to-Q Delay

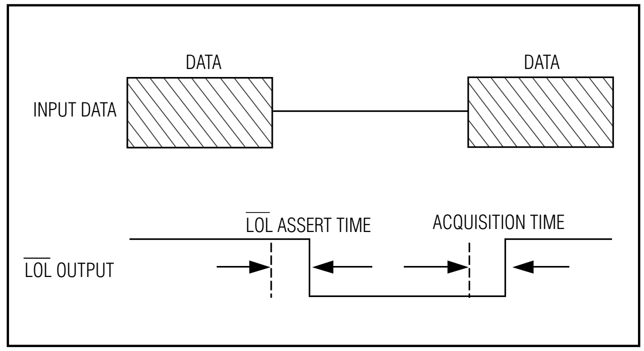
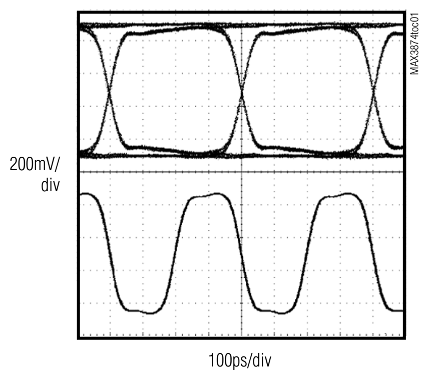


Figure 4. $\overline{LOL}$ Assert Time and PLL Acquisition Time Measurement

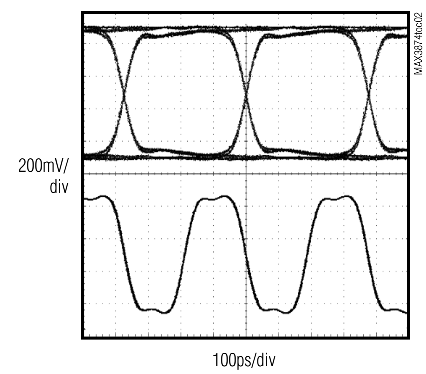
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

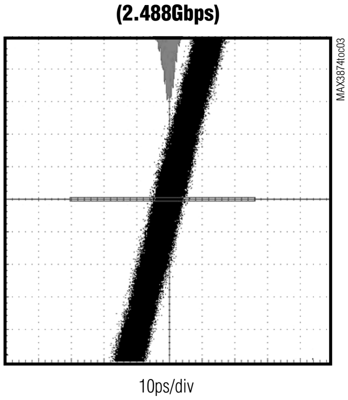
RECOVERED CLOCK AND DATA (2.488Gbps, 2^{23} - 1 PATTERN, V_{IN} = 10mV_{P-P})



RECOVERED CLOCK AND DATA (2.67Gbps, 2^{23} - 1 PATTERN, V_{IN} = 10mV_{P-P})

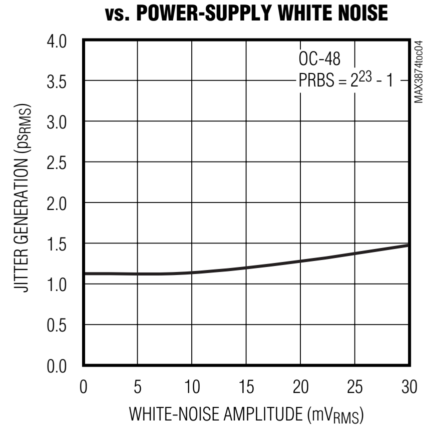


RECOVERED CLOCK JITTER (2.488Gbps)

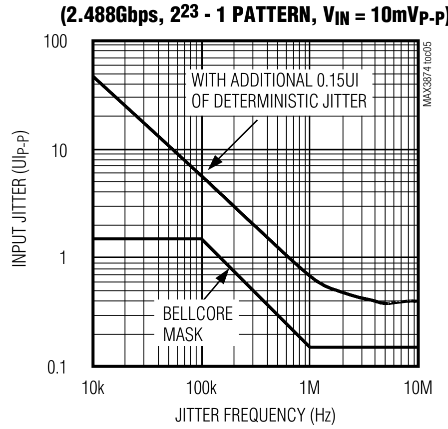


TOTAL WIDEBAND RMS JITTER = 1.60ps
PEAK-TO-PEAK JITTER = 12.20ps

JITTER GENERATION vs. POWER-SUPPLY WHITE NOISE



JITTER TOLERANCE (2.488Gbps, 2^{23} - 1 PATTERN, V_{IN} = 10mV_{P-P})

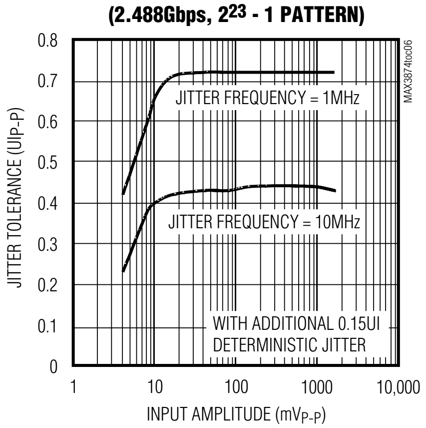


2.488Gbps/2.667Gbps Clock and Data Recovery with Limiting Amplifier

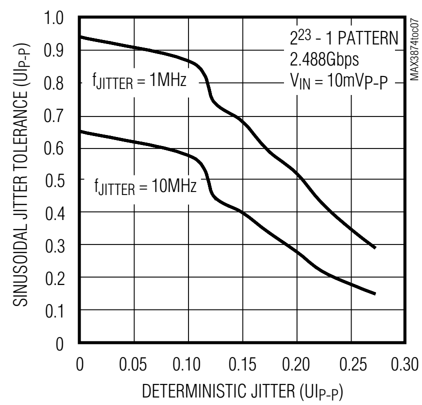
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

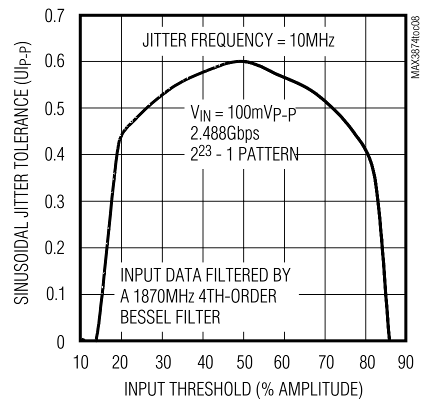
JITTER TOLERANCE vs. INPUT AMPLITUDE (2.488Gbps, 2^{23} - 1 PATTERN)



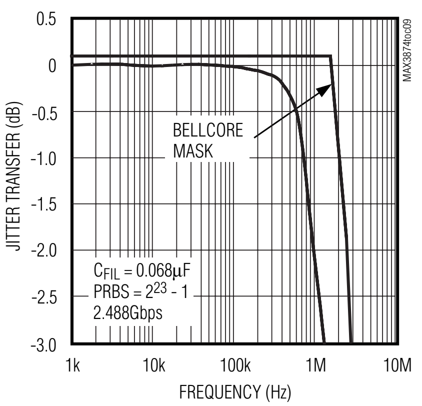
JITTER TOLERANCE vs. INPUT DETERMINISTIC JITTER



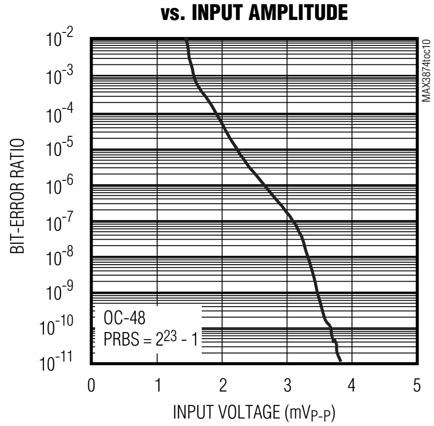
JITTER TOLERANCE vs. THRESHOLD ADJUST



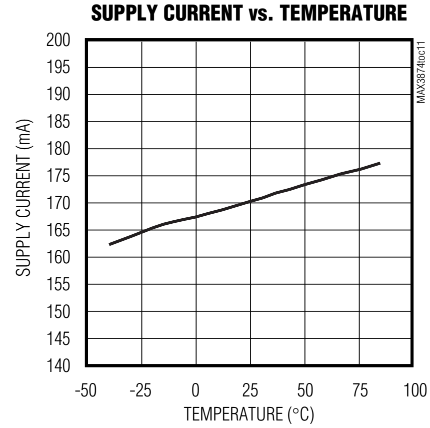
JITTER TRANSFER



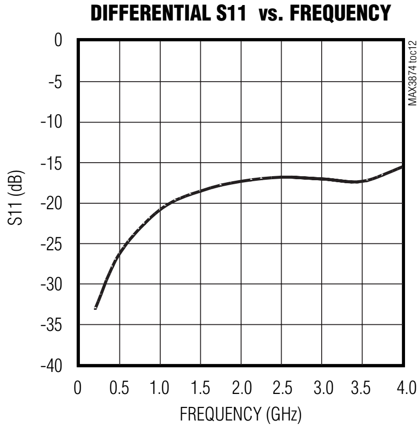
BIT-ERROR RATIO vs. INPUT AMPLITUDE



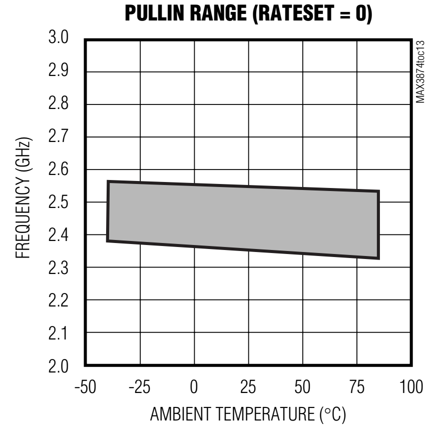
SUPPLY CURRENT vs. TEMPERATURE



DIFFERENTIAL S11 vs. FREQUENCY



PULLIN RANGE (RATESET = 0)



Pin Description

PIN	NAME	FUNCTION
1, 4, 27	V_{CC}	+3.3V Supply Voltage
2	SDI+	Positive Serial Data Input, CML
3	SDI-	Negative Serial Data Input, CML
5	SLBI+	Positive System Loopback Input or Reference Clock Input, CML
6	SLBI-	Negative System Loopback Input or Reference Clock Input, CML
7	SIS	Signal Selection Input, LVTTL. Set low for normal operation, set high for system loopback.
8	$\overline{\text{LREF}}$	Lock-to-Reference Clock Input, LVTTL. Set high for PLL lock to serial data, set low for PLL lock to reference clock.
9	$\overline{\text{LOL}}$	Loss-of-Lock Output, LVTTL. Active low.
10, 11, 16, 25, 32	GND	Supply Ground
12	FIL	PLL Loop-Filter Capacitor Input. Connect a 0.068µF capacitor between FIL and VCC_VCO.
13, 18	VCC_VCO	+3.3V Supply Voltage for the VCO
14, 15	N.C.	Not Connected
17	RATESET	VCO Frequency Select Input, LVTTL (Tables 2, 3, and 4)
19	SCLKO-	Negative Serial Clock Output, CML
20	SCLKO+	Positive Serial Clock Output, CML
21, 24	VCC_OUT	Supply Voltage for the CML Outputs
22	SDO-	Negative Serial Data Output, CML
23	SDO+	Positive Serial Data Output, CML
26	FREFSET	Reference Clock Frequency Select Input, LVTTL (Tables 2, 3, and 4)
28	CAZ+	Positive Capacitor Input for DC-Offset Cancellation Loop. Connect a 0.1µF capacitor between CAZ+ and CAZ-.
29	CAZ-	Negative Capacitor Input for DC-Offset Cancellation Loop. Connect a 0.1µF capacitor between CAZ+ and CAZ-.
30	V_{REF}	+2.2V Bandgap Reference Voltage Output. Optionally used for threshold adjustment.
31	V_{CTRL}	Analog Control Input for Threshold Adjustment. Connect to V_{CC} to disable threshold adjust.
EP	Exposed Pad	Ground. The exposed pad must be soldered to the circuit board ground for proper thermal and electrical performance.

2.488Gbps/2.667Gbps Clock and Data Recovery with Limiting Amplifier

Detailed Description

The MAX3874 consists of a fully integrated PLL limiting amplifier with threshold adjust, DC-offset cancellation loop, data retiming block, and CML output buffers (Figure 5). The PLL consists of a phase/frequency detector, a loop filter, and a VCO.

This device is designed to deliver the best combination of jitter performance and power dissipation by using a fully differential signal architecture and low-noise design techniques.

SDI Input Amplifier

The SDI inputs of the MAX3874 accept serial NRZ data with a differential input amplitude from $10mV_{P-P}$ to $1600mV_{P-P}$. The input sensitivity is $10mV_{P-P}$, at which the jitter tolerance is met for a BER of 10^{-10} with threshold adjust disabled. The input sensitivity can be as low as $4mV_{P-P}$ and still maintain a BER of 10^{-10}. The MAX3874 inputs are designed to directly interface with a transimpedance amplifier such as the MAX3745.

For applications in which vertical threshold adjustment is needed, the MAX3874 can be connected to the output of an AGC amplifier such as the MAX3861. When using the threshold adjust, the input voltage range is $50mV_{P-P}$ to $600mV_{P-P}$ (see the *Design Procedure* section).

SLBI Input Amplifier

The SLBI input amplifier accepts either NRZ loopback data or a reference clock signal. This amplifier can accept a differential input amplitude from $50mV_{P-P}$ to $800mV_{P-P}$.

Phase Detector

The phase detector incorporated in the MAX3874 produces a voltage proportional to the phase difference between the incoming data and the internal clock. Because of its feedback nature, the PLL drives the error voltage to zero, aligning the recovered clock to the center of the incoming data eye for retiming.

Frequency Detector

The digital frequency detector (FD) acquires frequency lock without the use of an external reference clock. The frequency difference between the received data and the VCO clock is derived by sampling the in-phase and quadrature VCO outputs on both edges of the data-input signal. Depending on the polarity of the frequency difference, the FD drives the VCO until the frequency difference is reduced to zero. Once frequency acquisition is complete, the FD returns to a neutral state. False locking is eliminated by this digital frequency detector.

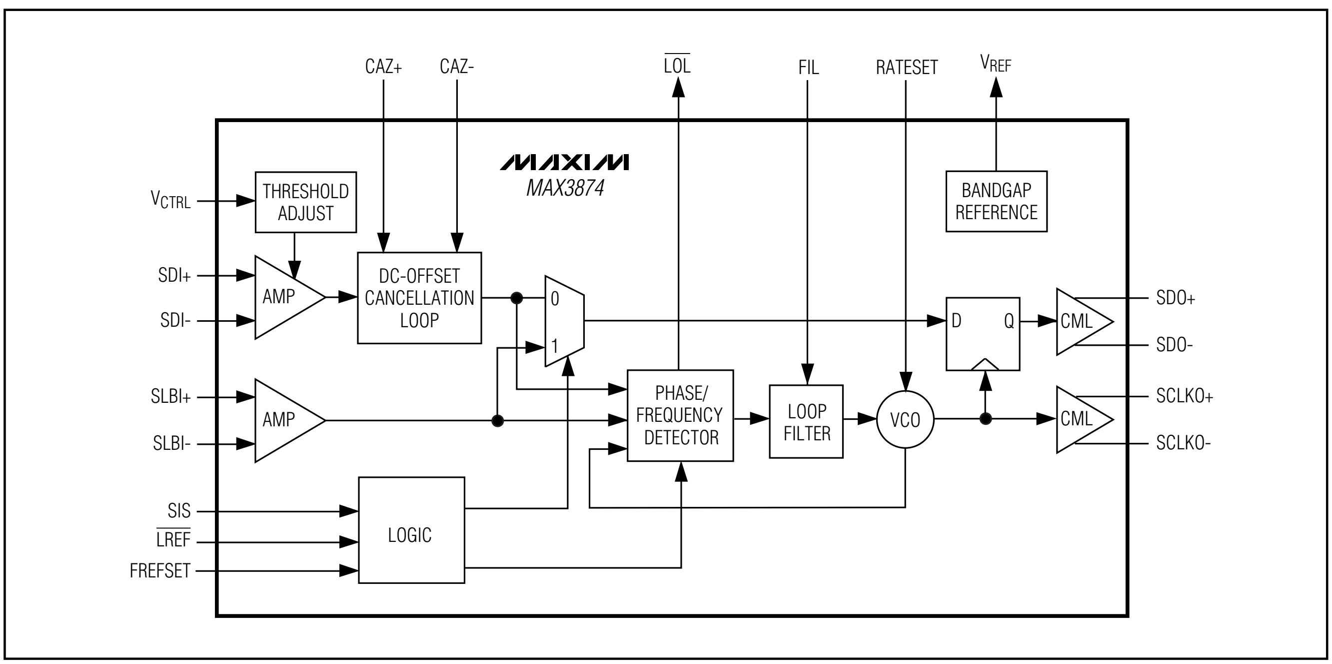


Figure 5. Functional Diagram

Loop Filter and VCO

The phase detector and frequency detector outputs are summed into the loop filter. An external capacitor (C_{FIL}) connected from FIL to VCC_VCO is required to set the PLL damping ratio. Note that the PLL jitter bandwidth does not change as the external capacitor changes, but the jitter peaking, acquisition time, and loop stability are affected. See the *Design Procedure* section for guidelines on selecting this capacitor.

The loop filter output controls the two on-chip VCOs. The VCOs provide low phase noise and are trimmed to the 2.488GHz and 2.667GHz frequencies. (The MAX3874A uses a single VCO trimmed to 2.0212GHz.) The RATESET pin is used to select the appropriate VCO. See Tables 2, 3, and 4 for the proper settings.

Loss-of-Lock Monitor

The $\overline{\text{LOL}}$ output indicates a PLL lock failure due to excessive jitter present at the data input or due to loss of input data. The $\overline{\text{LOL}}$ output is asserted low when the PLL loses lock.

DC-Offset Cancellation Loop

A DC-offset cancellation loop is implemented to remove the DC offset of the limiting amplifier. To minimize the low-frequency pattern-dependent jitter associated with this DC-cancellation loop, the low-frequency cutoff is 10kHz (typ) with CAZ = 0.1µF, connected from CAZ+ to CAZ-. The DC-offset cancellation loop operates only when threshold adjust is disabled.

Design Procedure

Decision Threshold Adjust

In applications in which the noise density is not balanced between logical zeros and ones (i.e., optical amplification using EDFA amplifiers), lower bit-error ratios (BERs) can be achieved by adjusting the input threshold. Varying the voltage at V_{CTRL} from +0.3V to +2.1V achieves a vertical decision threshold adjustment of +170mV to -170mV, respectively (Figure 2). Use the provided bandgap reference voltage output (V_{REF}) with a voltage-divider circuit or the output of a DAC to set the voltage at V_{CTRL}. See Figure 10 when using V_{REF} to generate the voltage for V_{CTRL}. V_{REF} can be used to generate the voltage for V_{CTRL} (Figure 10). If threshold adjust is not required, disable it by connecting V_{CTRL} directly to V_{CC} and leave V_{REF} floating.

Modes of Operation

The MAX3874 has three operational modes controlled by the $\overline{\text{LREF}}$ and SIS inputs: normal, system loopback, and clock holdover. Normal operation mode requires a serial data stream at the SDI± inputs, system loopback mode requires a serial data stream at the SLBI± inputs, and clock holdover mode requires a reference clock signal at the SLBI± inputs. See Table 1 for the required $\overline{\text{LREF}}$ and SIS settings. Once an operational mode is chosen, the remaining logic inputs (RATESET, FREFSET) program the input data rate or reference clock frequency.

Normal and System Loopback Settings

The RATESET pin is available for setting the SDI± and SLBI± inputs to receive the appropriate data rate. The FREFSET pin can be set to a zero or 1 while in normal or system-loopback mode (Tables 2 and 3).

Table 1. Operational Modes

MODE	$\overline{\text{LREF}}$	SIS
Normal	1	0
System loopback	1	1
Clock holdover	0	1 or 0

Table 2. Data-Rate Settings (MAX3874)

INPUT DATA RATE (Gbps)	RATESET	FREFSET
2.667	1	1 or 0
2.488	0	1 or 0

Table 3. Data-Rate Settings (MAX3874A)

INPUT DATA RATE (Gbps)	RATESET	FREFSET
2.0212	0	1 or 0

Table 4. Holdover Frequency Settings

REFERENCE CLOCK FREQUENCY (MHz)	SCLKO FREQUENCY (GHz)	RATESET	FREFSET
666.51	2.667	1	0
622.08	2.488	0	0
166.63	2.667	1	1
155.52	2.488	0	1

Clock Frequencies in Holdover Mode

Set the incoming reference-clock frequency and outgoing serial-clock frequency by setting RATESET and FREFSET appropriately (Table 3).

Setting the Loop Filter

The MAX3874 is designed for both regenerator and receiver applications. Its fully integrated PLL is a classic second-order feedback system, with a jitter transfer bandwidth (J_{BW}) below 2MHz. The external capacitor (C_{FIL}) connected from FIL to VCC_VCO sets the PLL damping. Note that the PLL jitter transfer bandwidth does not change as C_{FIL} changes, but the jitter peaking, acquisition time, and loop stability are affected. Figures 6 and 7 show the open-loop and closed-loop transfer functions.

The PLL zero frequency, f_Z, is a function of external capacitor C_{FIL}, and can be approximated according to:

$$f_Z = \frac{1}{2\pi(650\Omega)C_{FIL}}$$

For an overdamped system (f_Z / J_{BW} < 0.25), the jitter peaking (J_P) of a second-order system can be approximated by:

$$J_P = 20\log\left(1+\frac{f_Z}{J_{BW}}\right)$$

where J_{BW} is the jitter transfer bandwidth for a given data rate.

The recommended value of C_{FIL} = 0.068μF is to guarantee a maximum jitter peaking of less than 0.1dB. Decreasing C_{FIL} from the recommended value decreases acquisition time, with the trade-off of increased peaking. Excessive reduction of C_{FIL} can cause PLL instability. C_{FIL} must be a low-TC, high-quality capacitor of type X7R or better.

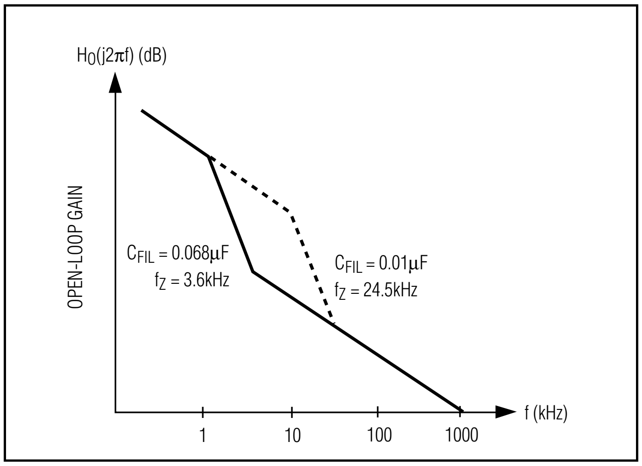


Figure 6. Open-Loop Transfer Function

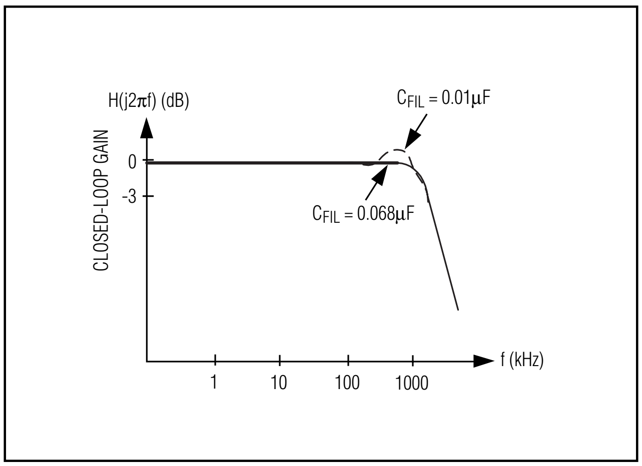


Figure 7. Closed-Loop Transfer Function

Input Terminations

The SDI± and SLBI± inputs of the MAX3874 are current-mode-logic (CML) compatible. The inputs all provide internal 50Ω termination to reduce the required number of external components. AC-coupling is recommended. See Figure 8 for the input structure. For additional information about logic interfacing, refer to Maxim Application Note HFAN 1.0: *Introduction to LVDS, PECL, and CML*.

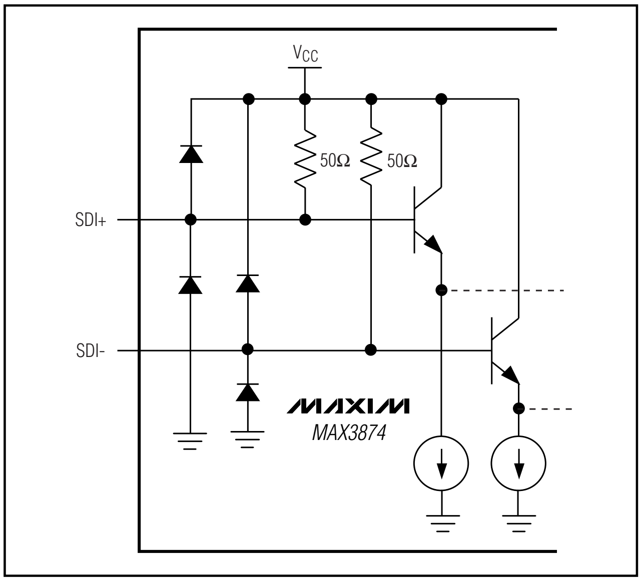


Figure 8. CML Input Model

Output Terminations

The MAX3874 uses CML for its high-speed digital outputs (SDO± and SCLKO±). The configuration of the output circuit includes internal 50Ω back terminations to V_{CC}. See Figure 9 for the output structure. CML outputs can be terminated by 50Ω to V_{CC}, or by 100Ω differential impedance. For additional information on logic interfacing, refer to Maxim Application Note HFAN 1.0: *Introduction to LVDS, PECL, and CML*.

Applications Information

Clock Holdover Capability

Clock holdover is required in some applications in which a valid clock must be provided to the upstream device in the absence of data transitions. To provide this function, an external reference clock signal must be applied to the SLBI± inputs and the proper control signals set (see the *Modes of Operation* section). To enter holdover mode automatically when there are no transitions applied to the SDI+ inputs, $\overline{LOL}$ or the system $\overline{LOS}$ can be directly connected to $\overline{LREF}$.

System Loopback

The MAX3874 is designed to allow system-loopback testing. When the device is set for system-loopback mode, the serial output data of a transmitter can be directly connected to the SLBI inputs to run system diagnostics. See Table 1 for selecting system loopback operation mode. While in system loopback mode, $\overline{LREF}$ should not be connected to $\overline{LOL}$.

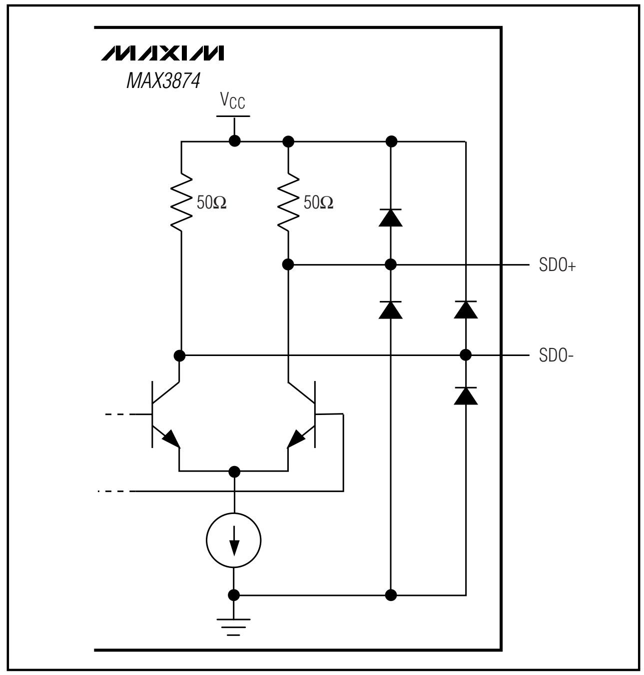


Figure 9. CML Output Model

Consecutive Identical Digits (CIDs)

The MAX3874 has a low phase and frequency drift in the absence of data transitions. As a result, long runs of consecutive zeros and ones can be tolerated while maintaining a BER better than 10^{-10}. The CID tolerance is tested using a 2^{13} - 1 PRBS with long runs of ones and zeros inserted in the pattern. A CID tolerance of 2000 bits is typical.

Exposed Pad (EP) Package

The EP, 32-pin QFN incorporates features that provide a very low thermal-resistance path for heat removal from the IC. The pad is electrical ground on the MAX3874 and should be soldered to the circuit board for proper thermal and electrical performance.

Layout Considerations

For best performance, use good high-frequency layout techniques. Filter voltage supplies, keep ground connections short, and use multiple vias where possible. Use controlled-impedance transmission lines to interface with the MAX3874 high-speed inputs and outputs. Place power-supply decoupling as close to V_{CC} as possible. To reduce feedthrough, isolate the input signals from the output signals. If a bare die is used, mount the back of die to ground (GND) potential.

Figure 10 shows interfacing with the MAX3861 AGC using threshold adjust.

2.488Gbps/2.667Gbps Clock and Data Recovery with Limiting Amplifier

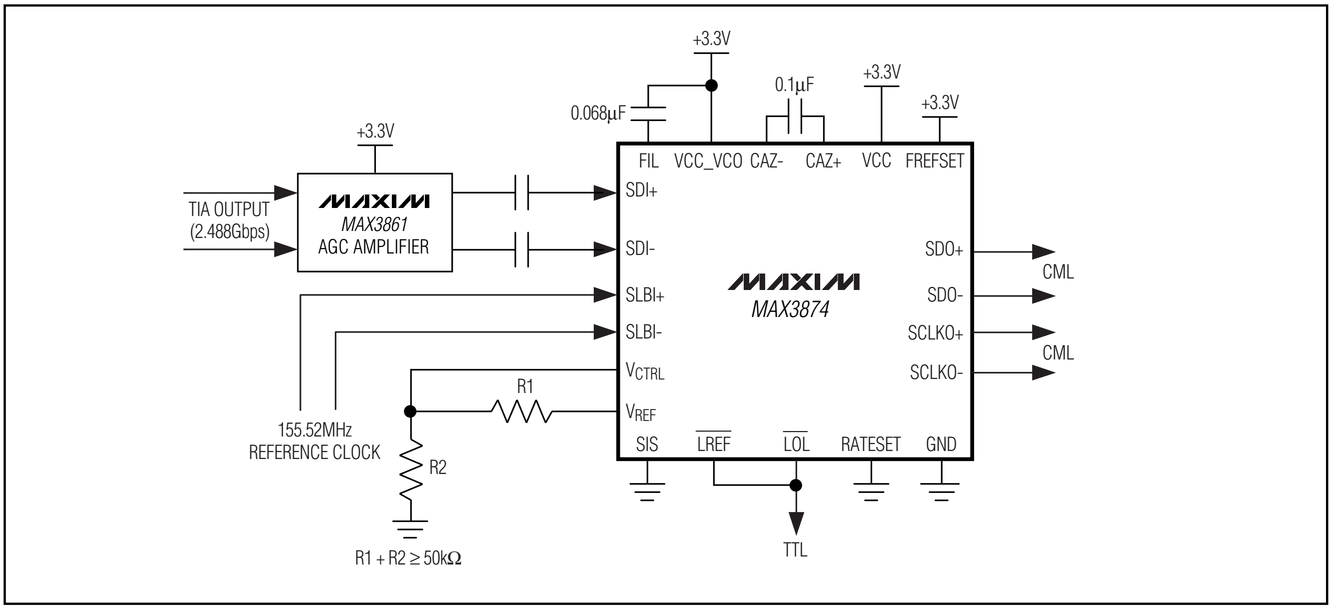
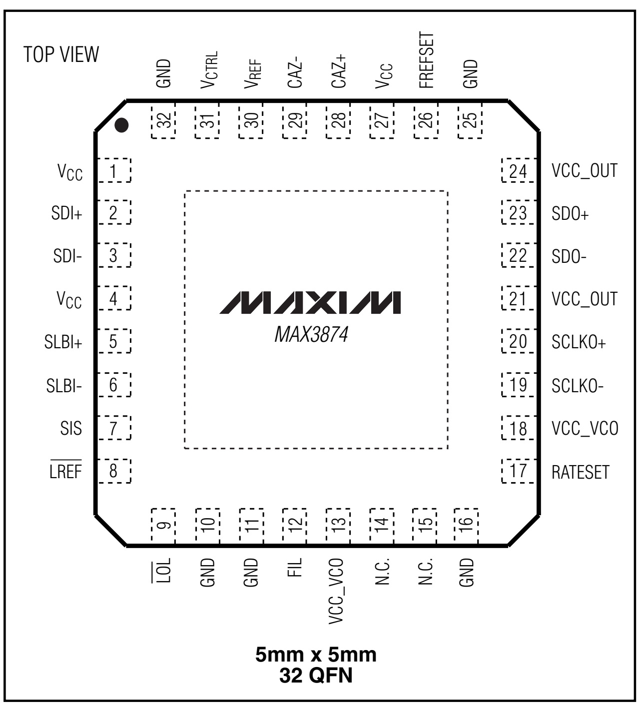


Figure 10. Interfacing with the MAX3861 AGC Using Threshold Adjust

Pin Configuration



Chip Information

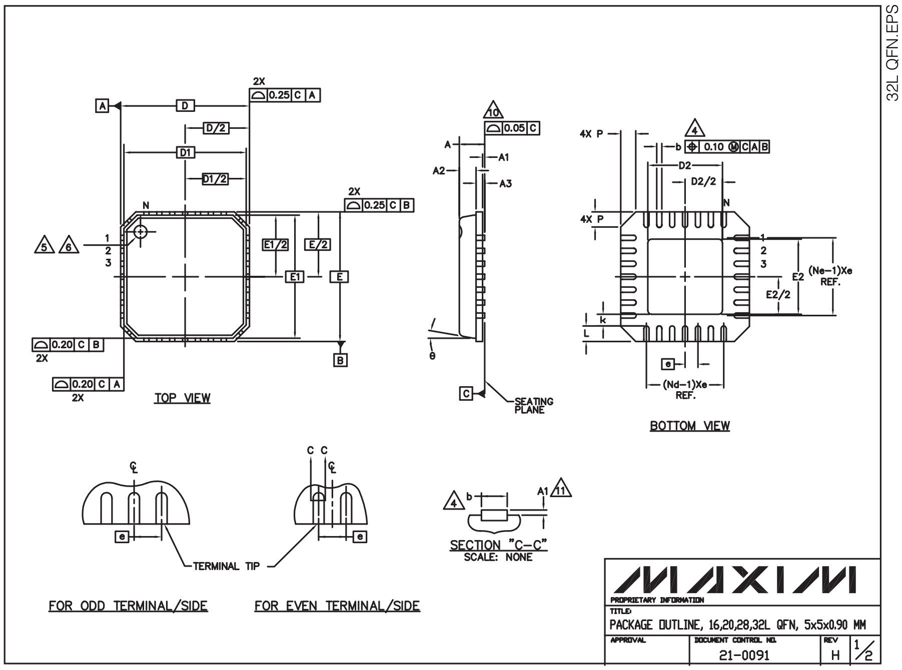
TRANSISTOR COUNT: 5142

PROCESS: SiGe BiPOLAR

SUBSTRATE: SOI

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS												
PKG	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
θ	0°		12°	0°		12°	0°		12°	0°		12°

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1655-3	2.95	3.10	3.25	2.95	3.10	3.25
G2055-1	2.55	2.70	2.85	2.55	2.70	2.85
G2055-2	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM
APPROVAL | DOCUMENT CONTROL NO. 21-0091 | REV H | 2/2

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