

2.7Gbps Post Amp with Automatic Gain Control

General Description

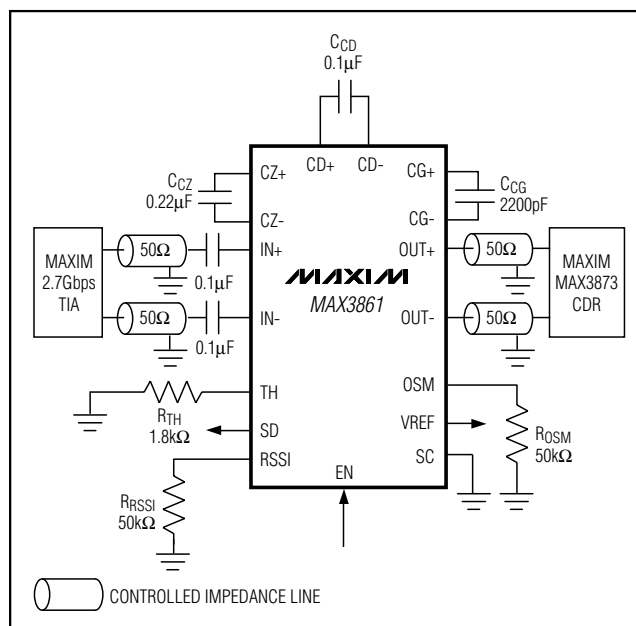
The MAX3861 is a low-power amplifier with automatic gain control (AGC), designed for WDM transmission systems employing optical amplifiers and requiring a vertical threshold adjustment after the post amp. Operating from a single 3.3V supply, this AGC amplifier linearly amplifies/attenuates the input signal while maintaining a fixed output-voltage swing at data rates up to 2.7Gbps. Both the input and output are on-chip terminated to match 50Ω interfaces.

This amplifier has a small-signal bandwidth of 3.4GHz and an input-referred noise of 0.26mVRMS. Over an input signal range of 6mVp-p to 1200mVp-p (46dB), the MAX3861 delivers a constant output amplitude that is adjustable from 400mVp-p to 920mVp-p. Variation in output swing is controlled within 0.2dB over a 16dB input range. The MAX3861 provides a received-signal-strength indicator (RSSI) that is linear, within 2.5%, for input signal levels up to 100mVp-p and an input signal detect (SD) with programmable threshold.

Applications

OC-48/STM-16 Transmission Systems
WDM Optical Receivers
Long Reach Optical Receivers
Continuous Rate Receivers

Typical Application Circuit



Features

- ◆ Single 3.3V Power Supply
- ◆ 72mA Supply Current
- ◆ 3.4GHz Small-Signal Bandwidth
- ◆ 0.26mVRMS Input-Referred Noise
- ◆ 6mVp-p to 1200mVp-p Input Range (46dB)
- ◆ Input Signal Detect with Programmable Threshold
- ◆ RSSI (Linear Up to 100mVp-p)
- ◆ Adjustable Output Amplitude
- ◆ 0.2dB Output Voltage Variation (Over 16dB Input Signal Variation)

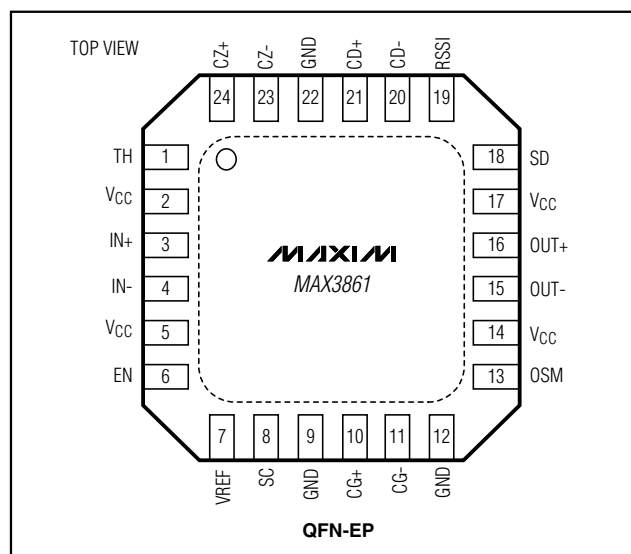
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3861EGG	-40°C to +85°C	24 QFN*
MAX3861E/D	-40°C to +85°C	Dice**

*EP = Exposed Pad

**Dice are designed to operate over a -40°C to +120°C junction temperature (T_J) range, but are tested and guaranteed at $T_A = +25^\circ\text{C}$.

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage-0.5V to +4.0V
 Voltage at IN+, IN-(V_{CC} - 1.5V) to (V_{CC} + 0.5V)
 Voltage at CZ+, CZ-, CG+,
 CG-, CD+, CD-(V_{CC} - 3.5V) to (V_{CC} + 0.5V)
 Voltage at SC, SD, EN, TH,
 OSM, VREF, and RSSI-0.5V to (V_{CC} + 0.5V)

CML Input Current at IN+, IN-25mA
 CML Output Current at OUT+, OUT-25mA
 Storage Temperature Range-55°C to +150°C
 Operating Junction Temperature Range-55°C to +150°C
 Lead Temperature (soldering, 10s)+300°C
 Processing Temperature (Die)+400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I _{CC}	RSSI and SD enabled (Notes 2, 3)	At minimum gain		72	86	mA
			At maximum gain		94	112	
		RSSI and SD disabled (Notes 2, 3)	At minimum gain		57	69	
			At maximum gain		78	94	
Power-Supply Noise Rejection	PSNR	V _{NOISE} = 100mV _{P-P} , f _{NOISE} ≤ 10MHz, V _{SC} = 2V (Note 4)	V _{IN} = 1000mV _{P-P}		35		dB
			V _{IN} = 10mV _{P-P}		25		
Input Data Rate					2.7		Gbps
Input Resistance	R _{IN}	Single ended to V _{CC}		40	50	60	Ω
Input Return Loss		≤2.7GHz			21		dB
		2.7GHz to 4.0GHz			15		
Input Common-Mode Level				V _{CC} - 0.3		V _{CC}	V
Input-Referred Noise		Up to 6GHz at max gain, C _{CZ} = 0.1μF			0.26	0.35	mV _{RMS}
Input Voltage Range	V _{IN}	Differential		6		1200	mV _{P-P}
Maximum Differential Input Voltage for Linear Operation		0.9 ≤ linearity ≤ 1.1	V _{SC} = 0		700		mV _{P-P}
			V _{SC} = 2V		650		
Output Resistance	R _{OUT}	Single ended to V _{CC}		40	50	60	Ω
Output Return Loss		≤2.7GHz			16		dB
		2.7GHz to 4.0GHz			11		
Output Common-Mode Level		R _L = 50Ω to V _{CC}	V _{SC} = 0		V _{CC} - 0.13		V
			V _{SC} = 2V		V _{CC} - 0.28		
Maximum Differential Output Offset		V _{SC} = 0, R _L = 50Ω to V _{CC} (Note 5)	6mV _{P-P} ≤ V _{IN} ≤ 700mV _{P-P}		±3	±14	mV
			700mV _{P-P} ≤ V _{IN} ≤ 1200mV _{P-P}		±8		
		V _{SC} = 2V, R _L = 50Ω to V _{CC} (Note 5)	6mV _{P-P} ≤ V _{IN} ≤ 700mV _{P-P}		±5.5	±28	
			700mV _{P-P} ≤ V _{IN} ≤ 1200mV _{P-P}		±11		

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +3.0V$ to $+3.6V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Output Amplitude	V _{OUT}	R _L = 50Ω to V _{CC} (Note 6)	V _{SC} = 0	300	400	500	mV _{P-P}
			V _{SC} = 2V	760	920	1050	
Output Amplitude Variation	ΔV _{OUT}	V _{IN} ≥ 6mV _{P-P} , R _L = 50Ω to V _{CC} (Notes 6, 7)			0.2	1.0	dB
Small Signal Bandwidth	BW	(Note 3)	At minimum gain	2.5	3.4	5.5	GHz
			At maximum gain	2.2	2.9	4.3	
Low-Frequency Cutoff		C _{CZ} = 0.1μF			7.6	13	kHz
Deterministic Jitter		(Note 8)			15	50	psp-p
Output Signal Monitor Voltage	V _{OSM}	R _{OSM} ≥ 2kΩ (Note 6)	V _{OUT} = 920mV _{P-P}	2.0			V
			V _{OUT} = 400mV _{P-P}	0.9			
Output Signal Monitor Linearity		0V ≤ V _{SC} ≤ 2V (Note 6)		±10			%
SC Input Range		(Note 9)		0		2.0	V
AGC Loop Constant		Without external capacitor C _{CG} , V _{SC} = 0 (Note 10)		16			μs
RSSI Output Voltage	RSSI	R _{RSSI} ≥ 2kΩ, V _{SC} = 0 (Note 6)	V _{IN} = 2mV _{P-P}	55			mV
			V _{IN} = 100mV _{P-P}	1800			
RSSI Linearity		2mV _{P-P} ≤ V _{IN} ≤ 100mV _{P-P} (Note 14)		±2.5	±12		%
		6mV _{P-P} ≤ V _{IN} ≤ 100mV _{P-P}		±2.5	±8		
Minimum SD Assert Input				2			mV _{P-P}
Maximum SD Assert Input				100			mV _{P-P}
SD Assert Time				10	70		μs
SD Deassert Time		CG+ and CG- are open (Note 11)		10	44		μs
SD Accuracy		(Note 12)		±10			%
SD Hysteresis		10mV _{P-P} ≤ V _{IN} ≤ 100mV _{P-P}		2.8	4.5	6.3	dB
		2mV _{P-P} ≤ V _{IN} ≤ 10mV _{P-P} (Note 13)		4.5			
SD Output High Voltage		Sourcing 20μA current		2.4			V
SD Output Low Voltage		Sinking 2mA current				0.44	V
EN Input Low Voltage	V _{IL}					0.8	V
EN Input High Voltage	V _{IH}			2.0			V
EN Input Low Current	I _{IL}	V _{IL} = 0				10	μA
EN Input High Current	I _{IH}	V _{IH} = 2.0V				10	μA
VREF Output Voltage		R _{VREF} ≥ 40kΩ		2.0			V

Note 1: Electrical characteristics are measured or characterized using a 2²³ - 1PRBS at 2.7Gbps with input edge speeds $\leq 200ps$, unless otherwise noted. Dice are tested at $T_A = +25^{\circ}C$ only. All AC specifications are guaranteed by design and characterization, unless otherwise noted.

Note 2: Supply current measurement is taken with AC-coupled inputs and excludes output currents into 50Ω loads.

Note 3: Minimum gain is defined as $V_{IN} = 1200mV_{P-P}$ and $V_{OUT} = 400mV_{P-P}$. Maximum gain is defined as $V_{IN} = 6mV_{P-P}$ and $V_{OUT} = 920mV_{P-P}$. Reference gain is measured at 100MHz.

Note 4: Power-supply noise rejection is characterized with a 2.7Gbps 1100 pattern on the input. It is calculated by the equation $PSNR = 20\log(\Delta V_{CC} / (\Delta V_{OUT}))$, where ΔV_{OUT} is the change in differential output voltage because of power-supply noise. See Power Supply Noise Rejection vs. Frequency in the *Typical Operating Characteristics*.

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +3.0V$ to $+3.6V$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

Note 5: See Distribution of Differential Output Offset (Worst-Case Conditions) in the *Typical Operating Characteristics*.

Note 6: Characterized with a 675Mbps 1-0 pattern.

Note 7: Measurements are taken over an input signal range of 16dB.

Note 8: Deterministic jitter is defined as the arithmetic sum of PWD (pulse-width distortion) and PDJ (pattern-dependent jitter). Deterministic jitter is the difference of total jitter and random jitter, with system jitter calibrated out. It is measured with a 2^7 - 1PRBS, and 80CIDs with DC-coupled outputs.

Note 9: Typical input resistance of SC pin is 40k Ω .

Note 10: AGC loop time constant is measured with a 20dB change in the input and V_{SC} held constant. With an external capacitor C_{CG} of 0.022 μF connected between CG+ and CG-, a typical AGC loop time constant of 760 μs is achieved.

Note 11: SD deassert time depends on the AGC loop time constant set by C_{CG} .

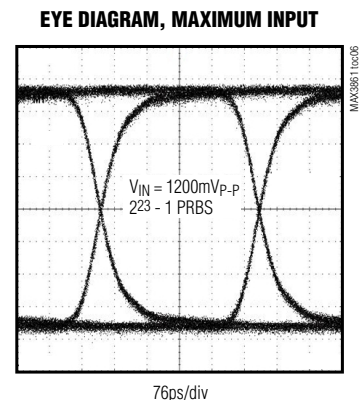
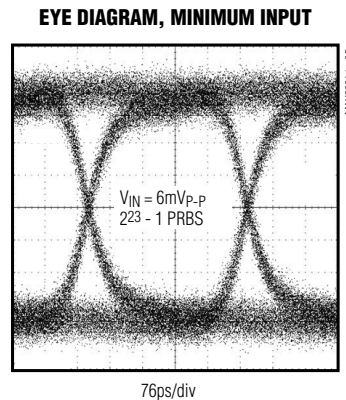
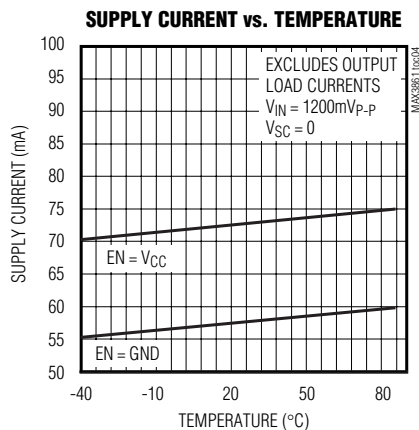
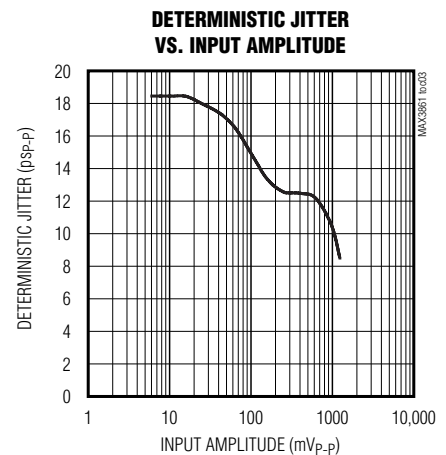
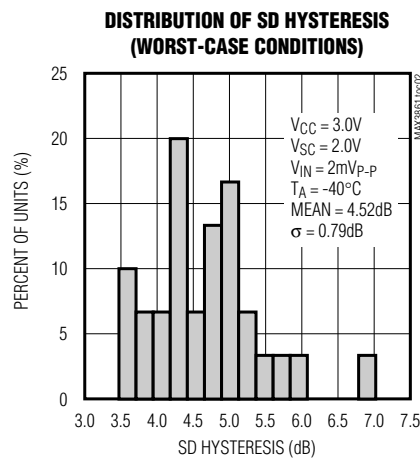
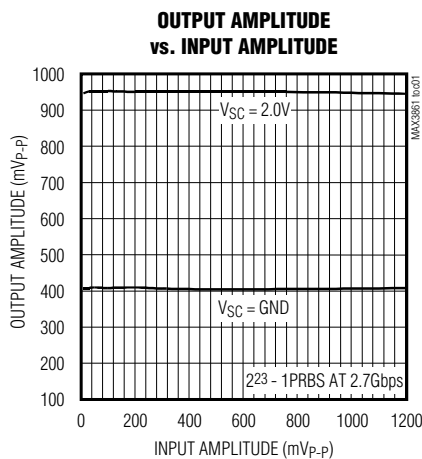
Note 12: SD accuracy is defined as the part-to-part variation of the SD threshold at a fixed R_{TH} value.

Note 13: See Distribution of SD Hysteresis (Worst-Case Conditions) in the *Typical Operating Characteristics*.

Note 14: Measurements are taken over an input signal range of 20dB.

Typical Operating Characteristics

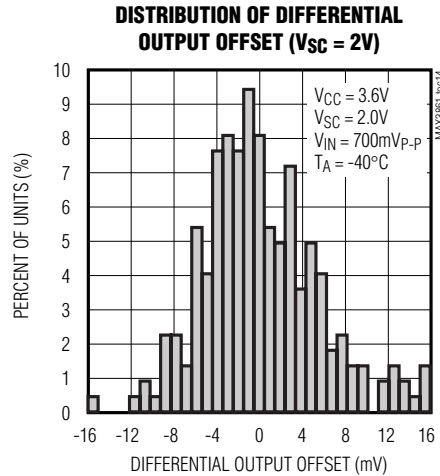
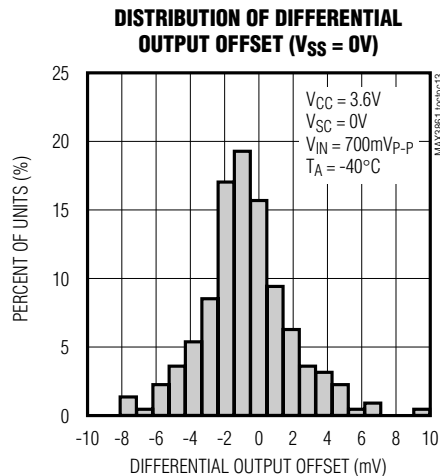
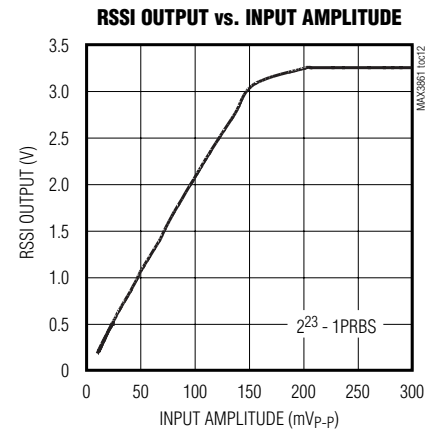
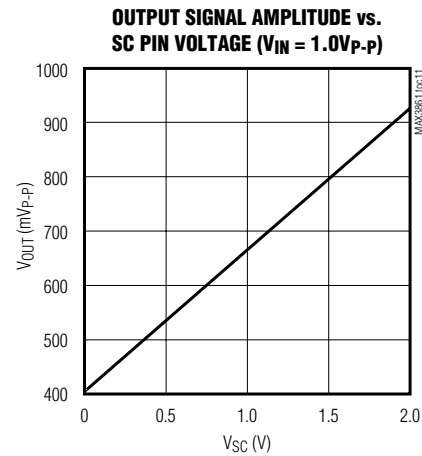
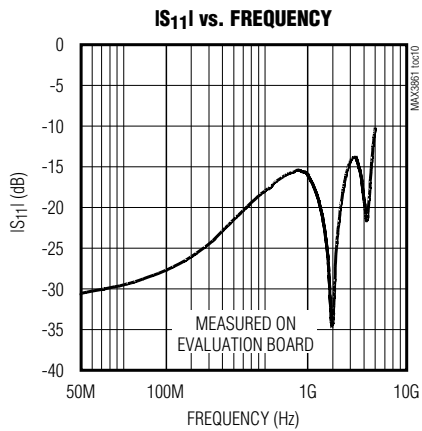
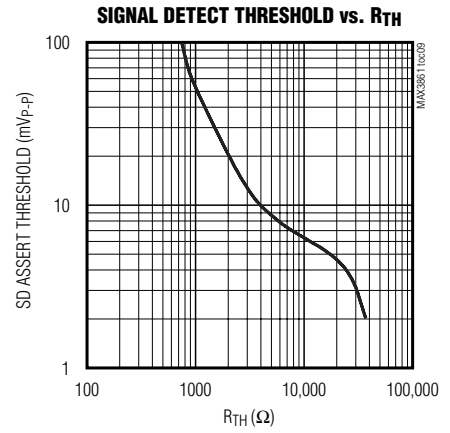
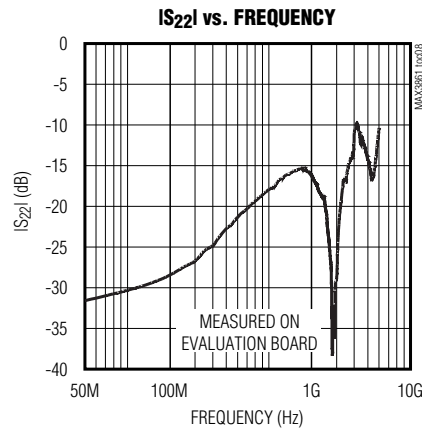
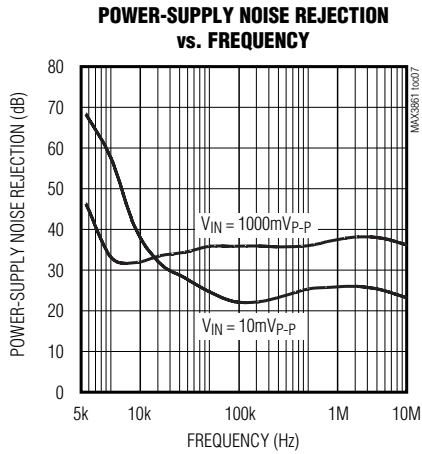
($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Description

PIN	NAME	FUNCTION
1	TH	Input Signal Detect Threshold Programming Pin. Attach a resistor between this pin and ground to program the input signal detect assert threshold. Leaving this pin open sets the signal detect threshold to its absolute minimum value ($<2\text{mV}_{\text{P-P}}$). See the <i>Design Procedure</i> section.
2, 5, 14, 17	V _{CC}	Supply Voltage Connection. Connect all V _{CC} pins to the board V _{CC} plane.
3	IN+	Positive CML Signal Input with On-Chip Termination Resistor
4	IN-	Negative CML Signal Input with On-Chip Termination Resistor
6	EN	Signal Detect Enable. Set high ($\geq 2.0\text{V}$) or leave open to enable the input signal detection (RSSI and SD) circuitry. Set low ($\leq 0.4\text{V}$) to power-down the input signal detection circuitry.
7	VREF	Reference Voltage Output (2.0V). Connect this pin to the SC pin for maximum output signal swing.
8	SC	Output Amplitude External Control. Ground SC for minimum output amplitude. Apply 2.0V to SC or connect SC directly to VREF for maximum output amplitude.
9, 12, 22	GND	Ground. Connect all GND pins to the board ground plane.
10	CG+	Connection for AGC Loop Capacitor. A capacitor connected between CG+ and CG- sets the AGC loop time constant.
11	CG-	Connection for AGC Loop Capacitor. A capacitor connected between CG+ and CG- sets the AGC loop time constant.
13	OSM	Output Signal Monitor. This DC signal is linearly proportional to the output signal amplitude.
15	OUT-	Negative CML Data Output with On-Chip Back-Termination Resistor
16	OUT+	Positive CML Data Output with On-Chip Back-Termination Resistor
18	SD	Input Signal Detect. Asserts logic low when the input signal level drops below the programmed threshold.
19	RSSI	Received Signal Strength Indicator. Outputs a DC signal that is linearly proportional to the input signal amplitude.
20	CD-	Connection for Signal Detect Capacitor. A capacitor connected between CD+ and CD- sets the offset-cancellation loop time constant of the input signal detection. See the <i>Detailed Description</i> section.
21	CD+	Connection for Signal Detect Capacitor. A capacitor connected between CD+ and CD- sets the offset-cancellation loop time constant of the input signal detection. See the <i>Detailed Description</i> section.
23	CZ-	Connection for Offset-Cancellation Loop Capacitor. A capacitor connected between CZ+ and CZ- sets the offset-cancellation loop time constant of the main signal path. See the <i>Detailed Description</i> section.
24	CZ+	Connection for Offset-Cancellation Loop Capacitor. A capacitor connected between CZ+ and CZ- sets the offset-cancellation loop time constant of the main signal path. See the <i>Detailed Description</i> section.
EP	Exposed Pad	Maxim recommends connecting the exposed pad to board ground.

2.7Gbps Post Amp with Automatic Gain Control

Detailed Description

Figure 1 is a functional diagram of the MAX3861 automatic gain-control amplifier. The MAX3861 is divided into three sections: main signal path, input signal detection, and output signal detection.

Main Signal Path

The main signal path consists of variable gain amplifiers with CML output levels and an offset cancellation loop. This configuration allows for overall gains ranging from -9.5dB to 43.5dB.

Offset-Cancellation Loop

The offset-cancellation loop partially reduces additional offset at the input. In communications systems using NRZ data with a 50% duty cycle, pulse-width distortion present in the signal or generated by the transimpedance amplifier appears as input offset and is partially removed by the offset cancellation loop. An external capacitor is required between CZ+ and CZ- to compensate the offset cancellation loop and determine the lower 3dB frequency of the signal path.

Input Signal Detection and SD Circuitry

The input signal detection circuitry consists of variable gain amplifiers and threshold voltages. Input signal detection information is compared to an internal reference and creates the RSSI voltage and an internal reference signal. The signal detect (SD) circuitry indicates when the input signal is below the programmed threshold by comparing a voltage proportional to the RSSI signal with internally generated control voltages. The SD threshold is set by a control voltage developed across the external TH resistor (R_{TH}). Two control voltages, VASSERT and VDEASSERT, define the signal detect assert and deassert levels. To prevent SD chatter in the region of the programmed threshold, 2.8dB to 6.3dB of hysteresis is built into the SD assert/deassert function and thus, once asserted, SD is not deasserted until sufficient gain is retained. When input signal detection (SD and RSSI) is not required, tie EN to a TTL low to power-down this circuitry.

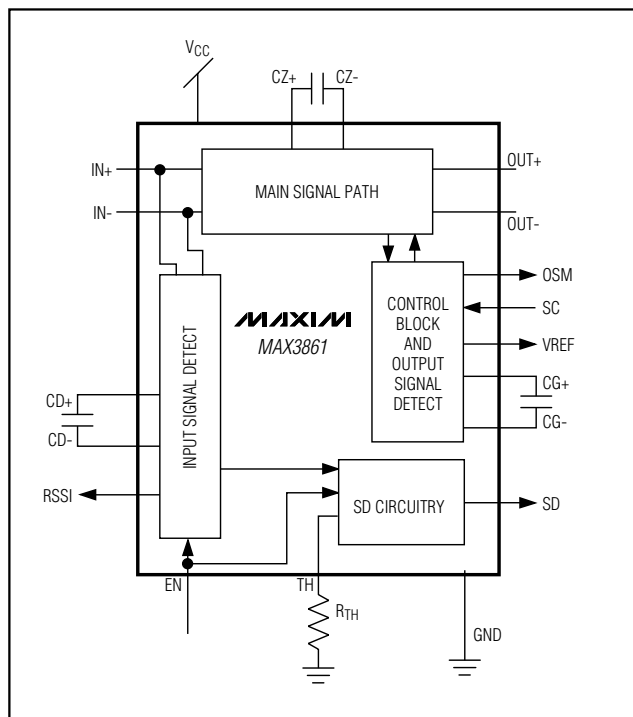


Figure 1. Functional Diagram

Output Signal Monitor and Amplitude Control

Output amplitude typically can be adjusted from 400mV_{P-P} to 920mV_{P-P} by applying a control voltage (0V to 2.0V) to the SC pin. See Output Signal Amplitude vs. SC Pin Voltage in the *Typical Operating Characteristics*. Connect the VREF pin (2.0V) to the SC pin for maximum output amplitude. The output signal monitor pin provides a DC voltage that is linearly proportional to the output signal.

Design Procedure

Program the SD Threshold

The SD threshold is programmed by an external resistor, R_{TH} , between the range of 2mV_{P-P} to 100mV_{P-P}. The circuit is designed to have approximately 4.5dB of hysteresis over the full range. See Signal Detect Threshold vs. R_{TH} graph in the *Typical Operating Characteristics* for proper sizing.

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Select the Coupling Capacitors

When AC-coupling is desired, coupling capacitors C_{IN} and C_{OUT} should be selected to minimize the receiver's deterministic jitter. Jitter is decreased as the input low-frequency cutoff (f_{IN}) is decreased.

$$f_{IN} = \frac{1}{2\pi(50)(C_{IN})}$$

For ATM/SONET or other applications using scrambled NRZ data, select (C_{IN} , C_{OUT}) $\geq 0.1\mu F$, which provides $f_{IN} < 32kHz$. For Fibre Channel, Gigabit Ethernet, or other applications using 8B/10B data coding, select (C_{IN} , C_{OUT}) $\geq 0.01\mu F$, which provides $f_{IN} < 320kHz$.

Setting the Offset-Cancellation Loop Time Constant for Input Signal Detection Circuitry (Selecting C_{CD})

The capacitor between $CD+$ and $CD-$ determines the time constant of the input signal detection DC offset-cancellation loop. A value of $0.1\mu F$ for C_{CD} provides a low-frequency cutoff (f_C) below $10kHz$. If a lower cutoff frequency is desired, $0.22\mu F$ gives $f_C = 4.5kHz$ and $0.47\mu F$ gives $f_C = 2.1kHz$. To guarantee stable operation, a capacitor of less than $0.01\mu F$ should not be used.

Setting the Offset-Cancellation Loop Time Constant for the Main Signal Path (Selecting C_{CZ})

The capacitor between $CZ+$ and $CZ-$ determines the time constant of the signal path DC offset-cancellation loop. To maintain stability, it is important to keep a one-decade separation between f_{IN} and the low-frequency cutoff (f_{OC}) associated with the DC offset-cancellation circuit. For SONET applications, $f_{IN} < 32kHz$, so $f_{OCMAX} < 3.2kHz$. Therefore, $C_{CZ} = 0.22\mu F$ ($f_{OC} = 2.99kHz$), $C_{CZ} = 0.47\mu F$ ($f_{OC} = 1.4kHz$), or a greater value may be used. To guarantee stable operation, a capacitor of less than $0.01\mu F$ should not be used.

Setting the Automatic Gain-Control Loop Time Constant (Selecting C_{CG})

The automatic gain-control loop time constant is determined by the external capacitor connected between $CG+$ and $CG-$. A value of at least $0.0022\mu F$ is recommended.

Programming the Output Amplitude (Programming the SC Pin)

Output amplitude can be programmed from $400mV_{P-P}$ to $920mV_{P-P}$ by applying a voltage to the SC pin. See Output Signal Amplitude vs SC Pin Voltage in the *Typical Operating Characteristics*.

Applications Information

Wire Bonding Die

For high current density and reliable operation, the MAX3861 uses gold metallization. Make connections to the dice with gold wire only, and use ball-bonding techniques (wedge bonding is not recommended). The MAX3861 has two types of bond pads: the dimensions for square bondpads are 94.4 microns by 94.4 microns; the dimensions for the octagonal bondpads are 33.6 microns per side. Die thickness is $12mils$ ($0.305mm$).

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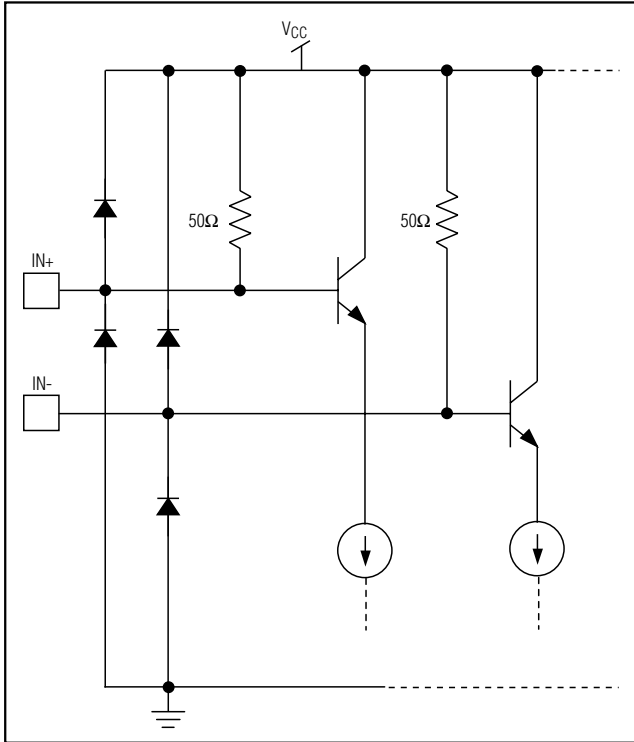


Figure 2. Input Interface

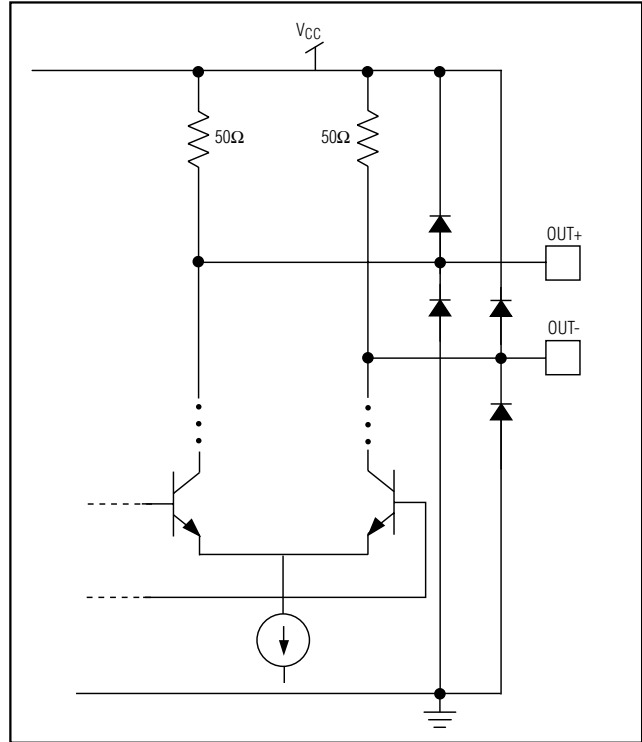


Figure 3. Output Interface

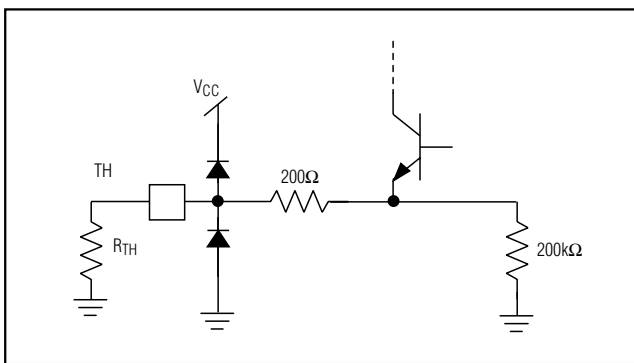


Figure 4. TH Interface

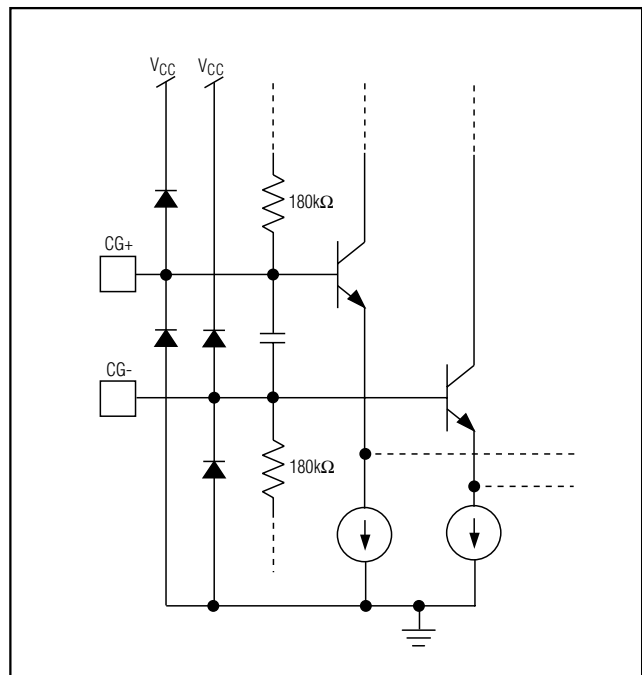


Figure 5. CG Interface

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Pad Coordinates

PAD	PAD NAME	COORDINATES (μm)
1	N.C.	47, 47
2	EN	44, 264
3	N.C.	44, 419
4	VCC	47, 582
5	IN-	43, 776
6	IN+	43, 927
7	VCC	45, 1123
8	TH	44, 1452
9	GND	47, 1672
10	CZ+	306, 1672
11	CZ-	432, 1672
12	GND	593, 1671
13	N.C.	908, 1672
14	N.C.	1034, 1672
15	CD+	1181, 1672
16	CD-	1307, 1672
17	RSSI	1461, 1672
18	GND	1662, 1671
19	SD	1669, 1458
20	VCC	1668, 1126
21	OUT+	1671, 927
22	OUT-	1671, 776
23	VCC	1668, 577
24	OSM	1669, 272
25	GND	1661, 47
26	N.C.	1356, 47
27	CG-	1207, 45
28	CG+	1081, 45
29	GND	670, 47
30	SC	513, 45
31	N.C.	355, 45
32	VREF	199, 45

Coordinates are for the center of the pad.

Coordinate 0, 0 is the lower left corner of the passivation opening for pad 1.

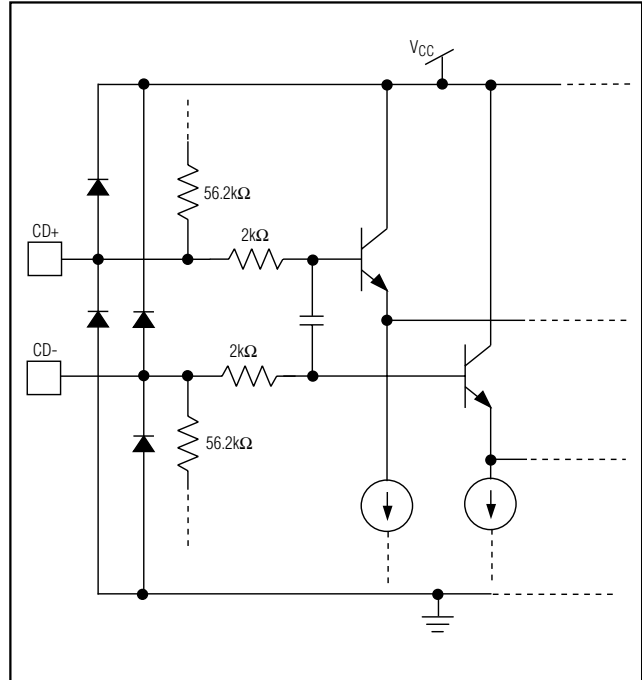


Figure 6. CD Interface

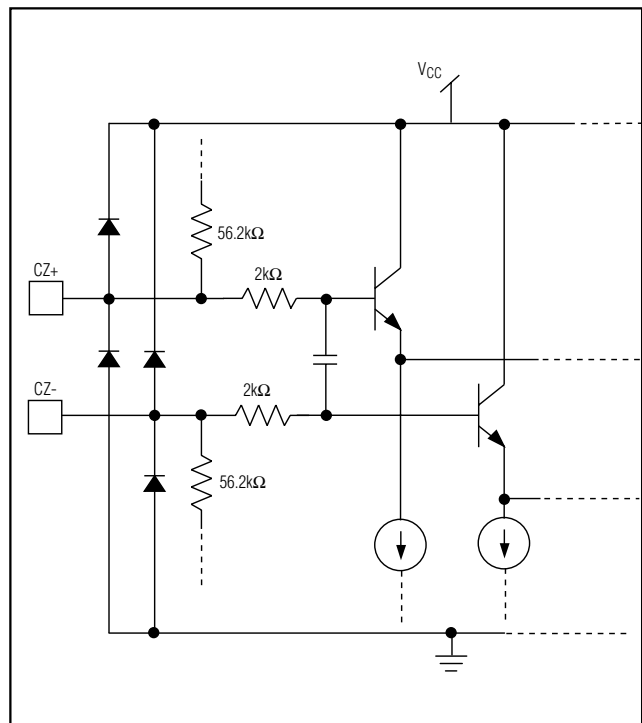
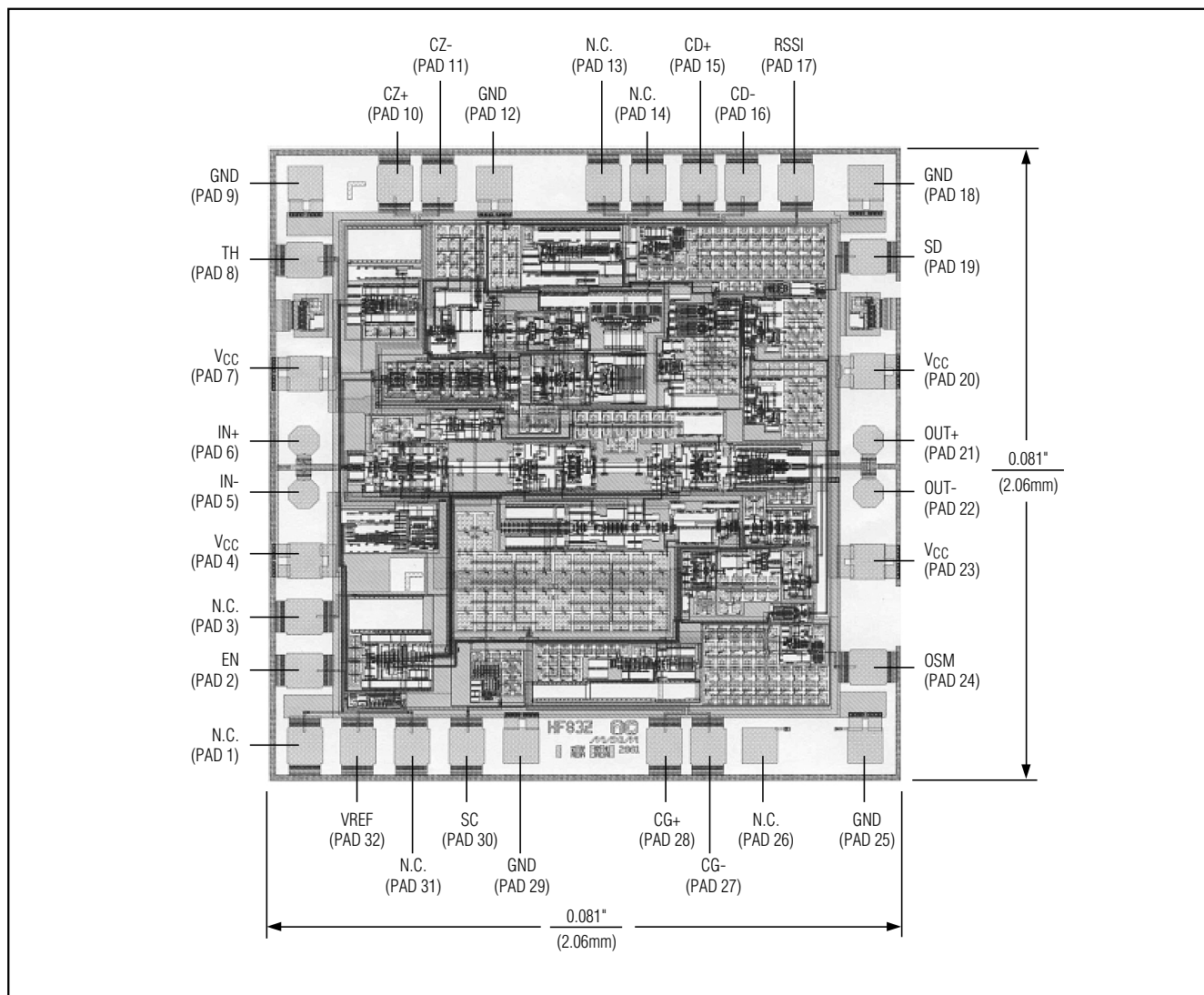


Figure 7. CZ Interface

2.7Gbps Post Amp with Automatic Gain Control

Chip Topography

MAX3861



TRANSISTOR COUNT: 952

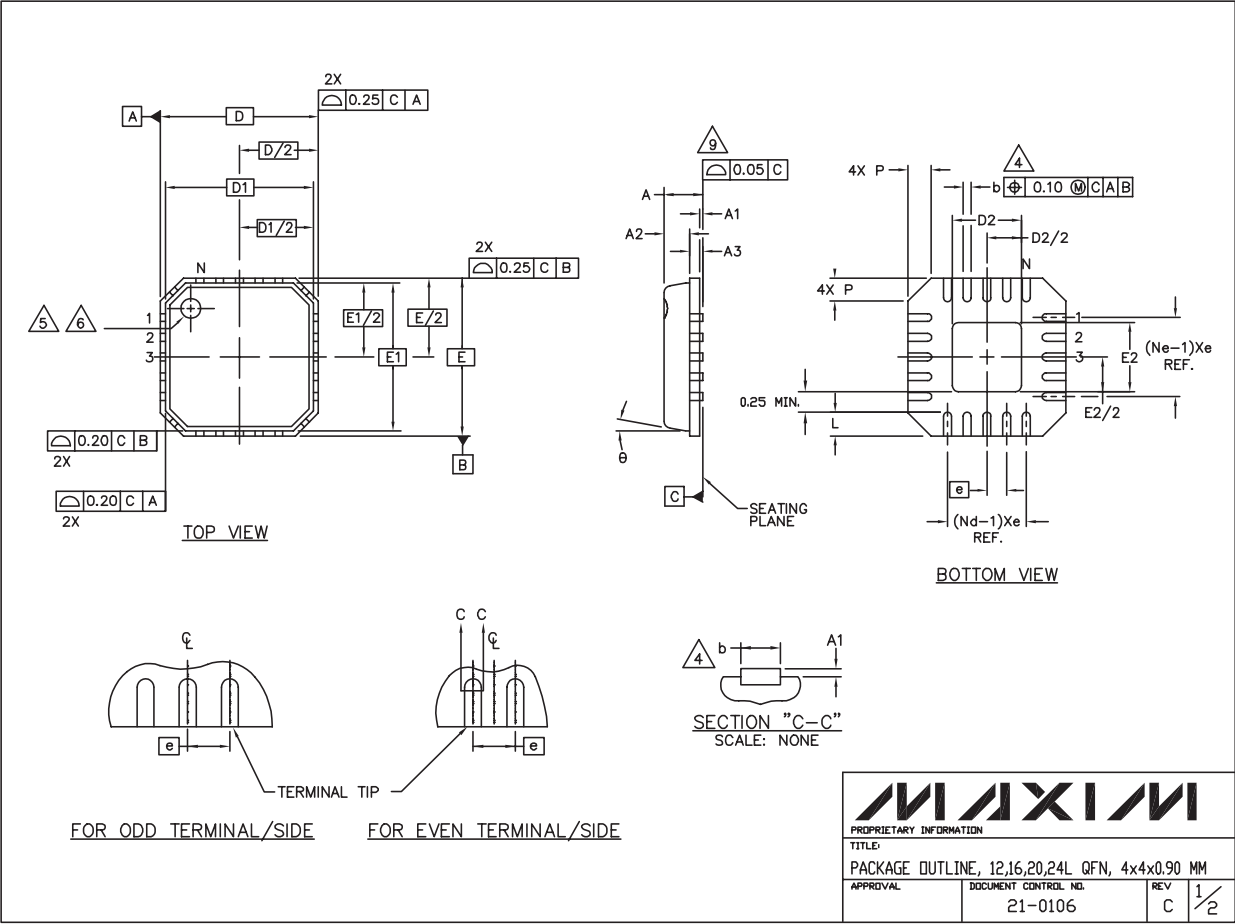
Insulated SiGe Bipolar

PROCESS: Bipolar F60

DIE SIZE: 2.06mm × 2.06mm

2.7Gbps Post Amp with Automatic Gain Control

Package Information



2.7Gbps Post Amp with Automatic Gain Control

Package Information (continued)

MAX3861

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM MUST TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES) AND TO SAW SINGULATION (STRAIGHT SIDES) QFN STYLES.

	COMMON DIMENSIONS			No. of
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	0.80	
A3	0.20 REF.			
D	4.00 BSC			
D1	3.75 BSC			
E	4.00 BSC			
E1	3.75 BSC			
θ	0°		12°	
P	0.00	0.42	0.60	
D2	0.75		2.25	
E2	0.75		2.25	

Symbol	PITCH VARIATION A			No. of	Symbol	PITCH VARIATION B			No. of	Symbol	PITCH VARIATION C			No. of	Symbol	PITCH VARIATION D			No. of
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
Ⓢ	0.80 BSC				Ⓢ	0.65 BSC				Ⓢ	0.50 BSC				Ⓢ	0.50 BSC			
N	12			3	N	16			3	N	20			3	N	24			3
Nd	3			3	Nd	4			3	Nd	5			3	Nd	6			3
Ne	3			3	Ne	4			3	Ne	5			3	Ne	6			3
L	0.50	0.60	0.75		L	0.50	0.60	0.75		L	0.50	0.60	0.75		L	0.30	0.40	0.55	
b	0.28	0.33	0.40	4	b	0.23	0.28	0.35	4	b	0.18	0.23	0.30	4	b	0.18	0.23	0.30	4

	
PROPRIETARY INFORMATION	
TITLE:	
PACKAGE OUTLINE, 12,16,20,24L QFN, 4x4x0.90 MM	
APPROVAL	DOCUMENT CONTROL NO.
	21-0106
REV	C
	2/2

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