19-2565; Rev 0; 8/02

5Gbps PC Board Equalizer

General Description

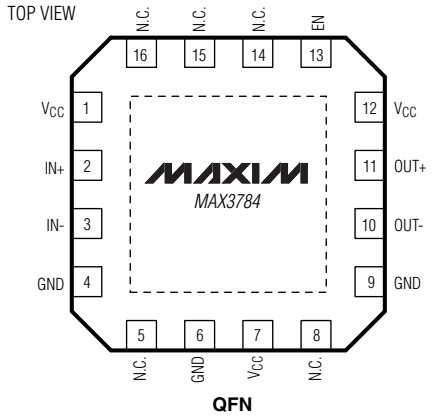
The MAX3784 5Gbps equalizer provides compensation for transmission-medium losses in up to 40in of FR4. It is optimized for short run length, balanced codes such as 8b10b, as found in multiplexed 1.25Gbps Ethernet systems.

The equalizer uses differential CML data inputs and outputs. A standby mode provides low power when the part is not in use. The MAX3784 is available in a 4mm × 4mm 16-pin QFN package that consumes only 185mW at +3.3V.

Features

- ♦ **Spans 40in (1m) of FR4 PC Board**
- ♦ **0.18UI Deterministic Jitter Up to 40in**
- ♦ **Low Power Consumption: 185mW**
- ♦ **Equalization Reduces Intersymbol Interference**
- ♦ **Single +3.3V Supply**
- ♦ **Standby Mode**
- ♦ **Small 4mm × 4mm 16-Pin QFN Package**

Pin Configuration



QFN

NOTE: THE EXPOSED PAD MUST BE SOLDERED TO SUPPLY GROUND FOR CORRECT THERMAL AND ELECTRICAL PERFORMANCE.

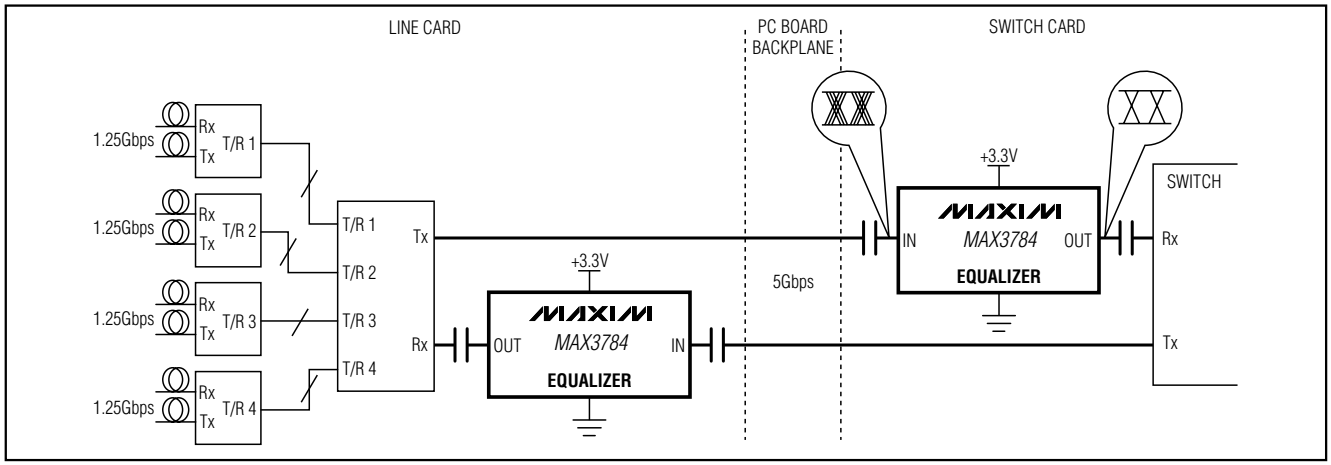
Applications

Chassis Life Extension

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3784UGE	0°C to +85°C	16 QFN

Typical Application Circuit



5Gbps PC Board Equalizer

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}.....-0.5V to +6V
Input Voltage.....(-0.5V) to (V_{CC} + 0.5V)
Continuous Output Current.....-25mA to +25mA
Continuous Power Dissipation (T_A = +85°C)
16-Pin QFN (derate 25mW/°C above +85°C) 1600mW
Operating Ambient Temperature Range .....0°C to +85°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Power		EN = low				30	mW
		EN = high			185	250	
Supply Noise Tolerance		(Note 1)	10Hz < f < 100Hz		100		mV_{P-P}
			100Hz < f < 1MHz		40		
			1MHz < f < 2.5GHz		10		
Latency		From input to output			200		ps
CML RECEIVER INPUT							
Input Voltage Swing	V_{IN}	Measured differentially at point A in Figure 1 (Note 2)		400		1000	mV_{P-P}
Return Loss		100MHz to 2.5GHz			15		dB
Input Resistance		Differential		80	100	120	Ω
EQUALIZATION							
Residual Deterministic Jitter, 5Gbps		Table 1 (Notes 2, 3, 4, 5)	20in		0.13	0.21	UI_{P-P}
			40in		0.18	0.23	
Residual Deterministic Jitter, 2.5Gbps		Table 1 (Notes 2, 3, 4, 5)	20in		0.08	0.14	UI_{P-P}
			40in		0.13	0.28	
Residual Deterministic Jitter, 1.25Gbps		Table 1 (Notes 2, 3, 4, 5)	20in		0.04	0.07	UI_{P-P}
			40in		0.07	0.15	
Random Jitter		(Notes 5, 6)			1.3	1.9	ps_{RMS}
CML TRANSMITTER OUTPUT (into 100Ω ±1Ω)							
Output Voltage Swing	V_O	Differential swing, measured differentially at point C in Figure 1		400		600	mV_{P-P}
Transition Time	t_f, t_r	20% to 80% (Notes 5, 8)		30	45	60	ps
Output Resistance		Single ended		40	50	60	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE CONTROL PIN						
Input High Voltage			1.5			V
Input Low Voltage					0.5	V
Input High Current		(Note 5)	-150		+10	µA
Input Low Current		(Note 5)	-150		+10	µA

Note 1: Allowed supply noise during jitter tests.

Note 2: Test pattern. This is a combination of K28.5± characters running at the full bit rate and at one-quarter the bit rate. This simulates the multiplexing of four each 1.25Gbps Ethernet data streams.

Pattern (hex) 100 bits

00 FFFF F0F0 FF 0000 0F0F (quarter rate K28.5+, quarter rate K28.5-)
3EB05 (K28.5± 00 1111 1010 11 0000 0101)

Note 3: Difference in deterministic jitter between reference points A and C in Figure 1.

Note 4: Signal source amplitude range is 400mV$_{P-P}$ to 1000mV$_{P-P}$, differential. Signal is applied differentially at point A as shown in Figure 1. The deterministic jitter at point B must be from media-induced loss and not from clock-source modulation. Deterministic jitter is measured at the 50% vertical level of the signal at point C.

Note 5: Guaranteed by design and characterization.

Note 6: Test pattern is K28.5 with 40in trace.

Note 7: On-chip pullup resistor of 40kΩ typical. Negative current indicates equalizer sources current.

Note 8: Using 00 0001 1111 or equivalent pattern. Measured over entire input voltage range, max and min media loss and within 2in of output pins.

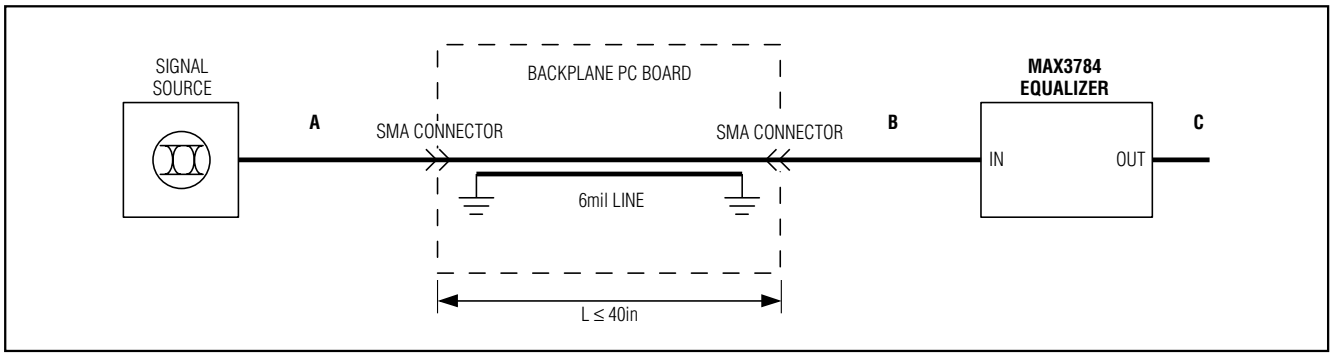


Figure 1. Test Conditions

Table 1. PC Board Assumptions (PC board material is FR4)

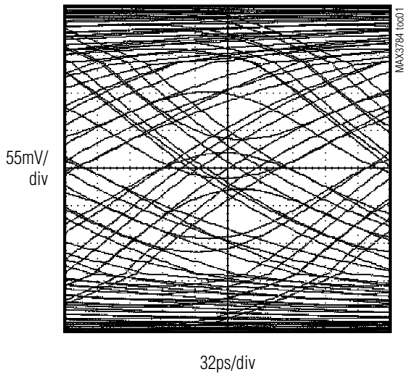
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Transmission Line	Edge-coupled stripline		6		mil
Relative Permittivity	FR4 or similar	4.4		4.5	
Loss Tangent	FR4 or similar	0.02		0.022	
Metal Thickness	0.7mil (0.5oz copper)		0.7		mil
Impedance	Differential	90	100	110	Ω

5Gbps PC Board Equalizer

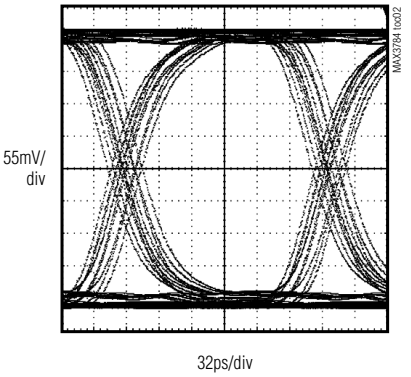
Typical Operating Characteristics

(V_{CC} = +3.3V, measurements done at 5Gbps, 800mV$_{P-P}$ board input with 100-bit pattern from Note 2 of the *EC Table*, T_A = +25°C, unless otherwise noted.)

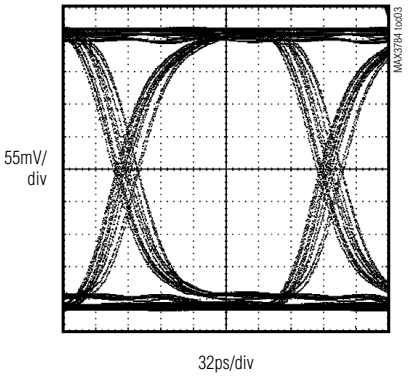
EQUALIZER INPUT EYE DIAGRAM BEFORE EQUALIZATION AT 5Gbps (40in, FR4, 6mil STRIPLINE)



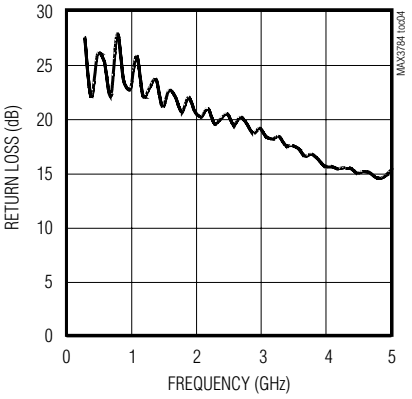
EQUALIZER OUTPUT EYE DIAGRAM AFTER EQUALIZATION AT 5Gbps (40in, FR4, 6mil STRIPLINE)



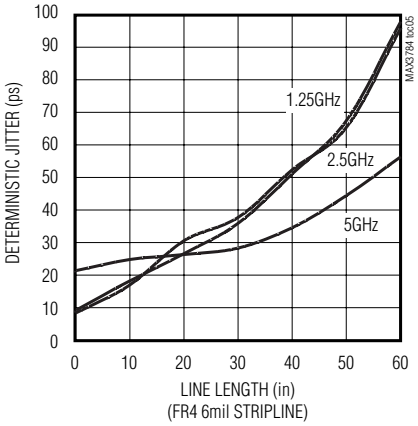
EQUALIZER OUTPUT EYE DIAGRAM AFTER EQUALIZATION AT 5Gbps (20in, FR4, 6mil STRIPLINE)



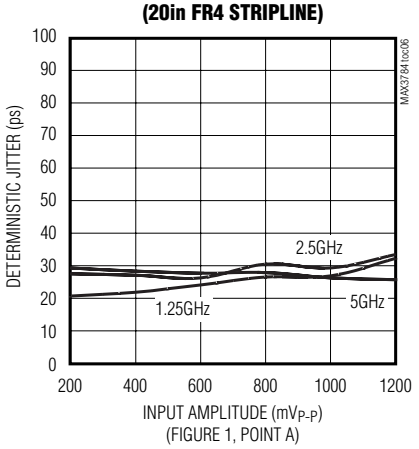
DIFFERENTIAL RETURN LOSS



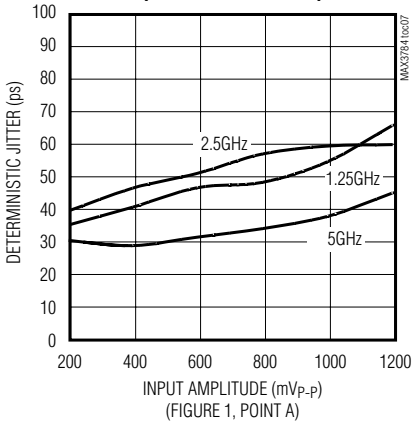
DETERMINISTIC JITTER vs. LINE LENGTH



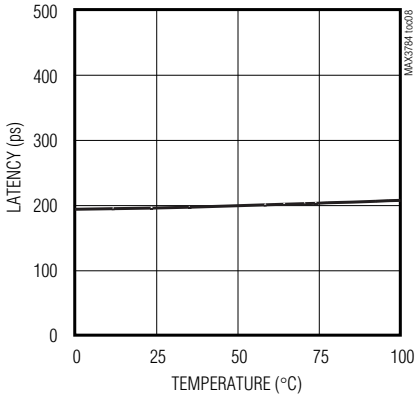
DETERMINISTIC JITTER vs. AMPLITUDE (20in FR4 STRIPLINE)



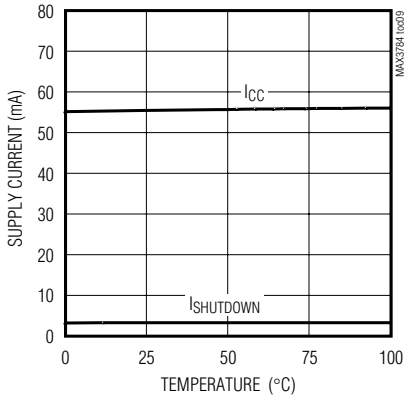
DETERMINISTIC JITTER vs. AMPLITUDE (40in FR4 STRIPLINE)



LATENCY vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1, 7, 12	V_{CC}	+3.3V Supply Voltage
2	IN+	Positive Input, CML
3	IN-	Negative Input, CML
4, 6, 9	GND	Supply Ground
5, 8, 14, 15, 16	N.C.	No Connection. Leave unconnected.
10	OUT-	Negative Output, CML
11	OUT+	Positive Output, CML
13	EN	Enable Equalizer. A logic high or open selects normal operation. A logic low selects low-power standby mode.
EP	Exposed Pad	Connect to Ground. The exposed pad must be soldered to the circuit board ground plane for proper thermal and electrical performance.

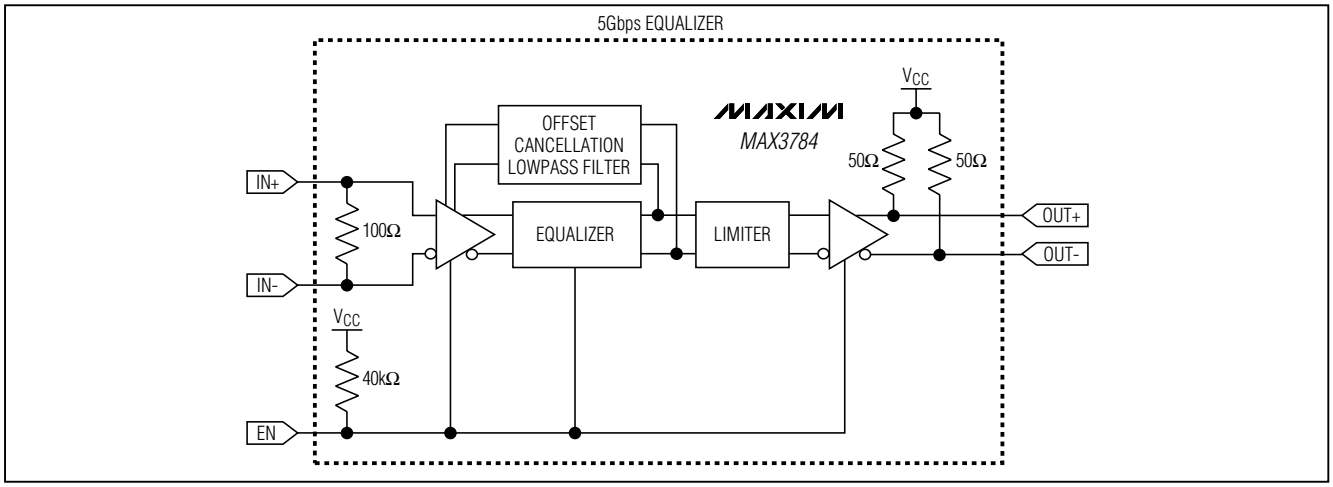


Figure 2. Functional Diagram

Detailed Description

General Theory of Operation

The MAX3784 adaptive equalizer extends the reach of transmission lines in high-frequency backplane interconnect applications. It can be used for up to 20-bit CID (coded), NRZ data operating at 5Gbps as found in 4 × 1G Ethernet (5Gbps). Internally, the MAX3784 is comprised of an equalizer control loop and limiting output driver. The equalizer reduces intersymbol interference (ISI), compensating for frequency-dependent media-induced loss. The equalization control detects the spectral contents of the input signal and provides a control voltage to the equalizer core, adapting it to different media. The equalizer operation is optimized for short-run, DC-balanced transmission codes.

Standby Mode

Standby saves power when the equalizer is not in use. The EN logic input must be set high or open for normal operation. Logic low at EN forces the equalizer into the standby state.

CML Input and Output Buffers

The input and output buffers are implemented using current-mode logic (CML). Equivalent circuits are shown in Figures 3 and 4. For details on interfacing with CML, see Maxim Application Note HFAN-1.0: *Interfacing Between CML, PECL, and LVDS*. The common-mode voltage of the input and output is above 2.5V. AC-coupling capacitors are required when interfacing this part with devices terminated in voltages such as 1.8V. Values of 0.10µF or greater are recommended.

5Gbps PC Board Equalizer

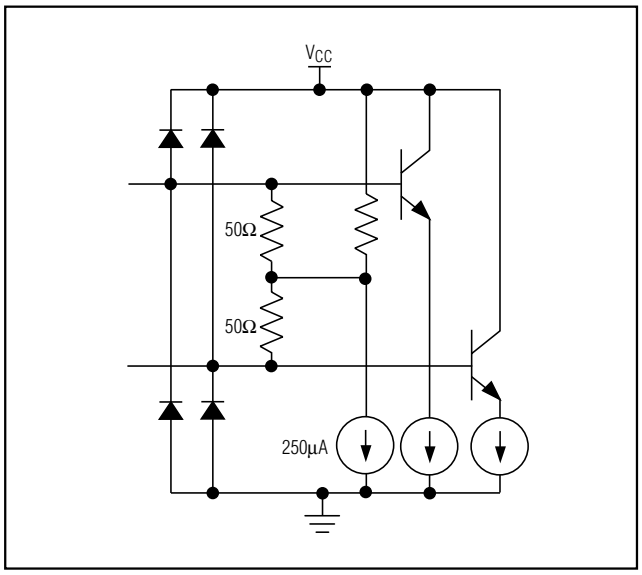


Figure 3. CML Input Equivalent Circuit

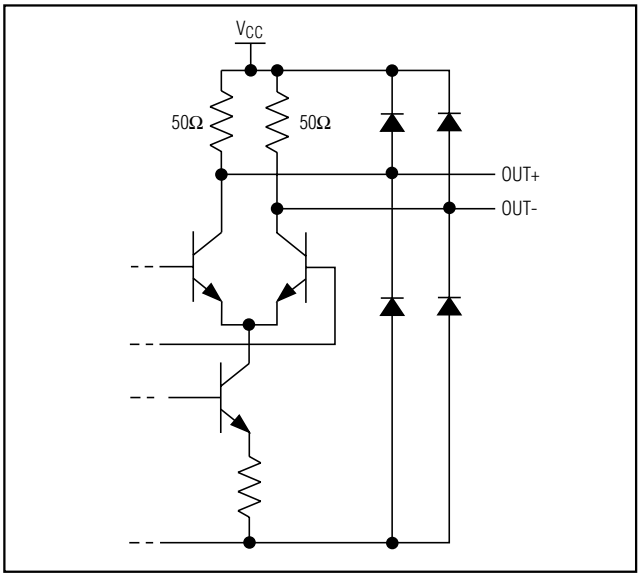


Figure 4. CML Output Equivalent Circuit

Applications Information

Alternate Data Rates

The MAX3784 is optimized for automatic operation at 5Gbps. Equalization at other data rates, such as 1.25Gbps and 2.5Gbps, is possible. See the *Typical Operating Characteristics* for Deterministic Jitter vs. Line Length and Deterministic Jitter vs. Amplitude for typical performance at these data rates.

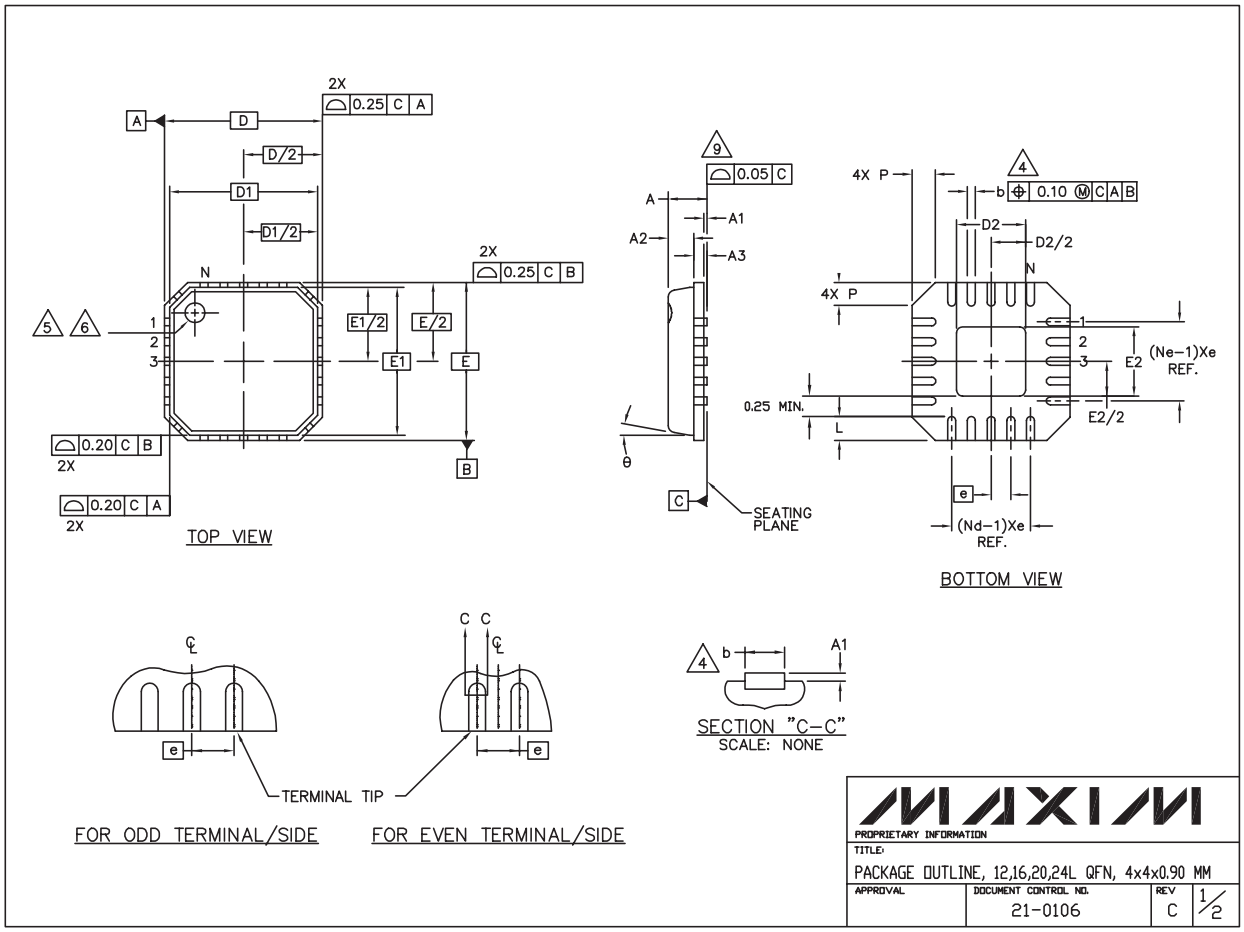
Layout Considerations

Circuit board layout and design can significantly affect the MAX3784's performance. Use good high-frequency design techniques, including minimizing ground inductance and connections and using controlled-impedance transmission lines for the high-frequency data signals. Route signals differentially to reduce EMI susceptibility and crosstalk. Solder the exposed pad to supply ground for proper thermal and electrical operation.

Place power-supply decoupling capacitors as close as possible to the V_{CC} pins.

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



5Gbps PC Board Equalizer

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM MUST TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES) AND TO SAW SINGULATION (STRAIGHT SIDES) QFN STYLES.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	0.80	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ	0°		12°	
P	0.00	0.42	0.60	
D2	0.75		2.25	
E2	0.75		2.25	

SYMBOL	PITCH VARIATION A			NOTE
	MIN.	NOM.	MAX.	
e		0.80 BSC		
N		12		3
Nd		3		3
Ne		3		3
L	0.50	0.60	0.75	
b	0.28	0.33	0.40	4

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e		0.65 BSC		
N		16		3
Nd		4		3
Ne		4		3
L	0.50	0.60	0.75	
b	0.23	0.28	0.35	4

SYMBOL	PITCH VARIATION C			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		20		3
Nd		5		3
Ne		5		3
L	0.50	0.60	0.75	
b	0.18	0.23	0.30	4

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		24		3
Nd		6		3
Ne		6		3
L	0.30	0.40	0.55	
b	0.18	0.23	0.30	4

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 12,16,20,24L QFN, 4x4x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0106	C	2/2