

RELIABILITY REPORT
FOR
MAX3286Cxx
PLASTIC ENCAPSULATED DEVICES

January 12, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

A handwritten signature in black ink, appearing to read "J Pedicord".

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

A handwritten signature in black ink, appearing to read "Bryan J. Preeshl".

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX3286 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

| | |
|-----------------------------------|--------------------------------------|
| I.Device Description | V.Quality Assurance Information |
| II.Manufacturing Information | VI.Reliability Evaluation |
| III.Packaging Information | |
| IV.Die Information |Attachments |

I. Device Description

A. General

The MAX3286 products is a high-speed laser driver for fiber optic LAN transmitters, optimized for Gigabit Ethernet applications. The device contains a bias generator, laser modulator, and comprehensive safety features. Automatic power control (APC) adjusts the laser bias current to maintain average optical power at a constant level, regardless of changes in temperature or laser properties. For lasers without a monitor photodiode, this product offers a constant-current mode. The circuit can be configured for use with conventional shortwave (780nm to 850nm) or longwave (1300nm) laser diodes, as well as vertical-cavity surface-emitting lasers (VCSELs).

The MAX3286 is optimized for operation at 1.25Gbps. The device can switch 30mA of laser modulation current at the specified data rate. Adjustable temperature compensation is provided to keep the optical extinction ratio within specifications over the operating temperature range. This device is optimized to drive lasers packaged in low-cost TO-46 headers. Deterministic jitter (DJ) for the MAX3286 is typically 22ps, allowing a 72% margin to Gigabit Ethernet DJ specifications.

These laser drivers provide extensive safety features to guarantee single-point fault tolerance. Safety features include dual enable inputs, dual shutdown circuits, and a laser-power monitor. The safety circuit detects faults that could cause dangerous light output levels. A programmable power-on reset pulse initializes the laser driver at start-up.

The MAX3286 is available in a compact, 5mm x 5mm QFN or 32-pin TQFP package.

B. Absolute Maximum Ratings

| <u>Item</u> | <u>Rating</u> |
|--|------------------------------|
| Supply Voltage, V_{CC} | -0.5V to +4.0V |
| Continuous Current at Serial Outputs (SO_, LO_ Pins) | ± 36 mA |
| Voltage at SELA, SELB, PD PImS | -0.5V to ($V_{CC} + 0.5$ V) |
| Common Mode Input Voltage (SI_, LI_ Pins) | -0.5V to ($V_{CC} + 0.5$ V) |
| Storage Temp. | -55°C to +150°C |
| Lead Temp. (10 sec.) | +300°C |
| Power Dissipation | |
| 28-Pin QFN | 2300mW |
| 32-Pin TQFP-EP | 1100mW |
| Derates above +70°C | |
| 28-Pin QFN | 28.7mW/°C |
| 32-Pin TQFP-EP | 14.3mW/°C |

II. Manufacturing Information

| | |
|----------------------------------|---|
| A. Description/Function: | 3.0V to 5.5V 1.25Gbps LAN Laser Driver |
| B. Process: | GST2 (High-Speed Double Poly-Silicon Bipolar Process) |
| C. Number of Device Transistors: | 1154 |
| D. Fabrication Location: | Oregon, USA |
| E. Assembly Location: | Korea or Malaysia |
| F. Date of Initial Production: | October, 1999 |

III. Packaging Information

| | | |
|--|--------------------------|--------------------------|
| A. Package Type: | 28-Pin QFN | 32-Pin TQFP |
| B. Lead Frame: | Copper | Copper |
| C. Lead Finish: | Solder Plate | Solder Plate |
| D. Die Attach: | Silver-filled Epoxy | Silver-filled Epoxy |
| E. Bondwire: | Gold (1.2 mil dia.) | Gold (1.2 mil dia.) |
| F. Mold Material: | Epoxy with silica filler | Epoxy with silica filler |
| G. Assembly Diagram: | # 05-7001-0442 | #05-7001-0337 |
| H. Flammability Rating: | Class UL94-V0 | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: | Level 1 | Level 1 |

IV. Die Information

| | |
|----------------------------|---|
| A. Dimensions: | 53 x 72 mils |
| B. Passivation: | Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Poly / Au |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 1.4 microns (as drawn) |
| F. Minimum Metal Spacing: | 1.4 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | SiO ₂ |
| I. Die Separation Method: | Wafer Saw |

V. Quality Assurance Information

A. Quality Assurance Contacts:

| | |
|-----------------|----------------------------|
| Jim Pedicord | (Reliability Lab Manager) |
| Bryan Preeshl | (Executive Director of QA) |
| Kenneth Huening | (Vice President) |

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 9823 \times 48 \times 2} \text{ (Chi square value for MTTF upper limit)}$$

└─ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 10.11 \times 10^{-9} \quad \lambda = 10.11 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The HF34-1 die type has been found to have all pins able to withstand a transient pulse of $\pm 500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 50\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX3286Cxx

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|-----------------------------------|---|----------------------------------|-------------|-------------|--------------------|
| Static Life Test (Note 1) | | | | | |
| | Ta = 150°C Biased Time = 192 hrs. | DC Parameters & functionality | | 48 | 0 |
| Moisture Testing (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs. | DC Parameters & functionality | TQFP QFN | 77 77 | 0 |
| 85/85 | Ta = 85°C RH = 85% Biased Time = 1000hrs. | DC Parameters & functionality | | 77 | 0 |
| Mechanical Stress (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C 1000 Cycles Method 1010 | DC Parameters | | 77 | 0 |

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic Package/Process Data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|----|---|---|
| 1. | All pins except V_{PS1} 3/ | All V_{PS1} pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.

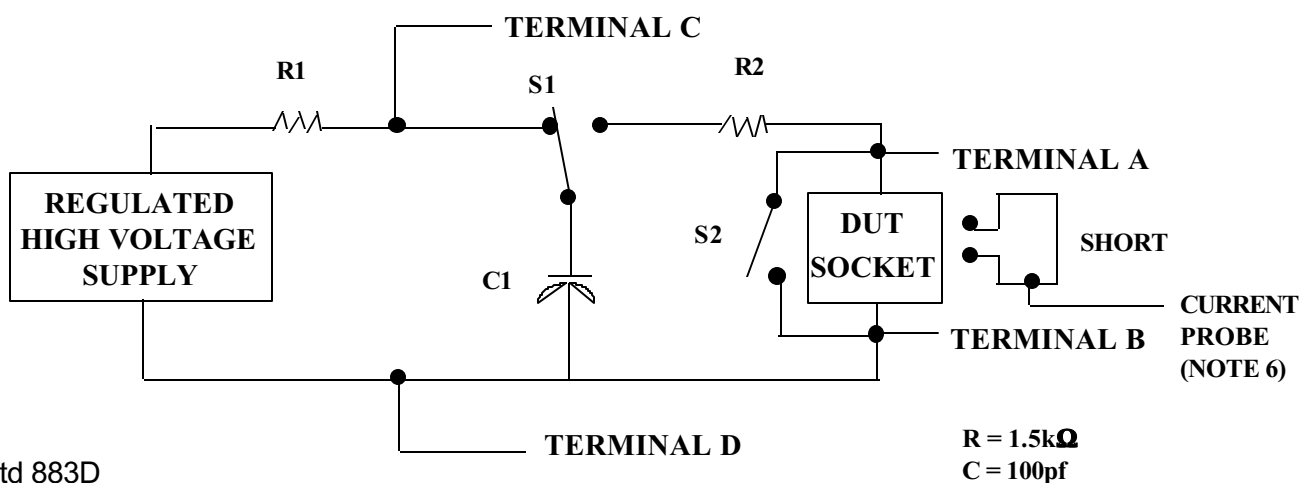
2/ No connects are not to be tested.

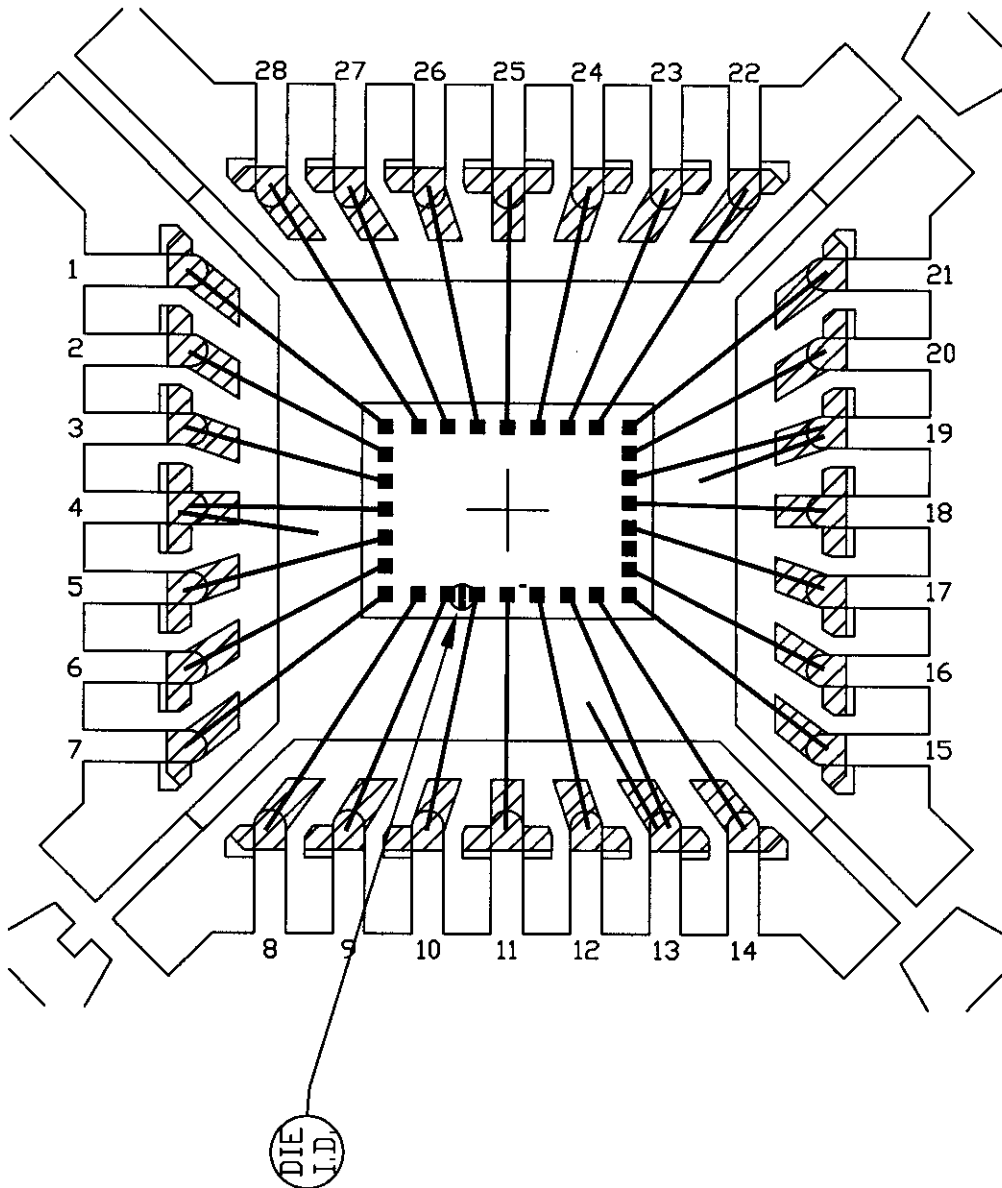
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.


- Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

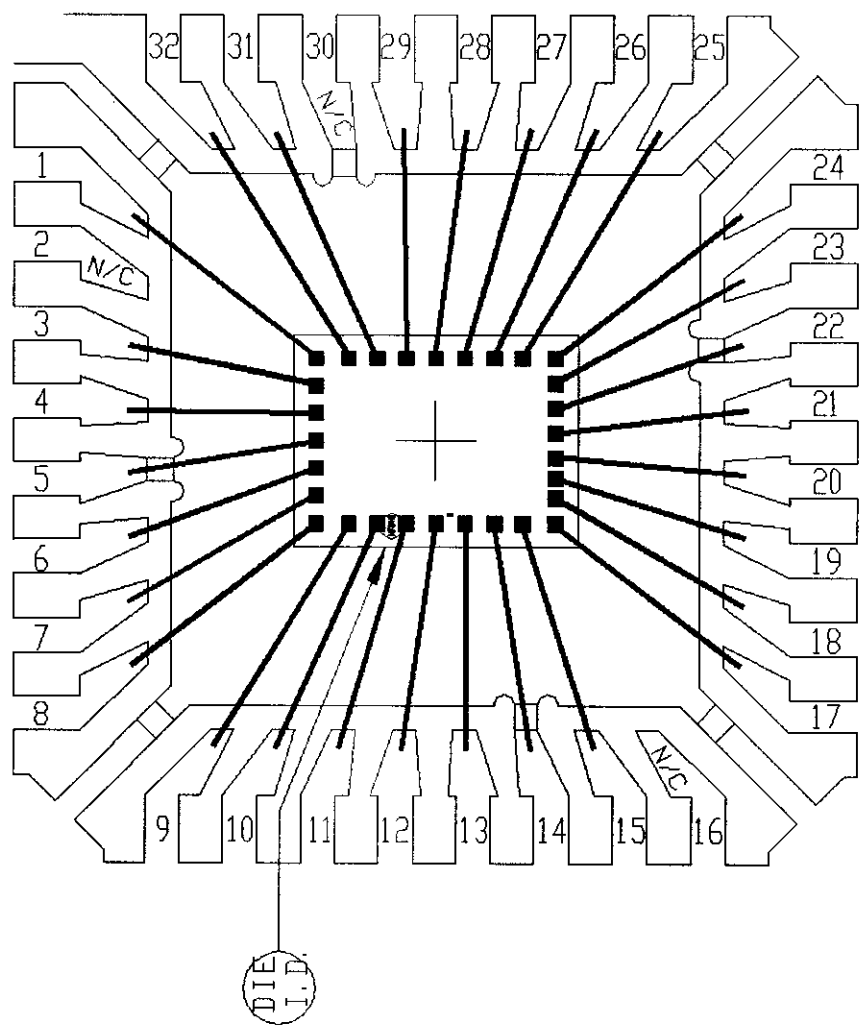




 BONDABLE AREA

PKG. BODY SIZE: 5x5 mm

| | | | | | | |
|----------------|---------|-------------|------------------------------|-------------------|---|------|
| PKG. CODE: | G2855-1 | | SIGNATURES | DATE |  CONFIDENTIAL & PROPRIETARY | |
| CAV./PAD SIZE: | 114x114 | PKG. DESIGN | <i>De Youm</i> <i>Lam</i> | 9/8/00 9/14/00 | BOND DIAGRAM #: | REV: |
| | | | | | 05-7001-0442 | C |



| | | | | | |
|------------------------|-------------|------------|---------------|---------------------------------|---------|
| PKG. CODE: H32-2F | | APPROVALS | DATE | MAXIM | |
| CAV./PAD SIZE: 133x133 | PKG. DESIGN | <i>WAX</i> | <i>6/2/99</i> | BUILDSHEET NUMBER: 05-7001-0337 | REV.: B |