



+3.3V, 2.5Gbps Low-Power Limiting Amplifier

MAX3272

General Description

The MAX3272 2.5Gbps limiting amplifier accepts a wide range of input voltages and provides a constant-level output voltage with controlled edge speeds. Additional features include power detectors with programmable loss-of-signal (LOS) indication, an optional squelch function that mutes the data output signal when the input voltage falls below a programmable threshold, and an output polarity selector. This part exhibits excellent jitter performance and has low power dissipation.

The MAX3272 features current-mode logic (CML) data outputs that are tolerant of inductive connectors, and is available in a 4mm × 4mm QFN package or in die form. Along with the MAX3271, the MAX3272 is ideal for low-power, compact optical receivers.

Applications

Gigabit Ethernet Optical Receivers
Fibre Channel Optical Receivers
System Interconnects
2.5Gbps Optical Receivers
SONET/SDH Receivers

Features

- ◆ Single +3.3V Power Supply
- ◆ 33mA Supply Current
- ◆ 5ps Deterministic Jitter
- ◆ 90ps Edge Speed
- ◆ Output Squelch Function
- ◆ Programmable Loss-of-Signal Function
- ◆ CML Output Interface
- ◆ 20-Pin 4mm × 4mm QFN Package
- ◆ Selectable Output Polarity

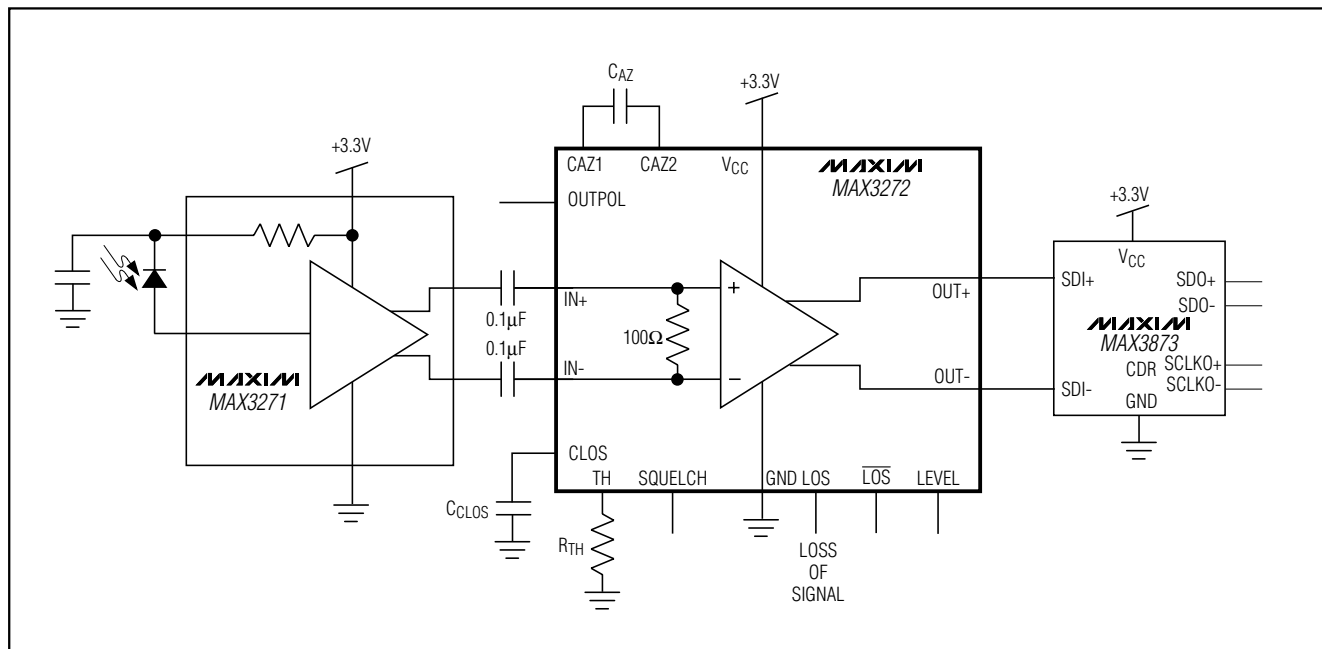
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3272EGP	-40°C to +85°C	20 QFN
MAX3272E/D	-40°C to +85°C	Dice*

*Dice are designed and guaranteed to operate from -40°C to +85°C, but are tested only at $T_A = +25^\circ\text{C}$.

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC}) -0.5V to +6.0V
 Voltage at $IN+$, $IN-$ ($V_{CC} - 2.4V$) to ($V_{CC} + 0.5V$)
 Voltage at SQUELCH, CAZ1, CAZ2, TH, CLOS -0.5V to ($V_{CC} + 0.5V$)
 Voltage at LOS, \overline{LOS} -0.5V to +6.0V
 Voltage at LEVEL -0.5V to +2.0V
 Voltage at OUTPOL -0.5V to +6.0V
 Current into LOS, \overline{LOS} -1mA to +9mA
 Differential Input Voltage ($IN+ - IN-$) 2.5VP-P
 Continuous Current at $IN+$, $IN-$ 50mA

Continuous Current at
 CML Outputs ($OUT+$, $OUT-$) -25mA to +25mA
 Continuous Power Dissipation 1600mW
 Storage Ambient Temperature
 Range (T_{STG}) -55°C to +150°C
 Operating Junction Temperature
 Range (T_J) -55°C to +150°C
 Die Attach Temperature +400°C
 Lead Temperature (soldering, 10s) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.0V$ to +3.6V, $T_A = -40^\circ C$ to +85°C. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Note 2)		33	44	mA
Input Data Rate				2.5		Gbps
Input Voltage Range	V_{IN}	Differential	15		1200	mVP-P
Output Deterministic Jitter		(Notes 3, 4, 5)		5	27	psp-p
Random Jitter		(Notes 4, 6)		3		psRMS
Data Output Edge Speed (20% to 80%)		(Notes 3, 4)		90	130	ps
		$15mVP-P \leq V_{IN} \leq 30mVP-P$ $30mVP-P < V_{IN} \leq 1200mVP-P$		90	115	
Differential Input Resistance	R_{IN}	$IN+$ to $IN-$	95	100	105	Ω
Input-Referred Noise				220		μV_{RMS}
CML Output Voltage	V_{OUT}	LEVEL open, $R_{LOAD} = 50\Omega$	550	750	1200	mVP-P
Output Signal when Squelched		Outputs AC-coupled		2.2		mVP-P
Power-Supply Noise Rejection	PSNR	$f \leq 2MHz$ (Note 7)		30		dB
Low Frequency Cutoff	f_{OC}	CAZ = open		0.9		MHz
		CAZ = 0.1 μF		1.5		kHz
Output Resistance	R_{OUT}	Single ended to V_{CC}	42.5	50	57.5	Ω
Single-Ended Output Return Loss		$\leq 2.5GHz$		10		dB
		2.5GHz to 4.0GHz		9		
Differential Input Return Loss		4.0GHz		10		dB
OUTPOL Input Limits	V_{IL}				0.8	V
	V_{IH}		2.4			
LOS Hysteresis		(Notes 3, 4, 8)	2	3.3		dB
LOS Assert/Deassert Time		$C_{CLOS} = \text{open}$ (Notes 3, 9, 10)		1		μs
		$C_{CLOS} = 0.01\mu F$ (Notes 3, 9, 10)	2.3	50	100	
Low LOS Assert Level		$R_{TH} = 20k\Omega$ (Notes 3, 10)	4.5	6.5		mVP-P
Low LOS Deassert Level		$R_{TH} = 20k\Omega$ (Notes 3, 10)		9.5	12.7	mVP-P
Medium LOS Assert Level		$R_{TH} = 1k\Omega$ (Notes 3, 10)	7.8	12.9		mVP-P
Medium LOS Deassert Level		$R_{TH} = 1k\Omega$ (Notes 3, 10)		17.4	22.4	mVP-P
High LOS Assert Level		$R_{TH} = 80\Omega$ (Notes 3, 10)	24.3	48		mVP-P

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ELECTRICAL CHARACTERISTICS (continued)

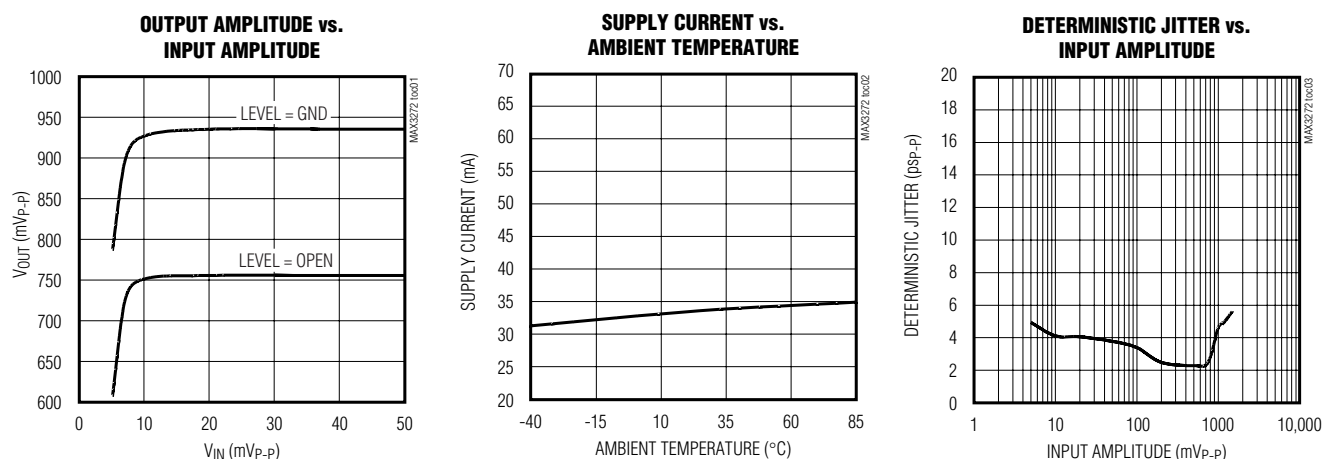
($V_{CC} = +3.0V$ to $+3.6V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^{\circ}C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High LOS Deassert Level		$R_{TH} = 80\Omega$ (Notes 3, 10)		73	124.7	mV _{P-P}
LOS Output High Voltage		Sinking $30\mu A$	2.4			V
LOS Output Low Voltage		Sourcing $1.2mA$			0.4	V
Squelch Input Current					400	μA

- Note 1:** Dice are designed and guaranteed from $-40^{\circ}C$ to $+85^{\circ}C$ but are tested only at $T_A = +25^{\circ}C$.
- Note 2:** Supply current measurement excludes the current of the CML output stage ($16mA$ typical). See Figure 1, *Power-Supply Current Measurement*.
- Note 3:** Guaranteed by design and characterization.
- Note 4:** Input edge speed is controlled using 4-pole, lowpass Bessel filters with bandwidth approximately 75% of the maximum data rate.
- Note 5:** Deterministic jitter is measured with a K28.5 pattern (0011 1110 1011 0000 0101). Deterministic jitter is the peak-to-peak deviation from ideal time crossings, measured at the zero-level crossings of the differential output per ANSI X3.230, Annex A.
- Note 6:** Random jitter is measured with the minimum input signal. For Fibre Channel and Gigabit Ethernet applications, the peak-to-peak random jitter is 14.1 times the RMS random jitter.
- Note 7:** Power-supply noise rejection (PSNR) is calculated by the equation $PSNR = 20\log(\Delta V_{CC}/(\Delta V_{OUT}))$, where ΔV_{OUT} is the change in differential output voltage due to the power-supply noise, ΔV_{CC} . See Power-Supply Noise Rejection vs. Frequency in *Typical Operating Characteristics*.
- Note 8:** Hysteresis is defined as: $20 \times \log(V_{LOS-DEASSERT}/V_{LOS-ASSERT})$.
- Note 9:** Response time to a 10dB change in input power. For the specification guaranteed, the power is assumed to switch back and forth between two levels (separated by 10dB and equidistant from assert and deassert levels) outside of the two hysteresis thresholds.
- Note 10:** All power-detect AC parameters are guaranteed with a $2^{23} - 1$ PRBS, 2.5Gbps input, with the longest possible run of 80CID.

Typical Operating Characteristics

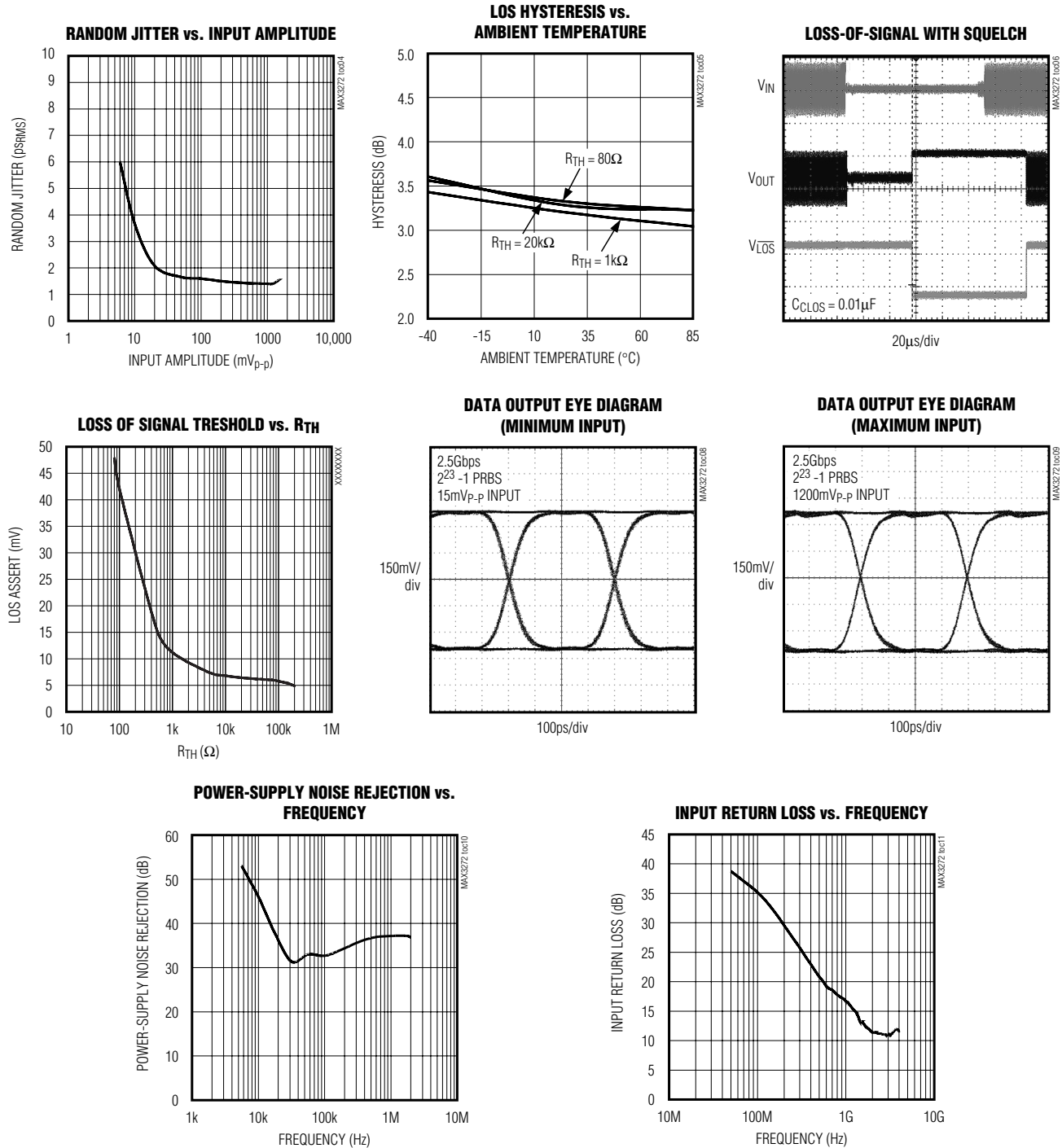
($V_{CC} = +3.3V$, $T_A = +25^{\circ}C$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

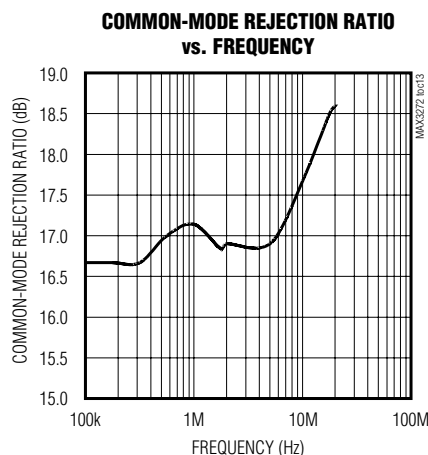
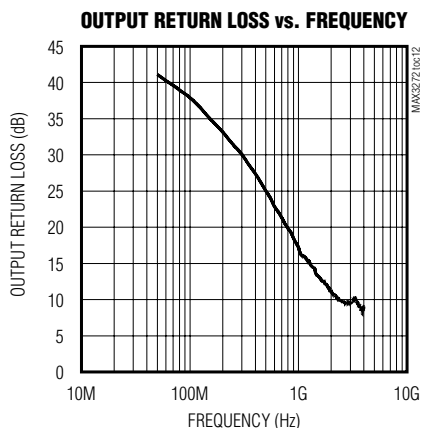
($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1, 4, 17	GND	Supply Ground
2	IN+	Noninverted Input Signal
3	IN-	Inverted Input Signal
5	TH	Loss-of-Signal Threshold Pin. Resistor to ground sets the LOS threshold.
6, 12, 15, 20	VCC	Power Supply
7	CLOS	LOS Time-Constant Capacitor Connection. For SONET applications, $C_{CLOS} = 0.01\mu F$ is recommended.
8	SQUELCH	Squelch Input. The squelch function is disabled when SQUELCH is not connected or set to TTL low level. When SQUELCH is set to TTL high level and LOS is asserted, the data outputs (OUT+, OUT-) are forced to static levels.
9	LOS	Noninverted Loss-of-Signal Output. LOS is asserted TTL high when the signal drops below the assert threshold set by the TH input.
10	\overline{LOS}	Inverted Loss-of-Signal Output. LOS is asserted TTL low when the signal drops below the assert threshold set by the TH input.
11	LEVEL	Output Current Level. When this pin is not connected, the CML output current is approximately 16mA. When this pin is connected to ground, the output current increases to about 20mA.
13	OUT-	Inverted Data Output
14	OUT+	Noninverted Data Output
16	OUTPOL	Output Polarity Control Input. Connect to GND for an inversion of polarity through the limiting amplifier and connect to V_{CC} for normal operation.
18	CAZ2	Offset-Correction-Loop Capacitor Connection. A capacitor connected between this pin and CAZ1 extends the time constant of the offset correction loop. Typical value of C_{AZ} is $0.1\mu F$.
19	CAZ1	Offset-Correction-Loop Capacitor Connection. A capacitor connected between this pin and CAZ2 extends the time constant of the offset correction loop. Typical value of C_{AZ} is $0.1\mu F$.
CP	CORNER PINS	Maxim recommends connecting the four corner pins to board ground. The four corner pins are internally connected to the exposed paddle.
EP	EXPOSED PADDLE	Connect the exposed paddle to board ground for optimal electrical and thermal performance.

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Interface Schematics

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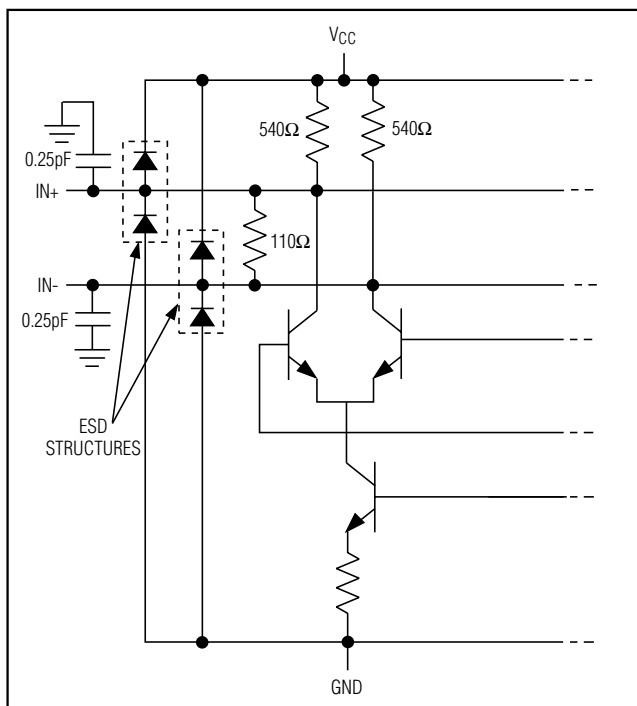


Figure 3. Input Circuit

Two control voltages V_{ASSERT} and V_{DEASSERT} define the LOS assert and deassert levels. To prevent LOS chatter in the region of the programmed threshold, approximately 3.3dB of hysteresis is built into the LOS assert/deassert function. Once asserted, LOS is not deasserted until the input amplitude rises to the required level (V_{DEASSERT}).

Gain Stage

The high-bandwidth gain stage provides approximately 42dB of gain.

Offset-Correction Loop

Due to the high gain of the amplifier, the MAX3272 is susceptible to DC offsets in the signal path. In communications systems using NRZ data with a 50% duty cycle, pulse-width distortion present in the signal or generated by the transimpedance amplifier appears as input offset and is removed by the offset-cancellation loop. An external capacitor is required between CAZ1 and CAZ2 to decouple the offset-cancellation loop and determine the lower 3dB frequency of the signal path.

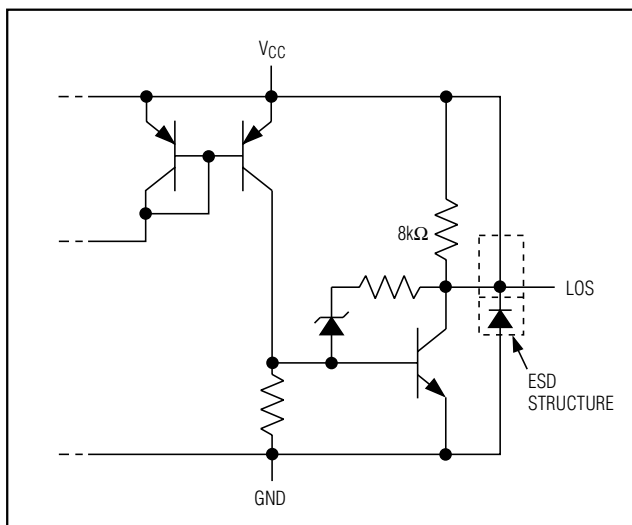


Figure 4. LOS Output Circuit

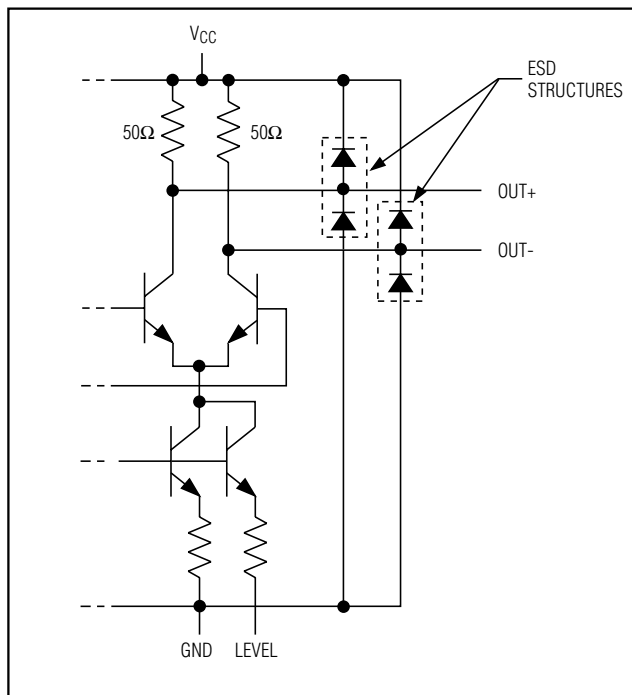


Figure 5. CML Output Circuit

CML Output Buffer

The MAX3272 CML output circuit (Figure 5) provides high tolerance to impedance mismatches and inductive connectors. The output current can be set to two levels

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using the LEVEL pin. When LEVEL is unconnected, the output current is approximately 16mA. Connecting LEVEL to ground sets the output current to approximately 20mA. The squelch function is enabled when the SQUELCH pin is set to a TTL high. This function holds OUT+ and OUT- to a static level whenever the input signal amplitude drops below the loss-of-signal threshold. This circuit is also equipped with a polarity selector, programmed by the OUTPOL pin. When this pin is connected to V_{CC}, no inversion will occur. When connected to ground, the output signal will be inverted.

Design Procedure

Program the LOS Assert Threshold

External resistor R_{TH} programs the loss-of-signal threshold. See the LOS Threshold vs. R_{TH} graph in the *Typical Operating Characteristics* section to select the appropriate resistor.

Select the Coupling Capacitors

When AC-coupling, input and output coupling capacitors (C_{IN} and C_{OUT}) should be selected to minimize the receiver's deterministic jitter. Jitter is decreased as the input low-frequency cutoff (f_{IN}) is decreased:

$$f_{IN} = 1 / [2\pi(50)(C_{IN})]$$

For ATM/SONET or other applications using scrambled NRZ data, select (C_{IN}, C_{OUT}) ≥ 0.1μF, which provides f_{IN} < 32kHz. For Fibre Channel, Gigabit Ethernet, or other applications using 8B/10B data coding, select (C_{IN}, C_{OUT}) ≥ 0.01μF, which provides f_{IN} < 320kHz. Refer to application note HFAN-1.1, *Choosing AC-Coupling Capacitors*.

Select the Offset-Correction Capacitor

The capacitor between CAZ1 and CAZ2 determines the time constant of the signal path DC offset-cancellation loop. To maintain stability, it is important to keep a one-decade separation between f_{IN} and the low-frequency cutoff (f_{OC}) associated with the DC offset-cancellation circuit. For ATM/SONET or other applications using scrambled NRZ data, f_{IN} < 32kHz, so f_{OC}MAX < 3.2kHz. Therefore, CAZ = 0.1μF (f_{OC} = 2kHz). For Fibre Channel or Gigabit Ethernet applications, leave pins CAZ1 and CAZ2 open.

Program the LOS Time Constant

External capacitor C_{CLOS} programs the LOS assert and deassert times. When inputting data with many consecutive identical digits (CIDs), a longer time constant may be advantageous, so LOS does not flag incorrectly. In this case, connect the CLOS pin to a 0.01μF capacitor to set the assert time in the range of

2μs to 100μs. For scrambled data where the mark density is kept at 50%, a shorter time constant may be desirable. Leave the CLOS pin open for a shorter time constant of about 1μs.

Applications Information

Optical Hysteresis

In an optical receiver, the electrical power change at the limiting amplifier is 2 times the optical power change.

As an example, if a receiver's optical input power (x) increases by a factor of two, and the preamplifier is linear, then the voltage input to the limiting amplifier also increases by a factor of two.

The optical power change is 10log(2x/x) = 10log(2) = +3dB.

At the limiting amplifier, the electrical power change is:

$$10\log \frac{(2V_{IN})^2 / R_{IN}}{V_{IN}^2 / R_{IN}} = 10\log(2^2) = 20\log(2) = +6\text{dB}$$

The MAX3272 typical voltage hysteresis is 3.3dB. This provides an optical hysteresis of 1.65dB.

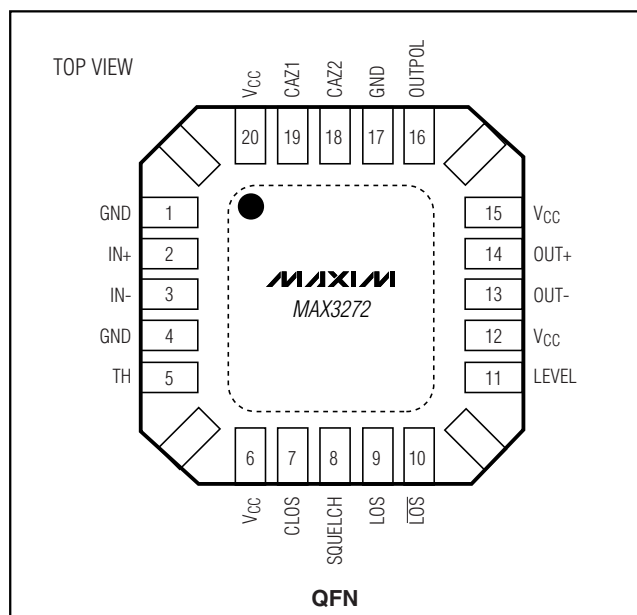
Wire Bonding Die

For high-current density and reliable operation, the MAX3272 uses gold metallization. Make connections to the dice with gold wire only, and use ball-bonding techniques (wedge bonding is not recommended). Die pad dimensions are 94.4 microns by 94.4 microns. Die thickness is 15mils (0.375mm).

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Pin Configuration



Pad Coordinates

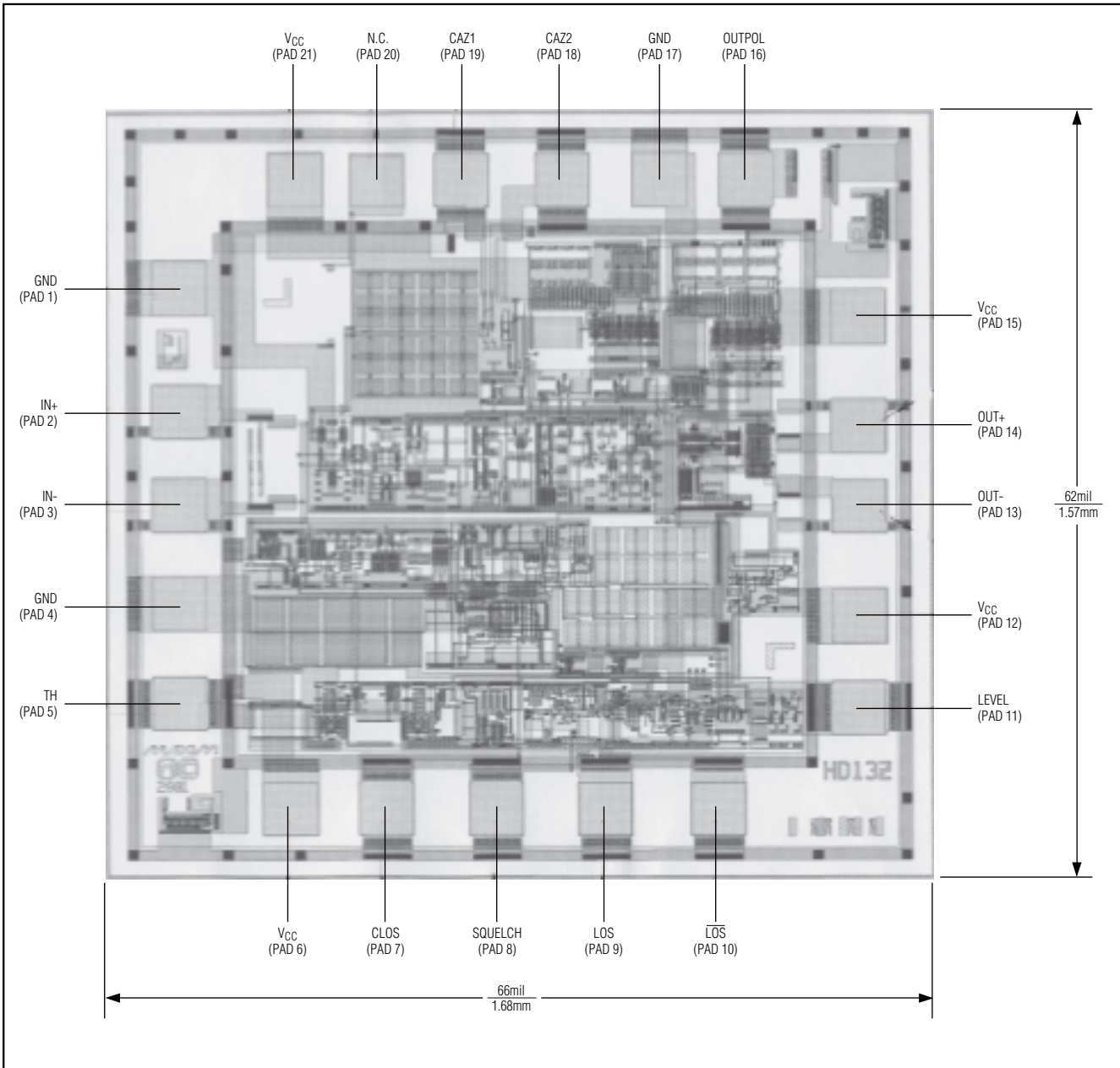
PAD#	PAD NAME	COORDINATES (μm)
1	GND	47, 836
2	IN+	47, 603
3	IN-	47, 425
4	GND	47, 237
5	TH	47, 47
6	VCC	255, -154
7	CLOS	436, -154
8	SQUELCH	645, -154
9	LOS	850, -154
10	LOS	1063, -154
11	LEVEL	1331, 37
12	VCC	1331, 212
13	OUT-	1331, 421
14	OUT+	1331, 573
15	VCC	1331, 780
16	OUTPOL	1119, 1042
17	GND	957, 1042
18	CAZ2	773, 1042
19	CAZ1	583, 1042
20	N.C.	422, 1042
21	VCC	268, 1042

Coordinates are for the center of the pad.

Coordinate 0, 0 is the lower left corner of the passivation opening for pad 5.

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Chip Information



TRANSISTOR COUNT: 726

SUBSTRATE: Isolated

PROCESS: SiGe Bipolar

DIE SIZE: 1.68mm × 1.57mm

MAX3272

12, 16, 20, 24L QFN.EPS



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Package Information (continued)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM MUST TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.
12. MEETS JEDEC M0220.

SYMBOL	COMMON DIMENSIONS			No. of Terminals
	MIN.	NOM.	MAX.	
A	—	0.85	1.00	11
A1	0.00	0.01	0.05	
A2	—	0.65	0.80	
A3	—	0.20 REF.	—	
D	—	4.00 BSC	—	
D1	—	3.75 BSC	—	
E	—	4.00 BSC	—	
E1	—	3.75 BSC	—	
θ	—	—	12°	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	

SYMBOL	PITCH VARIATION A			NO. OF TERMINALS	SYMBOL	PITCH VARIATION B			NO. OF TERMINALS	SYMBOL	PITCH VARIATION C			NO. OF TERMINALS	SYMBOL	PITCH VARIATION D			NO. OF TERMINALS
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
Ⓐ	0.80 BSC			3	Ⓐ	0.65 BSC			3	Ⓐ	0.50 BSC			3	Ⓐ	0.50 BSC			3
N	12				N	16				N	20				N	24			
Nd	3				Nd	4				Nd	5				Nd	6			
Ne	3				Ne	4				Ne	5				Ne	6			
L	0.50	0.60	0.75	4	L	0.50	0.60	0.75	4	L	0.50	0.60	0.75	4	L	0.30	0.40	0.55	4
b	0.28	0.33	0.40		b	0.23	0.28	0.35		b	0.18	0.23	0.30		b	0.18	0.23	0.30	
Q	0.30	0.40	0.65		Q	0.30	0.40	0.65		Q	0.30	0.40	0.65		Q	0.00	0.20	0.45	
D2	SEE EXPOSED PAD VARIATION: A, B				D2	SEE EXPOSED PAD VARIATION: A, B				D2	SEE EXPOSED PAD VARIATION: A, B				D2	SEE EXPOSED PAD VARIATION: A, B			
E2	SEE EXPOSED PAD VARIATION: A, B				E2	SEE EXPOSED PAD VARIATION: A, B				E2	SEE EXPOSED PAD VARIATION: A, B				E2	SEE EXPOSED PAD VARIATION: A, B			

SYMBOLS	D2			E2			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD VARIATIONS	A	1.95	2.10	2.25	1.95	2.10	2.25
	B	1.55	1.70	1.85	1.55	1.70	1.85

EXAMPLE: WE CAN CALL VARIATION "BB" FOR 16 TERMINAL QFN WITH 1.70x1.70 mm NOMINAL EXPOSED PAD DIMENSION. THE FORMER ONE IN VARIATION IS FOR PITCH VARIATION AND THE LATTER ONE IS FOR EXPOSED PAD VARIATION.

MAXIM			
PROPRIETARY INFORMATION			
TITLE:			
PACKAGE OUTLINE, 12,16,20,24L QFN, 4x4x0.90 MM			
APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0106	B	2/2

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