MAX3185xxP Rev. A

**RELIABILITY REPORT** 

FOR

# MAX3185xxP

PLASTIC ENCAPSULATED DEVICES

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## MAXIM INTEGRATED PRODUCTS

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#### Conclusion

The MAX3185 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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#### I. Device Description

A. General

The MAX3185 is a complete DTE RS-232 serial port designed to meet the stringent ESD requirements of the European community. All transmitter outputs and receiver inputs are protected to ±15kV using IEC 1000-4-2 Air-Gap Discharge, ±8kV using IEC 1000-4-2 Contact Discharge, and ±15kV using the Human Body Model.

The MAX3185 has three RS-232 transmitters, five RS-232 receivers, and no charge pump, optimizing it for operation in desktop PC and motherboard applications. It is guaranteed to run at data rates up to 230kbps, providing compatibility with popular software for communicating with personal computers. Power-supply current is less than  $300\mu A$  for  $I_{DD}$  and  $I_{SS}$ , and less than 1mA for  $I_{CC}$ .

The MAX3185 is pin and functionally compatible with the industry standard 75185, so existing designs can instantly become EMC compliant.

#### B. Absolute Maximum Ratings

ltem	Rating
V <sub>cc</sub>	-0.3V to +7V
V <sub>DD</sub>	-0.3V to +14V
V <sub>SS</sub>	+0.3V to -14V
Input Voltages	
T <sub>IN</sub>	-0.3V to +6V
R <sub>IN</sub>	±30V
Output Voltages	
T <sub>OUT</sub>	±15kV
R <sub>out</sub>	-0.3V to (V <sub>cc</sub> + 0.3V)
Short-Circuit Duration	
T <sub>OUT</sub> (one at a time)	Continuous
R <sub>out</sub> (one at a time)	Continuous
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
20 Lead SO	800mW
20 Lead SSOP	640mW
Derates above +70°C	
20 Lead SO	10mW/°C
20 Lead SSOP	8mW/°C

#### **II. Manufacturing Information**

- A. Description/Function: ±15kV ESD-Protected, EMC-Compliant, 230kbps RS-232 Serial Port for Motherboards/Desktop PCs
- B. Process: M5 (5 micron metal gate CMOS)
- C. Number of Device Transistors: 217
- D. Fabrication Location: California, USA
- E. Assembly Location: Philippines, Malaysia, or Thailand
- F. Date of Initial Production: September, 1996

#### **III.** Packaging Information

A. Package Type:	20 Lead SO	20 Lead SSOP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1901-0143	05-1901-0142
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
<ol> <li>Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:</li> </ol>	Level 1	Level 1

#### **IV. Die Information**

- A. Dimensions: 94 x 178 mils
- B. Passivation: Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 5 microns (as drawn)
- F. Minimum Metal Spacing: 5 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric: SiO<sub>2</sub>
- I. Die Separation Method: Wafer Saw

#### V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Relaibility Lab Manager) Bryan Preeshl (Executive Director) Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

 $\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{1.83}_{192 \text{ x } 4389 \text{ x } 320 \text{ x } 2} \text{ (Chi square value for MTTF upper limit)}$  Temperature Acceleration factor assuming an activation energy of 0.8eV  $\lambda = 3.39 \text{ x } 10^{-9}$ 

 $\lambda$  = 3.39 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5213) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1J**).

## B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

## C. E.S.D. and Latch-Up Testing

The RS42Z die type has been found to have all pins able to withstand a transient pulse of  $\pm$  1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm$ 250mA and/or  $\pm$ 20V.

# Table 1Reliability Evaluation Test ResultsMAX3185xxP

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	t (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		320	0
Moisture Testi	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	SO SSOP	80 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality (generic test vehicle)		77	0
Mechanical Str	ress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic package/process data.

## Attachment #1

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V <sub>PS1</sub> <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

# TABLE II. Pin combination to be tested. 1/2/

- 1/ Table II is restated in narrative form in 3.4 below.
- $\overline{2/}$  No connects are not to be tested.
- $\overline{\underline{3/}}$  Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_{S}$ ,  $-V_{S}$ ,  $V_{REF}$ , etc).

- 3.4 <u>Pin combinations to be tested.</u>
  - a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
  - b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V<sub>SS1</sub>, or V<sub>SS2</sub> or V<sub>SS3</sub> or V<sub>CC1</sub>, or V<sub>CC2</sub>) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





