RELIABILITY REPORT

FOR

MAX3095xxE

PLASTIC ENCAPSULATED DEVICES

January 28, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX3095 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3095 is a rugged, low-power, quad, RS-422/RS-485 receiver with electrostatic discharge (ESD) protection for use in harsh environments. All receiver inputs are protected to ±15kV using IEC 1000-4-2 Air-Gap Discharge, ±8kV using IEC 1000-4-2 Contact Discharge, and ±15kV using the Human Body Model. The MAX3095 operates from a +5V supply. Receiver propagation delays are guaranteed to within ±8ns of a pre-determined value, thereby ensuring device-to-device matching across production lots.

Complementary enable inputs can be used to place this device in a 1nA low-power shutdown mode in which the receiver outputs are high impedance. When active, these receivers have a fail-safe feature that guarantees a logic-high output if the input is open circuit. The MAX3095 also features a quarter-unit-load input impedance that allows 128 receivers on a bus.

The MAX3095 is a pin-compatible, low-power upgrade to the industry-standard '26LS32.

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage (V_{CC})	7V
Control Input Voltage (G, /G)	-0.3V to (V_{CC} + 0.3V)
Receiver Input Voltage (A_, B_)	±25V
Receiver Output Voltage (Y_)	-0.3V to (V_{CC} + 0.3V)
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin NSO	696mW
16-Pin PDIP	762mW
16-Pin QSOP	667mW
Derates above +70°C	
16-Pin NSO	8.7mW/°C
16-Pin PDIP	10.5mW/°C
16-Pin QSOP	8.3mW/°C

II. Manufacturing Information

A. Description/Function:	±15kV ESD-Protected, 10Mbps, 5V, Quad RS-422/RS-485 Receivers
B. Process:	S3 - Standard 3 micron silicon gate CMOS
C. Number of Device Transistors:	676
D. Fabrication Location:	Oregon or California, USA
E. Assembly Location:	Philippines, Malaysia, or Thailand
F. Date of Initial Production:	January, 1998

III. Packaging Information

	16 Lead NSO	**16-Lead PDIP**	**16-Lead QSOP**
A. Package Type:			
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1901-0166	# 05-1901-0165	# 05-1901-0167
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	85 X 129 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-9}$ $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5286) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The RS56 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX3095xxE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP NSO QSOP	260 1035 140	0 2 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the uMax package.
Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

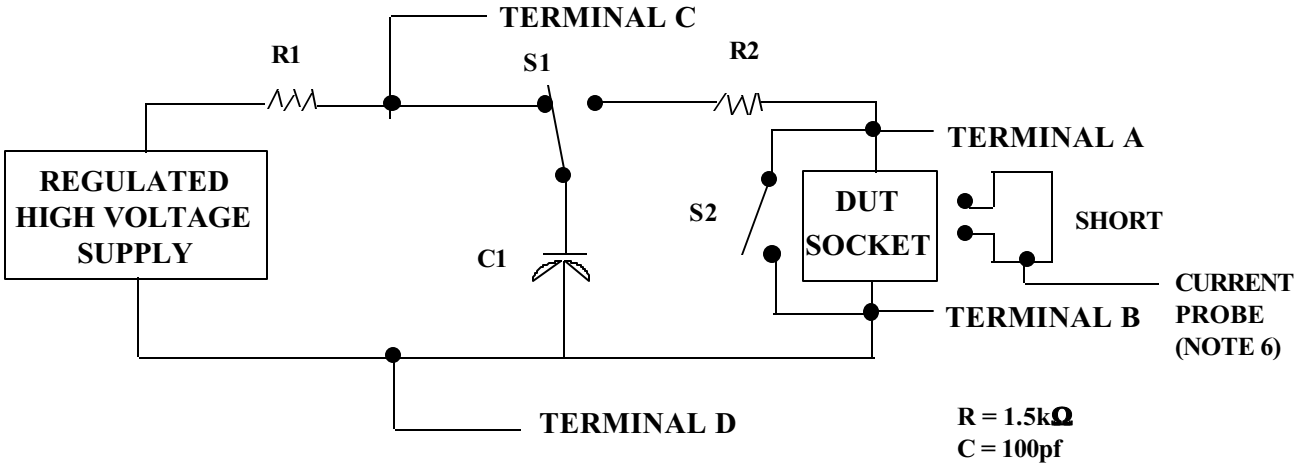
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

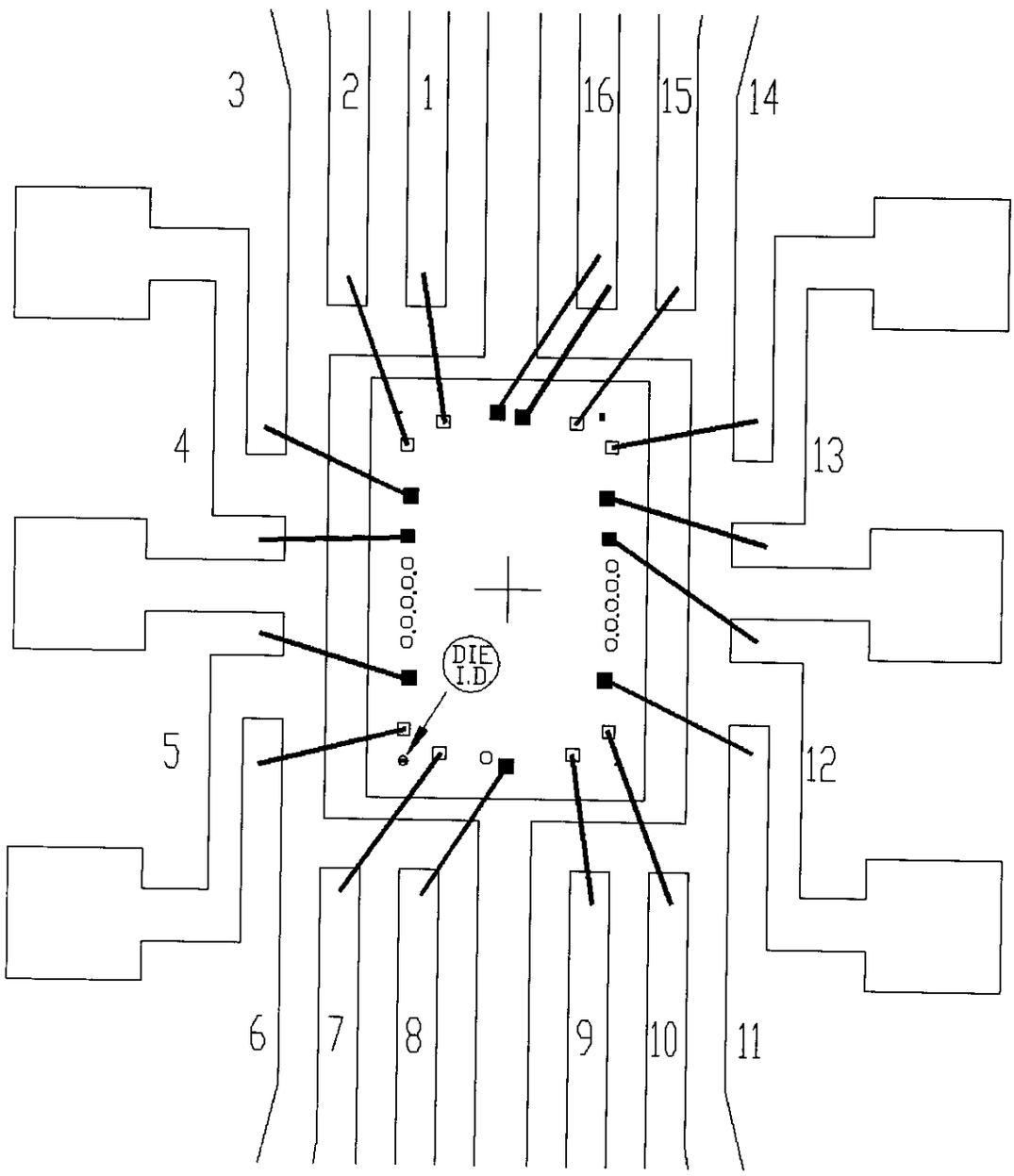
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

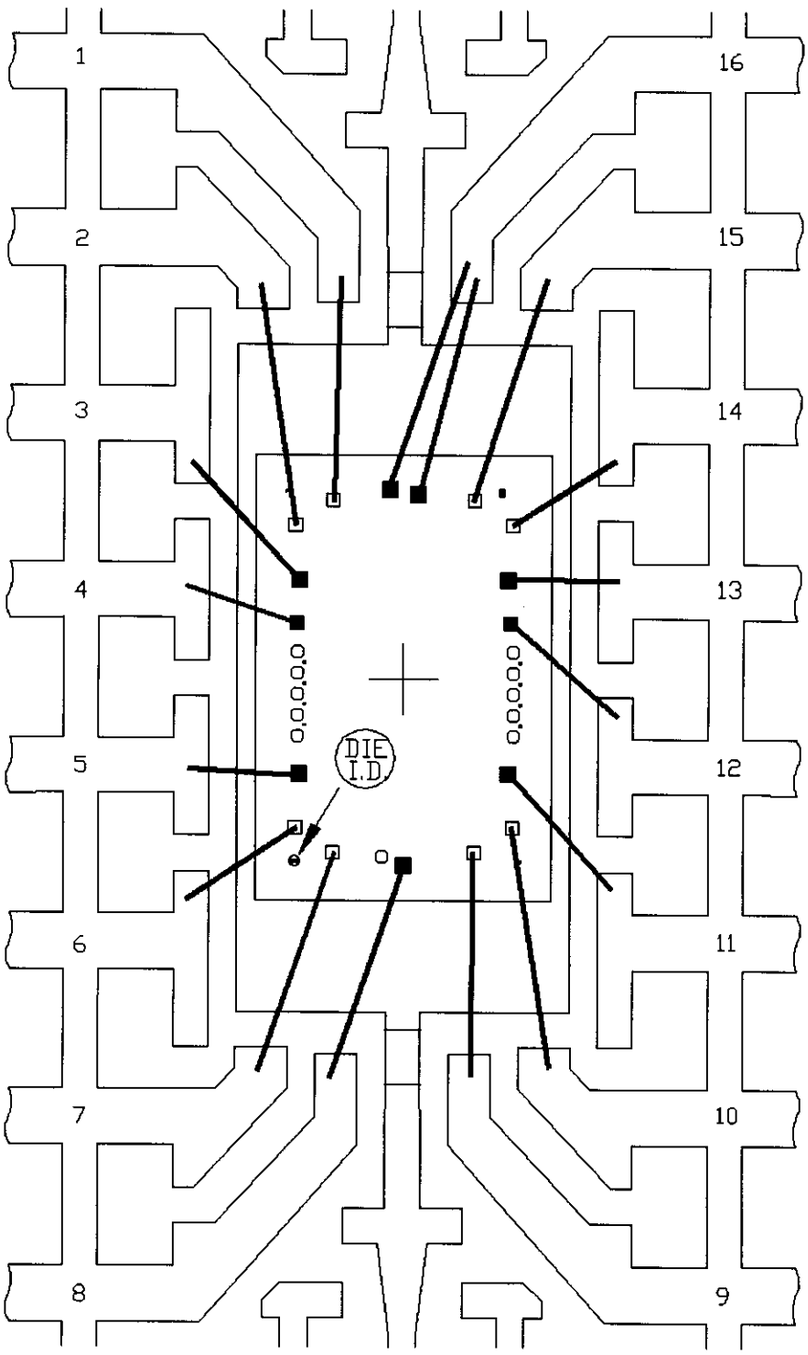
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

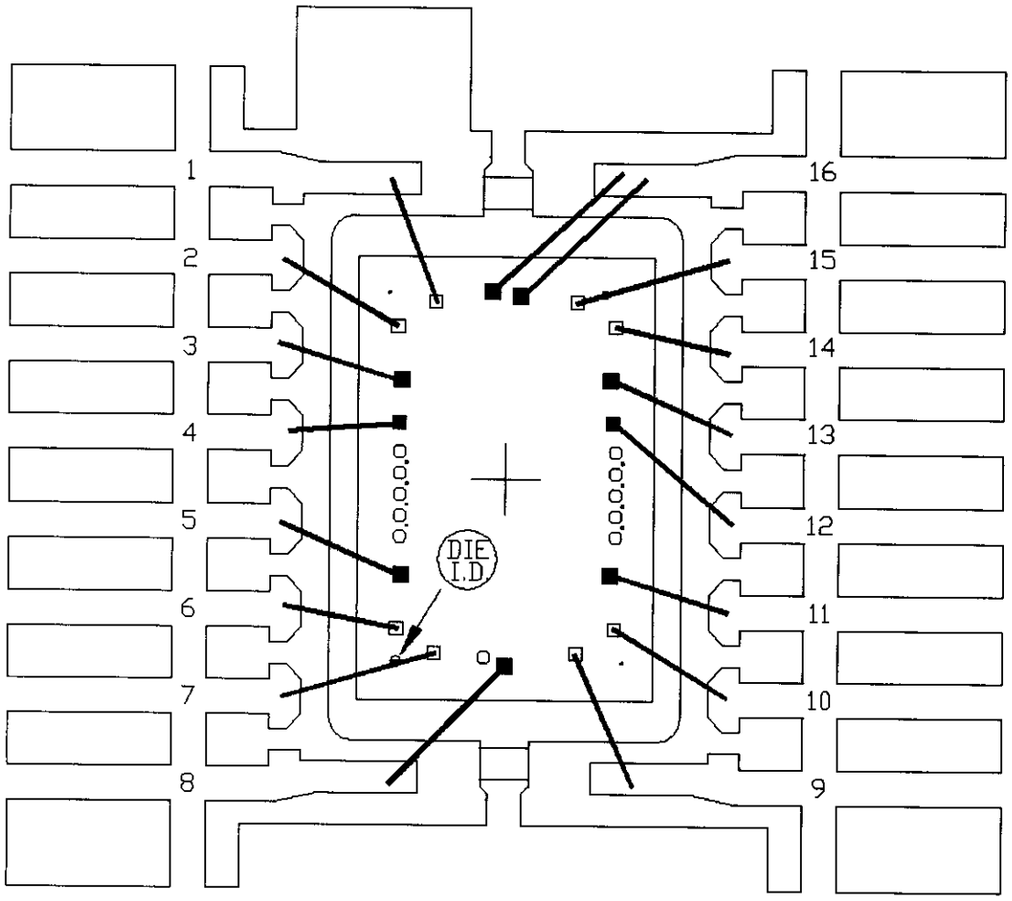




PKG.CODE: P16-1		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 110 X 140	PKG.	SVC MAR 25 1997		BUILDSHEET NUMBER: 05-1901-0165	REV.: A
	DESIGN		3/25/97		



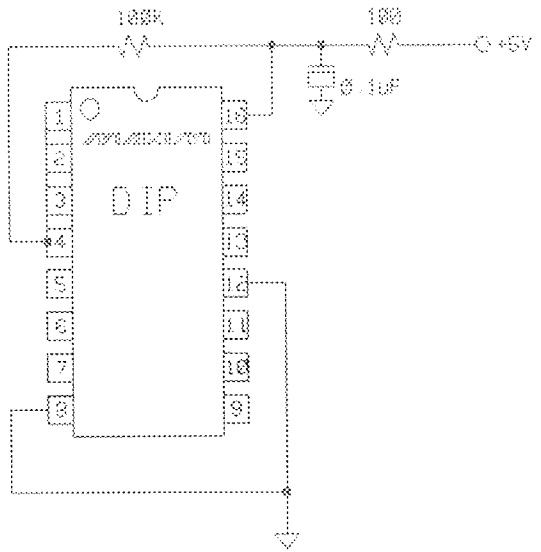
PKG.CODE: S16-5		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 96X190	PKG.	SVC MAR	25 1997	BUILDSHEET NUMBER: 05-1901-0166	REV.: A
	DESIGN		3/25/97		



PKG.CODE: E16-5		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 101X150	PKG.		MAR 25 1997	BUILDSHEET NUMBER: 05-1901-0167
	DESIGN		3/25/97	REV.: A

ONCE PER BOARD

ONCE PER DEVICE



+5V I < 3.5mA

100uF

PS2 I=

PS3 I =

PS4 I=

PS5 I =

PS6 I =

CLK0 FREQ= AMP=

CLK1 FREQ= AMP=

CLK2 FREQ= AMP=

CLK3 FREQ= AMP=

CLK4 FREQ= AMP=

GND

-STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
-BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 168 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL
   [X] MR/883

SPEC. NO. 06-5206 REV: A

DATE: 4/04/97

DRAWN BY: R. TARIGA

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE(S):

MAX3095