SCOPE: **PRECISION DUAL HIGH SPEED ANALOG SWITCHES**

Device Type	Generic Number
01	MAX301M(x)/883B
02	MAX303M(x)/883B
03	MAX305M(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
JE	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
LP	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maximum Ratings

Voltage Referenced to V-

V+ 44V
GND 25V
V_L ..... (GND -0.3V) to (V+)+0.3V
NO_,NC_,IN_,COM_ ..... (V- -2.0V) to (V+ +2.0V) or 30mA, whichever occurs first
Continuous Current, COM_, NO_,NC_ 30mA
Peak Current, COM_,NO_,NC_(pulsed at 1ms, 10% duty cycle max) 100mA
Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
16 lead CERDIP(derate 10.0mW/°C above +70°C) 800mW
20-Pin LCC (derate 9.09mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC:
Case Outline 16 lead CERDIP..... 50°C/W
Case Outline 20-Pin LCC ..... See Mil-Std-1835
Thermal Resistance, Junction to Ambient, ΘJA:
Case Outline 16 lead CERDIP..... 100°C/W
Case Outline 20-Pin LCC ..... 110°C/W

Recommended Operating Conditions.

Ambient Operating Range (T_A) ..... -55°C to +125°C

NOTE 1: Signals on NO_, NC_, or COM_ beyond V+ or V- are clamped by internal diodes. Limit forward current to maximum curent rating.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS 2/ -55 °C <=T_A<= +125°C Unless otherwise specified	Group A Subgroup	Device type	Limits 3/ Min	Limits Max	Units
SWITCH							
Analog-Signal Range	V_{ANA}	4/			V-	V+	V
ON Resistance	R_{ON}	$I_{(NC\ or\ NO)}$ =-10mA, V_{INH}=2.4V, $V_{COM\_}$=+/-10V, V_{INL}=0.8V	1 2,3	All		30 45	Ω
ON Resistance Match Between Channels 5/	R_{ON}	$I_{(NC\ or\ NO)}$ =-10mA, $V_{COM\_}$=+/-10V, V+=15V, V-=-15V	1 2,3	All		2 3	Ω
ON Resistance Flatness 5/	R_{ON}	I_S= -10mA, $V_{COM\_}$=+/-5V V+=15V, V-=-15V	1 2,3	All		3 5	Ω
NC or NO Off Leakage Current	$NC\_{(OFF)}$ or $NO\_{(OFF)}$	$V_{COM\_}$=+/-15.5V V_{NC_or} $V_{NO\_}$=-/+15.5V V+=16.5V, V-=-16.5V	1 2,3	All	-0.25 -20.0	0.25 20.0	nA
COM Off Leakage Current	COM_{OFF}	$V_{COM\_}$=+/-15.5V V_{NC_or} $V_{NO\_}$=-/+15.5V V+=16.5V, V-=-16.5V	1 2,3	All	-0.25 -20.0	0.25 20.0	nA
COM On Leakage Current	COM_{ON}	$V_{COM\_}$=+/-15.5V V_{NC_or} $V_{NO\_}$=+/-15.5V V+=16.5V, V-=-16.5V	1 2,3	All	-0.4 -40.0	0.4 40.0	nA
INPUT							
Input current with V_{IN} low	I_{INL}	$V_{IN\_}$=0.8V all others = 2.4V	1,2,3	All	-1.0	+1.0	µA
Input current with V_{IN} high	I_{INH}	$V_{IN\_}$=2.4V all others = 0.8V	1,2,3	All	-1.0	+1.0	µA
SUPPLY							
Power-Supply Range			1,2,3	All	±4.5	±20	V
Positive Supply Current	I+	All channels on or off, V+=16.5V, V-=-16.5V, V_{IN}=0V or 5.0V	1 2,3	All	-1.0 -5.0	+1.0 +5.0	µA
Negative Supply Current	I-	All channels on or off, V+=16.5V, V-=-16.5V, V_{IN}=0V or 5.0V	1 2,3	All	-1.0 -5.0	+1.0 +5.0	µA
Logic Supply Current	I_L	All channels on or off, V+=16.5V, V-=-16.5V, V_{IN}=0V or 5.0V	1 2,3	All	-1.0 -5.0	+1.0 +5.0	µA
Ground Current	I_{GND}	All channels on or off, V+=16.5V, V-=-16.5V, V_{IN}=0V or 5.0V	1 2,3	All	-1.0 -5.0	+1.0 +5.0	µA
DYNAMIC							
Turn ON time	t_{ON}	Figure 3	9	All		150	ns
Turn OFF time	t_{OFF}	Figure 3	9	All		100	ns
Charge Injection	Q	Figure 5, V_{GEN}=0V, R_{GEN}=0Ω, C_L=10nF 4/	9	All		15	pC
Break-Before-Make Time Delay	t_D	Figure 4 MAX303 only 4/	9	All	10		ns

NOTE 2: V+=15V, V-=-15V, V_L=5V and GND = 0V, V_{INH}=+2.4V, V_{INL}=+0.8V unless otherwise specified.
NOTE 3: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used on this data sheet.
NOTE 4: Guaranteed by design.
NOTE 5: $\Delta R_{ON}=\Delta R_{ON}MAX-\Delta R_{ON}MIN$. On resistance match between channels and flatness are guaranteed only with specified voltages.

Ordering Information.		PKG.Code
01	MAX301MJE/883B	J16
01	MAX301MLP/883B	L20
02	MAX303MJE/883B	J16
02	MAX303MLP/883B	L20
03	MAX305MJE/883B	J16
03	MAX305MLP/883B	L20

FIGURE 1 TERMINAL CONNECTIONS
DEVICE TYPES 01, 02, 03

TERMINAL NUMBER	FUNCTION	MAX 301 MJE	MAX 301 MLP	MAX 303 MJE	MAX 303 MLP	MAX 305 MJE	MAX 305 MLP
1	Drain (Analog Signal) COM1, COM2	COM1	N.C.	COM1	N.C.	COM1	N.C.
2	Not internally connected N.C.	N.C.	COM1	N.C.	COM1	N.C.	COM1
3		N.C.	N.C.	COM3	N.C.	COM3	N.C.
4	Source (Analog Signal) NC3, NC4 normally closed	N.C.	N.C.	NC3	COM3	NO3	COM3
5		N.C.	N.C.	NC4	NC3	NO4	NO3
6		N.C.	N.C.	COM4	N.C.	COM4	N.C.
7		N.C.	N.C.	N.C.	NC4	N.C.	NO4
8	Drain (Analog Signal) COM1, COM2	COM2	N.C.	COM2	COM4	COM2	COM4
9	Source (Analog Signal) NO1, NO2 normally open	NO2	N.C.	NO2	N.C.	NO2	N.C.
10	Digital Logic Inputs IN2, IN1	IN2	COM2	IN2	COM2	IN2	COM2
11	Positive Supply-Voltage Input-connected to substrate (V+)	V+	N.C.	V+	N.C.	V+	N.C.
12	Logic Supply-Voltage Input (V_L)	V_L	NO2	V_L	NO2	V_L	NO2
13	Ground (GND)	GND	IN2	GND	IN2	GND	IN2
14	Negative Supply Voltage Input (V-)	V-	V+	V-	V+	V-	V+
15	Digital Logic Inputs	IN1	V_L	IN1	V_L	IN1	V_L
16	Source (Analog Signal)	NO1	N.C.	NO1	N.C.	NO1	N.C.
17			GND		GND		GND
18			V-		V-		V-
19			IN1		IN1		IN1
20			NO1		NO1		NO1

FIGURE 2. TRUTH TABLES

	MAX301	MAX303	MAX303	MAX305
SWITCH		1,2	3,4	
LOGIC				
0	OFF	OFF	ON	OFF
1	ON	ON	OFF	ON

FIGURE 3: Overvoltage Protection Using Blocking Diodes

See Maxim 1995 New Release Data Book, Volume IV, page 1-13.

FIGURE 4: Switching-Time Test Circuit

See Maxim 1995 New Release Data Book, Volume IV, page 1-14.

FIGURE 5: Break-Before-Make Test Circuit

See Maxim 1995 New Release Data Book, Volume IV, page 1-14.

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 9
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.