19-2601; Rev 0; 10/02

IF Digitally Controlled Variable-Gain Amplifier

General Description

The MAX2027 high-performance, digitally controlled variable-gain amplifier is designed for use from 50MHz to 400MHz.

The device integrates a digitally controlled attenuator and a high-linearity IF amplifier in one package. Targeted for IF signal chains to adjust gain either dynamically or as a one-time channel gain setting, the MAX2027 is ideal for applications requiring high performance. The attenuator provides 23dB of attenuation range with ±0.2dB accuracy.

The MAX2027 is available in a thermally enhanced 20-pin TSSOP-EP package and operates over the -40°C to +85°C temperature range.

Applications

Cellular Base Stations
Receiver Gain Control
Transmitter Gain Control
Broadband Systems
Automatic Test Equipment
Terrestrial Links

Features

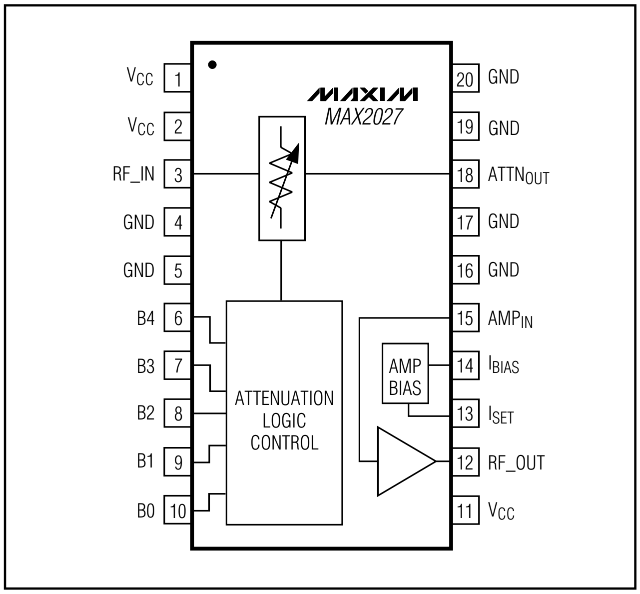
- **50MHz to 400MHz Frequency Range**
- **Variable Gain: -8dB to +15dB**
- **Output IP3: 40dBm (at All Gain Settings and 50MHz)**
- **Noise Figure: 4.7dB at Maximum Gain**
- **Digitally Controlled Gain with 1dB Resolution and ±0.2dB Accuracy**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2027EUP-T	-40°C to +85°C	20 TSSOP-EP*

EP = exposed pad.

Pin Configuration/ Functional Diagram



ABSOLUTE MAXIMUM RATINGS

All Pins (except B0–B4)
to GND ....-0.3V to +5.5V
Input Voltage Levels (B0–B4) ....-0.3V to (V_{CC} + 0.5V)
RF Input Signal 20dBm
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP-EP
(derate 21.7mW/°C above +70°C) 1.7W

Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +165°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(Typical application circuit, V_{CC} = +4.75V to +5.25V, GND = 0V. No RF signals applied, and RF input and output ports are terminated with 50Ω. R1 = 825Ω, T_A = -40°C to +85°C. Typical values are at V_{CC} = +5V and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
Supply Voltage	V_{CC}		4.75	5	5.25	V
Supply Current	I_{CC}			60	70	mA
I_{SET} Current	I_{SET}			0.9		mA
CONTROL INPUTS/OUTPUTS						
Control Bits		Parallel		5		Bits
Input Logic High		(Note 3)	V_{CC} - 0.5			V
Input Logic Low					0.5	V
Input Leakage Current			-2		+2	µA

AC ELECTRICAL CHARACTERISTICS

(Typical application circuit without matching, V_{CC} = +4.75V to +5.25V, GND = 0V, max gain (B0 = B1 = B2 = B3 = B4 = 0), R_1 = 825Ω, P_{OUT} = 5dBm, f_{IN} = 50MHz, 50Ω RF system impedance. Typical values are at V_{CC} = +5V and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	f_R		50		400	MHz
Gain	G	Max gain		15.3		dB
Noise Figure	NF	Max gain		4.7		dB
Minimum Reverse Isolation		Max gain		22		dB
Output 1dB Compression Point	P_{1dB}	Max gain		20.6		dBm
2nd-Order Output Intercept Point	OIP2	$f_1 + f_2$, f_1 = 50MHz, f_2 = 51MHz, 5dBm/tone at RF_OUT		42		dBm
3rd-Order Output Intercept Point	OIP3	All gain conditions, 5dBm/tone at RF_OUT		40		dBm
2nd Harmonic	$2f_{IN}$	All gain conditions		-42		dBc
3rd Harmonic	$3f_{IN}$	All gain conditions		-68		dBc
RF Gain-Control Range				23		dB
Gain-Control Resolution				1		dB
Attenuation Absolute Accuracy		Compared to the ideal expected attenuation		±0.2		dB
Attenuation Relative Accuracy		Between adjacent states		±0.2		dB
Gain Drift Over Temperature		T_A = -40°C to +85°C		±0.1		dB
Gain Flatness Over 50MHz BW		Peak-to-peak for all settings		0.3		dB
Attenuator Switching Time		50% control to 90% RF		40		ns
Input Return Loss		f_R = 50MHz to 150MHz, all gain conditions		15		dB
Output Return Loss		f_R = 50MHz to 150MHz, all gain conditions		15		dB

Note 1: Guaranteed by design and characterization.

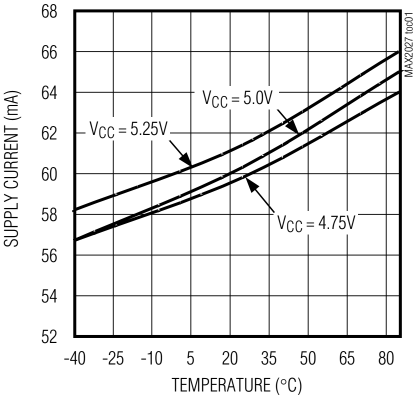
Note 2: All limits reflect losses of external components. Output measurements are taken at RF OUT using the typical application circuit.

Note 3: Device draws current in excess of the specified supply current when a digital input is driven with a voltage of $V_{IN} < V_{CC}$ - 0.5V or V_{IN} > 0.5V. This is due to the CMOS input stage crowbar current. Part may be damaged if operated in this condition for an extended period of time.

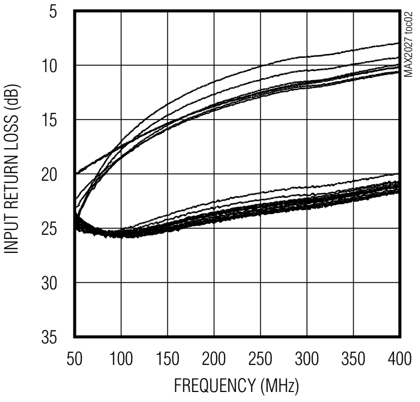
Typical Operating Characteristics

(Typical application circuit, V_{CC} = 5.0V, max gain (B0 = B1 = B2 = B3 = B4 = 0), P_{OUT} = 5dBm, R_1 = 825Ω, T_A = +25°C, unless otherwise noted. External matching components for 300MHz in Table 2 are used for matched circuit.)

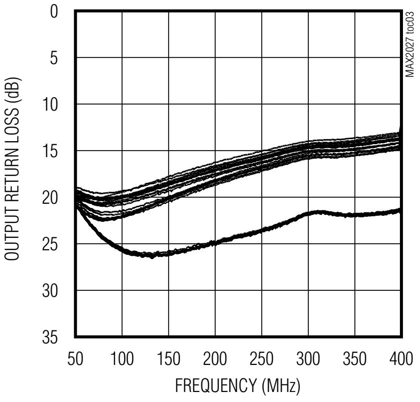
SUPPLY CURRENT vs. TEMPERATURE



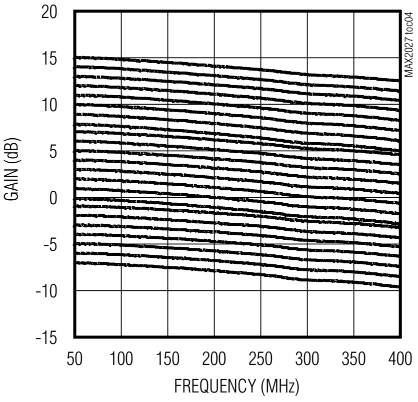
INPUT RETURN LOSS vs. RF FREQUENCY WITHOUT MATCHING (ALL STATES)



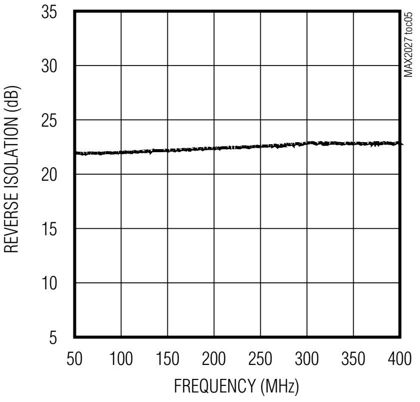
OUTPUT RETURN LOSS vs. RF FREQUENCY WITHOUT MATCHING (ALL STATES)



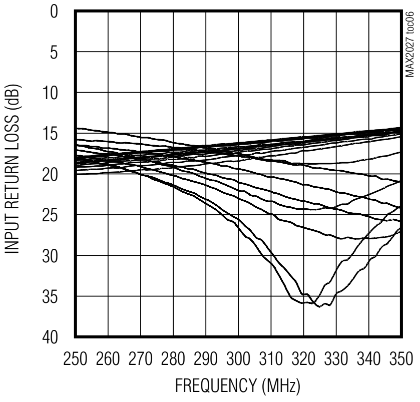
GAIN vs. RF FREQUENCY WITHOUT MATCHING (ALL STATES)



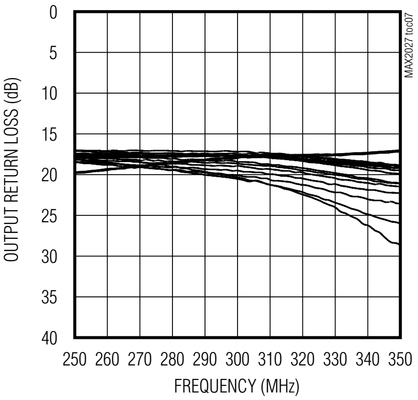
REVERSE ISOLATION vs. FREQUENCY WITHOUT MATCHING



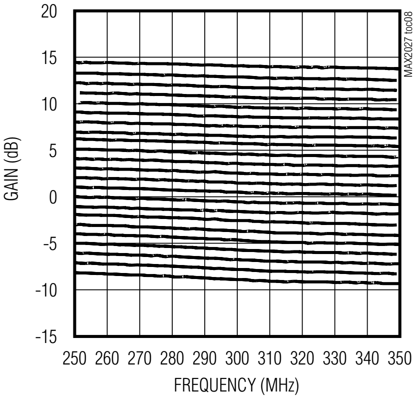
INPUT RETURN LOSS vs. RF FREQUENCY WITH MATCHING (ALL STATES)



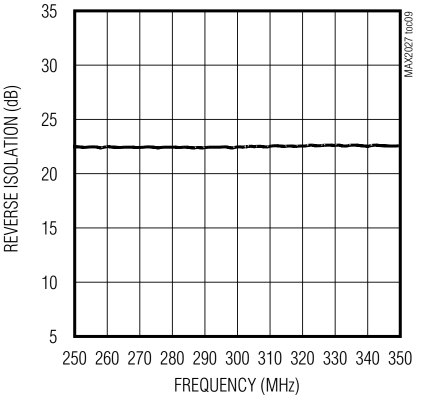
OUTPUT RETURN LOSS vs. RF FREQUENCY WITH MATCHING (ALL STATES)



GAIN vs. RF FREQUENCY WITH MATCHING (ALL STATES)



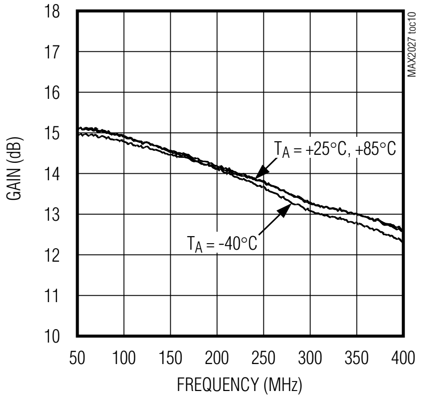
REVERSE ISOLATION vs. FREQUENCY WITH MATCHING



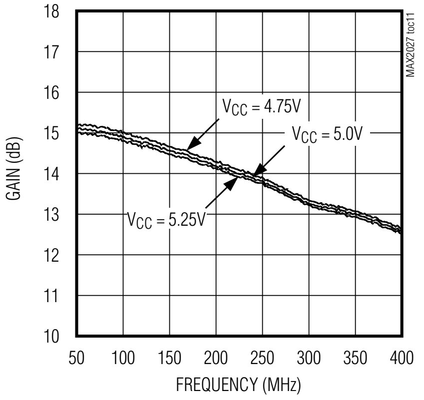
Typical Operating Characteristics (continued)

(Typical application circuit, V_{CC} = 5.0V, max gain (B0 = B1 = B2 = B3 = B4 = 0), P_{OUT} = 5dBm, R_1 = 825Ω, T_A = +25°C, unless otherwise noted. External matching components for 300MHz in Table 2 are used for matched circuit.)

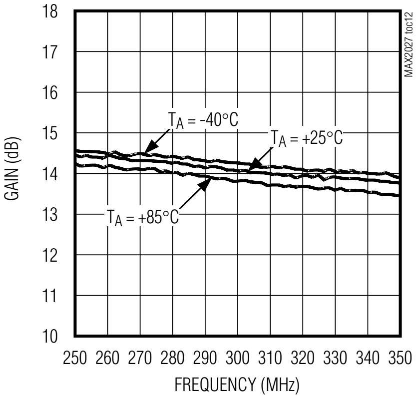
GAIN vs. FREQUENCY WITHOUT MATCHING



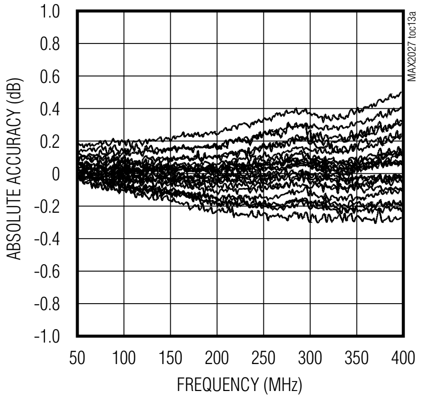
GAIN vs. FREQUENCY WITHOUT MATCHING



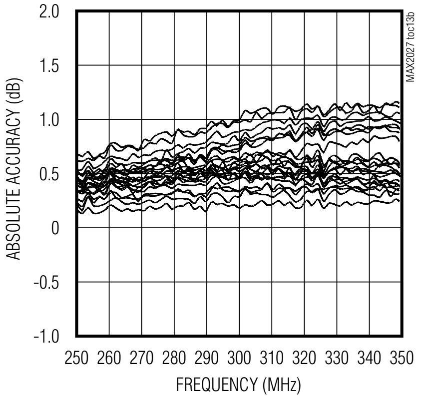
GAIN vs. FREQUENCY WITH MATCHING



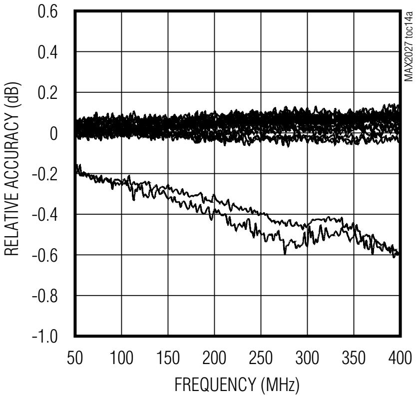
ATTENUATION ABSOLUTE ACCURACY WITHOUT MATCHING (ALL STATES)



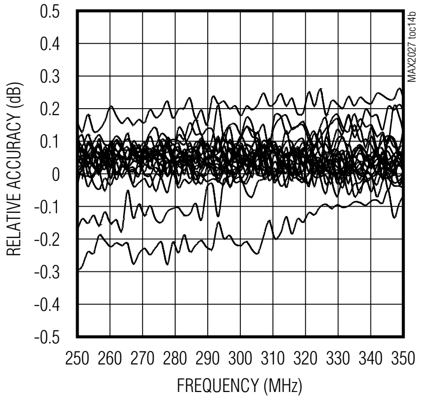
ATTENUATION ABSOLUTE ACCURACY WITH MATCHING (ALL STATES)



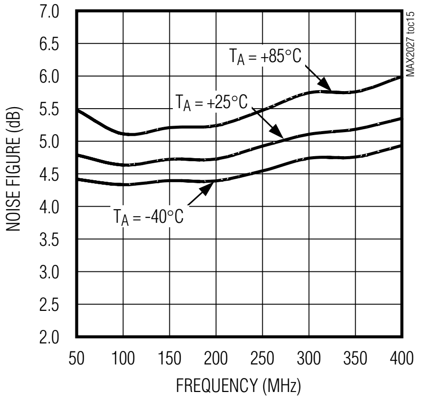
ATTENUATION RELATIVE ACCURACY WITHOUT MATCHING (ALL STATES)



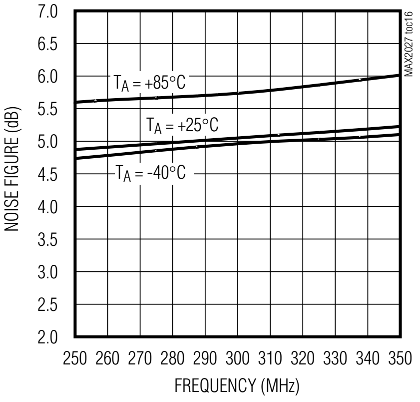
ATTENUATION RELATIVE ACCURACY WITH MATCHING (ALL STATES)



NOISE FIGURE vs. FREQUENCY WITHOUT MATCHING



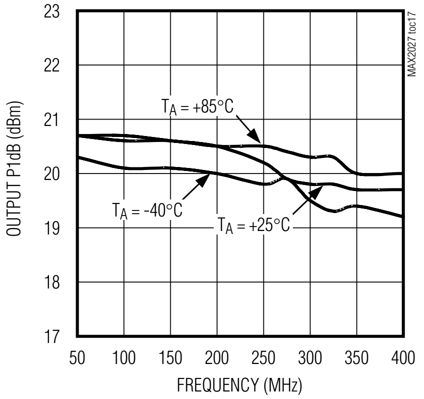
NOISE FIGURE vs. FREQUENCY WITH MATCHING



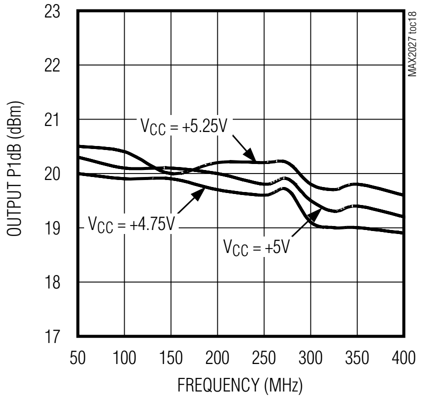
Typical Operating Characteristics (continued)

(Typical application circuit, V_{CC} = 5.0V, max gain (B0 = B1 = B2 = B3 = B4 = 0), P_{OUT} = 5dBm, R_1 = 825Ω, T_A = +25°C, unless otherwise noted. External matching components for 300MHz in Table 2 are used for matched circuit.)

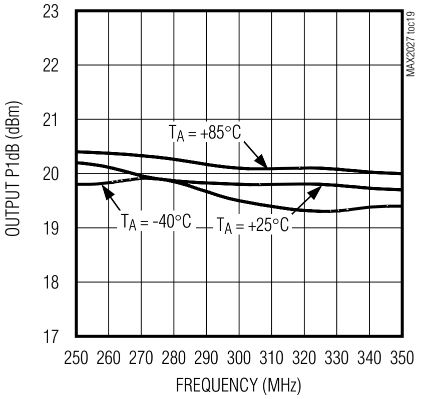
OUTPUT P1dB vs. FREQUENCY WITHOUT MATCHING



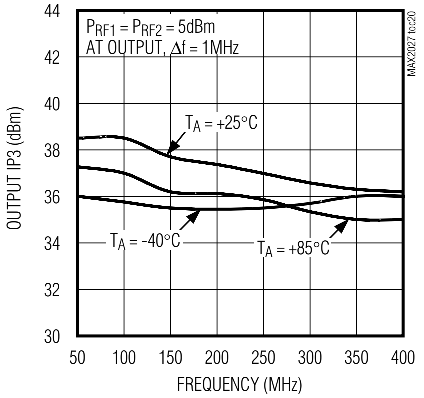
OUTPUT P1dB vs. FREQUENCY WITHOUT MATCHING



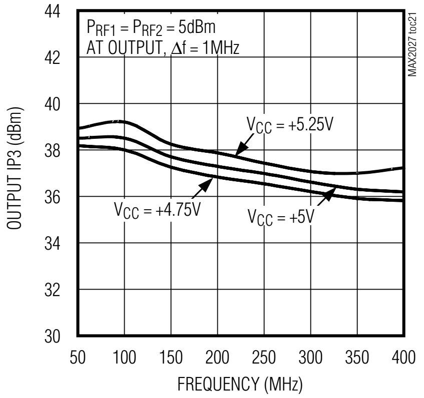
OUTPUT P1dB vs. FREQUENCY WITH MATCHING



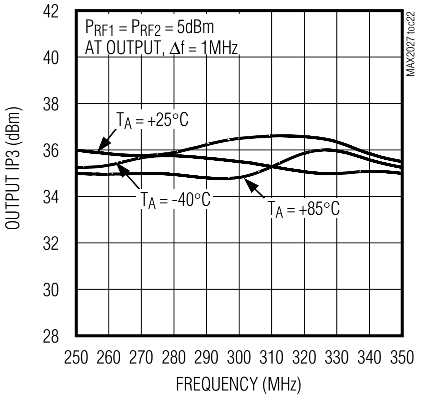
OUTPUT IP3 vs. FREQUENCY WITHOUT MATCHING



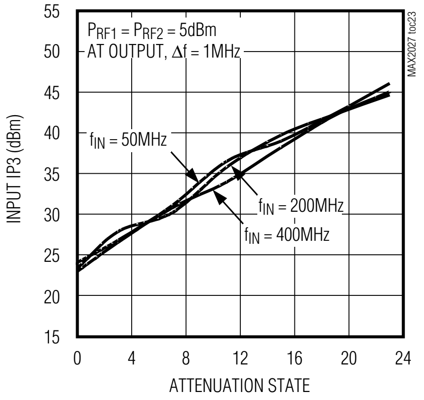
OUTPUT IP3 vs. FREQUENCY WITHOUT MATCHING



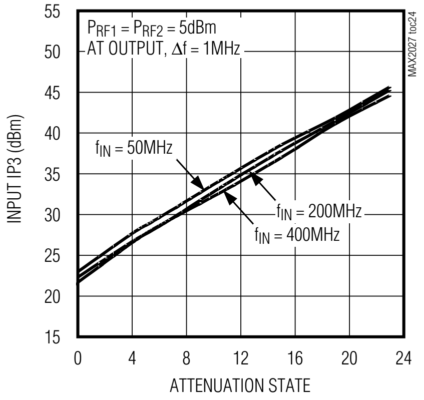
OUTPUT IP3 vs. FREQUENCY WITH MATCHING



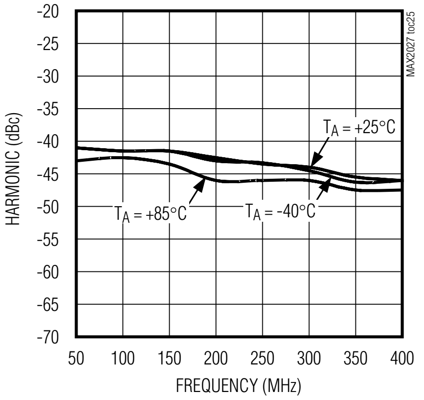
INPUT IP3 vs. ATTENUATION STATE WITHOUT MATCHING



INPUT IP3 vs. ATTENUATION STATE WITH MATCHING



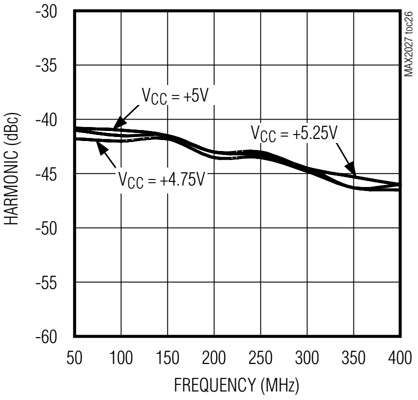
2ND HARMONIC vs. FREQUENCY WITHOUT MATCHING



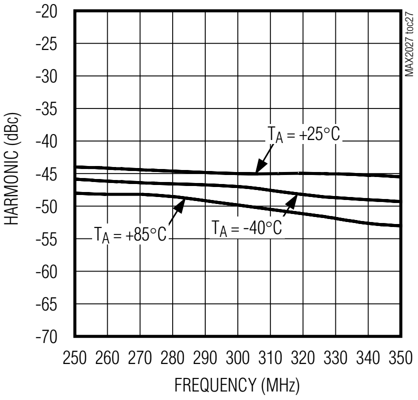
Typical Operating Characteristics (continued)

(Typical application circuit, V_{CC} = 5.0V, max gain (B0 = B1 = B2 = B3 = B4 = 0), P_{OUT} = 5dBm, R_1 = 825Ω, T_A = +25°C, unless otherwise noted. External matching components for 300MHz in Table 2 are used for matched circuit.)

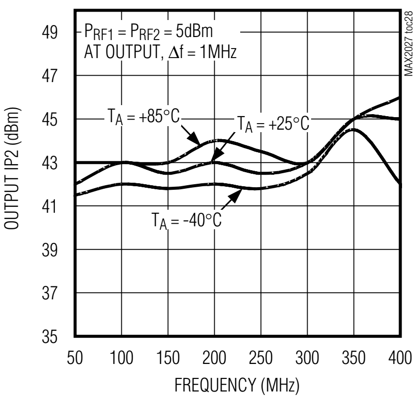
2ND HARMONIC vs. FREQUENCY WITHOUT MATCHING



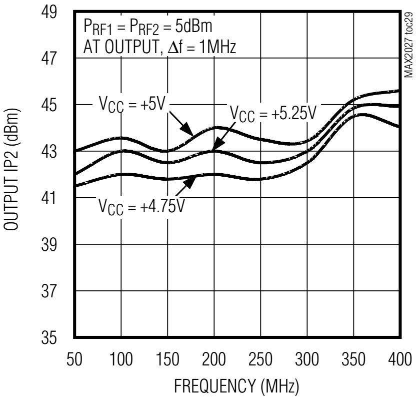
2ND HARMONIC vs. FREQUENCY WITH MATCHING



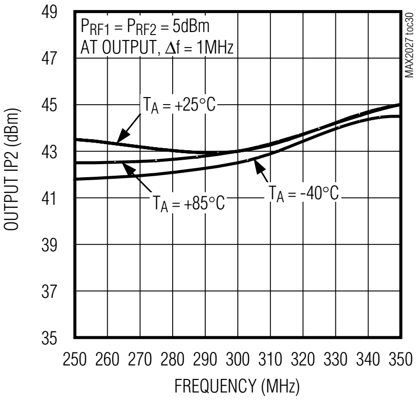
OUTPUT IP2 vs. FREQUENCY WITHOUT MATCHING ($f_1 + f_2$)



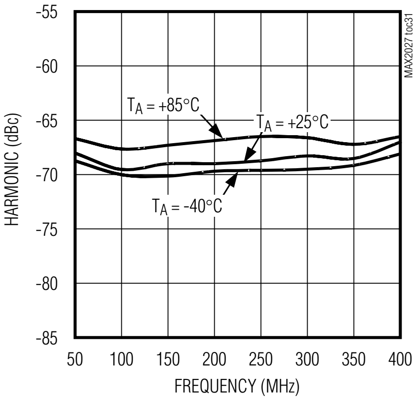
OUTPUT IP2 vs. FREQUENCY WITHOUT MATCHING ($f_1 + f_2$)



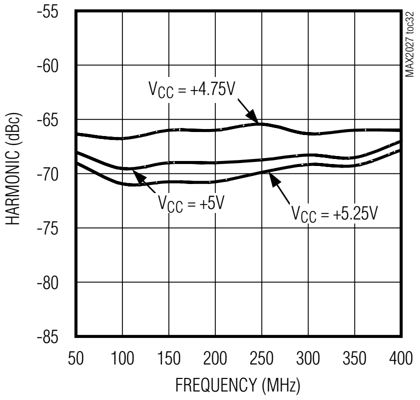
OUTPUT IP2 vs. FREQUENCY WITH MATCHING ($f_1 + f_2$)



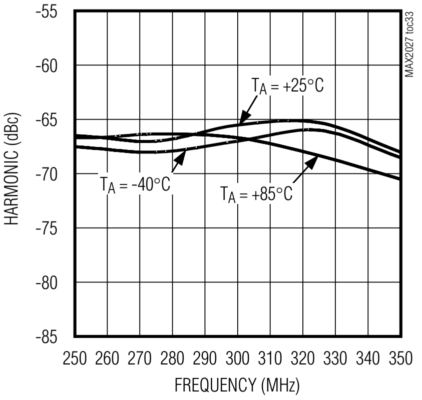
3RD HARMONIC vs. FREQUENCY WITHOUT MATCHING



3RD HARMONIC vs. FREQUENCY WITHOUT MATCHING



3RD HARMONIC vs. FREQUENCY WITH MATCHING



Pin Description

PIN	NAME	FUNCTION
1, 2, 11	V_{CC}	Power Supply. Bypass to GND with capacitors as close to the pin as possible as shown in the typical application circuit (Figure 1).
3	RF_IN	Signal Input. See the typical application circuit for recommended component values. Requires an external DC-blocking capacitor.
4, 5, 16, 17, 19, 20, EP	GND	Ground. Use low-inductance layout techniques on PC board. Solder the exposed pad evenly to the board ground plane.
6–10	B4–B0	Gain-Control Bits. See Table 3 for gain setting.
12	RF_OUT	Signal Output. Requires an external pullup choke inductor (52mA typical current) to V_{CC} along with a DC-blocking capacitor (Figure 1).
13	I_{SET}	Connect an 825Ω resistor from I_{SET} to GND.
14	I_{BIAS}	Amplifier Bias. Connect to AMP_{IN} (pin 15) through a choke inductor (0.3mA typ).
15	AMP_{IN}	Amplifier Input. Requires a DC-coupling capacitor to allow biasing.
18	$ATTN_{OUT}$	Attenuator Output. Requires an external DC-blocking capacitor.

Detailed Description

The MAX2027 is a high-performance, digitally controlled variable-gain amplifier for use in applications from 50MHz to 400MHz.

The MAX2027 incorporates a digital attenuator with a 23dB selectable attenuation range followed by a fixed-gain, high-linearity amplifier. The attenuator is digitally controlled through five logic lines: B0–B4. This on-chip attenuator provides up to 23dB of attenuation with ±0.2dB accuracy. The fixed-gain amplifier utilizes negative feedback to achieve high stability, gain, linearity, and wide bandwidth.

Applications Information

Input and Output Matching

The MAX2027 incorporates on-chip input and output matching for operation below 150MHz. Use a DC-blocking capacitor value of 1000pF for pins 3, 12, and 18 (see Figure 1). For operation above 150MHz, external matching improves performance. Table 1 and Table 2 provide recommended components for device operation.

Digitally Controlled Attenuator

The digital attenuator is controlled through five logic lines: B0, B1, B2, B3, and B4. Table 3 lists the attenuation settings. The input and output of this attenuator require external DC-blocking capacitors. This attenuator insertion loss is 2dB when the attenuator is set to 0dB (B0 = B1 = B2 = B3 = B4 = 0).

Table 1. Suggested Components of Typical Application Circuit

COMPONENT	VALUE	SIZE
C1, C3, C4, C6, C7, C10	1000pF	0603
C2, C5	100pF	0603
R1	825Ω ±1%	0603
R2–R6	47kΩ	0603
L1	330nH	0805
L2	680nH	1008

Table 2. Suggested Matching Components

FREQUENCY	COMPONENT	VALUE	SIZE
200MHz	L3, L4	18nH	0603
	C8, C9	8pF	0603
250MHz	L3, L4	15nH	0603
	C8, C9	8pF	0603
300MHz	L3, L4	11nH	0603
	C8, C9	7pF	0603
400MHz	L3, L4	10nH	0603
	C8, C9	5pF	0603

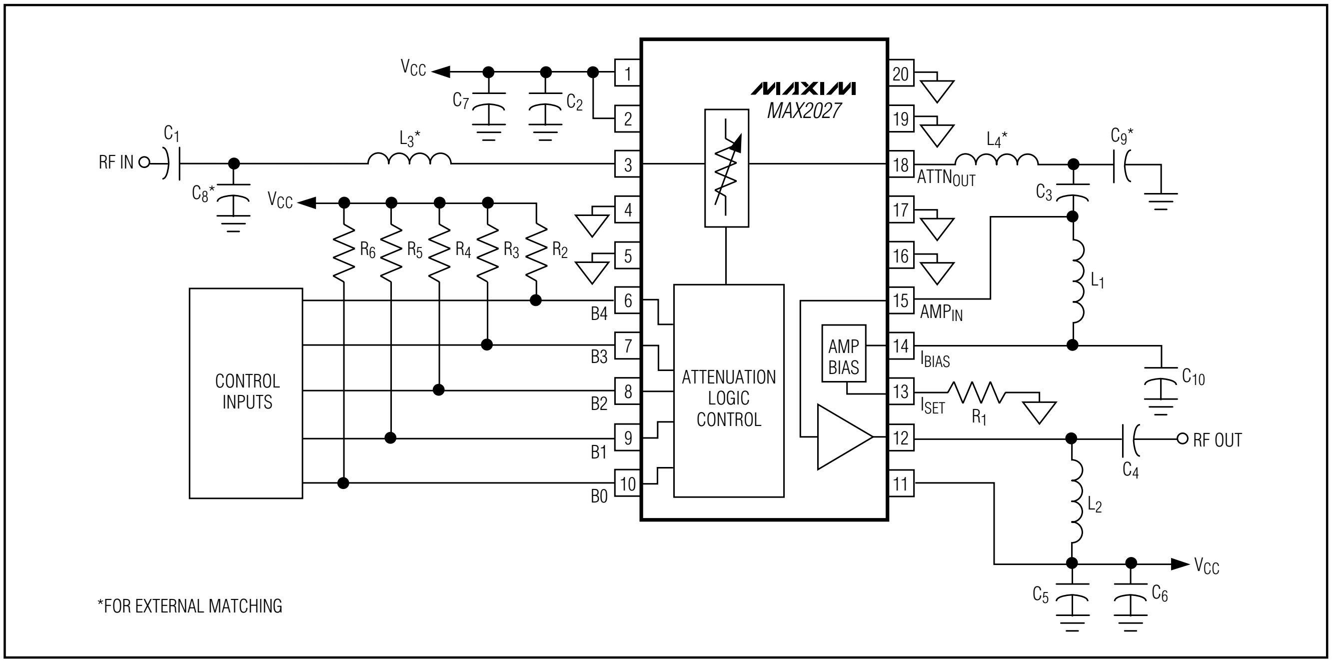


Figure 1. Typical Application Circuit

Fixed-Gain Amplifier

The MAX2027 integrates a fixed-gain amplifier in a negative feedback topology. This fixed-gain amplifier is optimized for a frequency range of operation from 50MHz to 400MHz with a high-output third-order intercept point (OIP3). The bias current is chosen to optimize the IP_3 of the amplifier. When R_1 is 825Ω, the current consumption is 60mA while exhibiting a typical 40dBm output IP_3 at 50MHz.

Choke Inductor

The fixed-gain amplifier output port requires an external pullup choke inductor to V_{CC}. At the input, connect a bias inductor of 330nH from AMP_{IN} (pin 15) to I_{BIAS} (pin 14). At the output, connect a 680nH choke inductor from RF_OUT (pin 12) to V_{CC} (pin 11) to provide bias current to the amplifier.

Layout Considerations

A properly designed PC board is an essential part of any RF/microwave circuit. Keep RF signal lines as short as possible to reduce losses, radiation, and inductance. For the best performance, route the ground pin traces directly to the exposed pad under the package. Solder the exposed pad on the bottom of the device package evenly to the board ground plane to provide a heat transfer path along with RF grounding.

Power-Supply Bypassing

Proper voltage-supply bypassing is essential for high-frequency circuit stability. Bypass each V_{CC} pin with a 1000pF and 100pF capacitor. Connect the 100pF capacitor as close to V_{CC} pins as possible.

Exposed Pad RF/Thermal Considerations

The exposed paddle (EP) of the MAX2027's 20-pin TSSOP-EP package provides a low thermal-resistance path to the die. It is important that the PC board on which the MAX2027 is mounted be designed to conduct heat from the EP. In addition, provide the EP with a low-inductance path to electrical ground. The EP should be soldered to a ground plane on the PC board, either directly or through an array of plated via holes.

Table 3. Attenuation Setting vs. Gain-Control Bits

ATTENUATION 2dB MINIMUM INSERTION LOSS	B4	B3*	B2	B1	B0
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	X	0	0	0
17	1	X	0	0	1
18	1	X	0	1	0
19	1	X	0	1	1
20	1	X	1	0	0
21	1	X	1	0	1
22	1	X	1	1	0
23	1	X	1	1	1

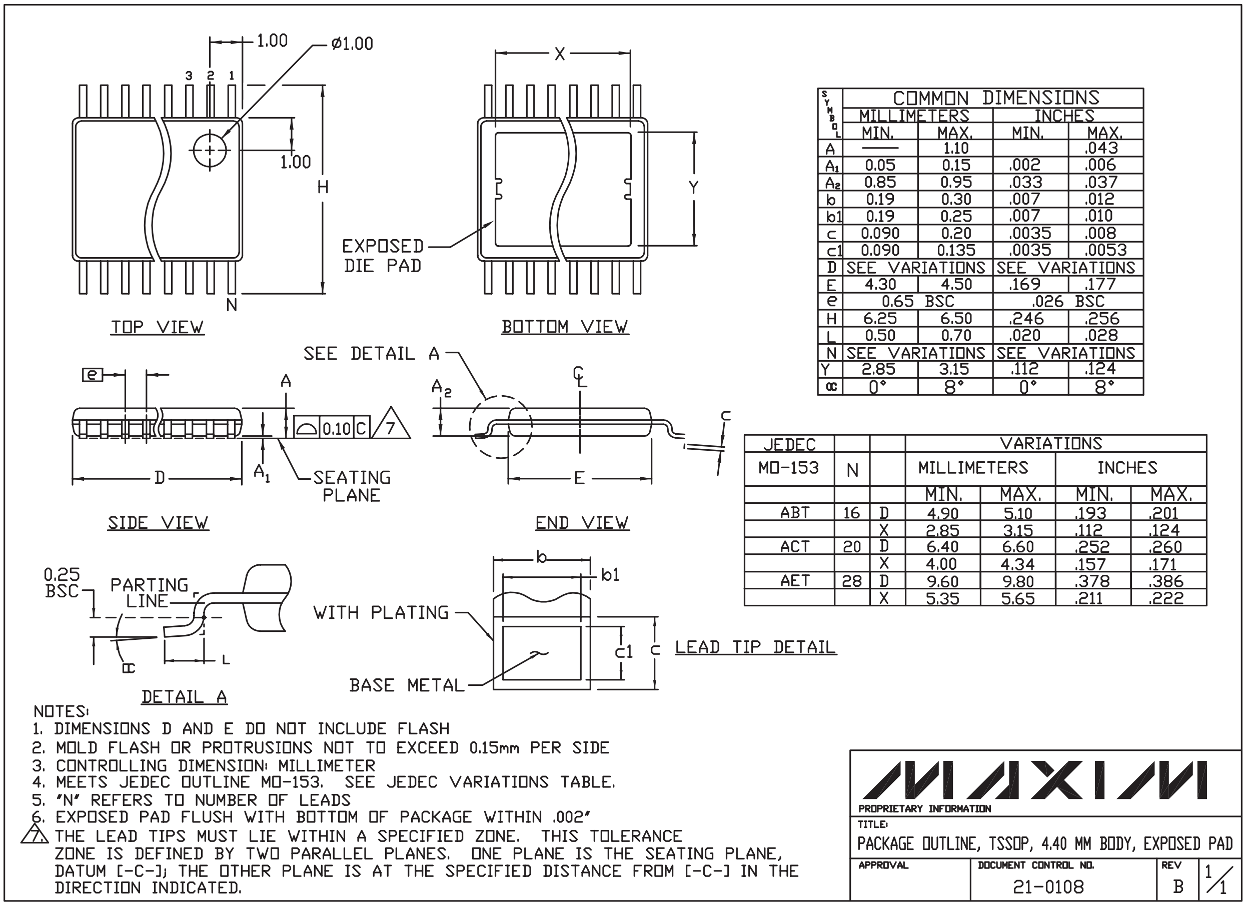
**Enabling B4 disables B3, and the minimum attenuation is 16dB.*

Chip Information

TRANSISTOR COUNT: 325

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
ABT	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
ACT	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AET	28	D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002"
△7 THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, TSSOP, 4.40 MM BODY, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0108	B	1/1