19-2188; Rev 0; 10/01

MAXIM

Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

General Description

The MAX1887/MAX1897 step-down slave controllers are intended for low-voltage, high-current, multiphase DC-to-DC applications. The MAX1887/MAX1897 slave controllers can be combined with any of Maxim's Quick-PWM™ step-down controllers to form a multiphase DC-to-DC converter. Existing Quick-PWM controllers, such as the MAX1718, function as the master controller, providing accurate output voltage regulation, fast transient response, and fault protection features. Synchronized to the master's low-side gate driver, the MAX1887/MAX1897 include the Quick-PWM constant on-time controller, gate drivers for a synchronous rectifier, active current balancing, and precision current-limit circuitry.

The MAX1887/MAX1897 provide the same high efficiency, ultra-low duty factor capability, and excellent transient response as other Quick-PWM controllers. The MAX1887/MAX1897 differentially sense the inductor currents of both the master and the slave across current-sense resistors. These differential inputs and the adjustable current-limit threshold derived from an external reference allow the slave controller to accurately balance the inductor currents and provide precise current-limit protection. The MAX1887/MAX1897's dual-purpose current-limit input also allows the slave controller to automatically enter a low-power standby mode when the master controller shuts down.

The MAX1887 triggers on the rising edge of the master's low-side gate driver, which staggers the on-times of both master and slave, providing out-of-phase operation that can reduce the input ripple current and consequently the number of input capacitors. The MAX1897 features a selectable trigger polarity, allowing out-of-phase or simultaneous in-phase operation.

Applications

Notebook Computers

CPU Core Supply

Single-Stage (BATT to V_{CORE}) Converters

Two-Stage (+5V to V_{CORE}) Converters

Servers/Desktop Computers

Telecom

Quick-PWM is a registered trademark of Maxim Integrated Products, Inc.

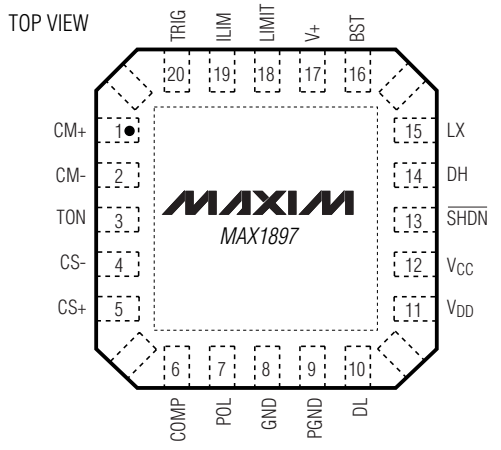
Features

- ♦ **Quick-PWM Slave Controller**
- ♦ **Precise, Active Current Balance (±1.25mV)**
- ♦ **Accurate, Adjustable Current-Limit Threshold**
- ♦ **Optimized for Low-Output Voltages (≤2.0V)**
- ♦ **4.0V to 28V Battery Input Range**
- ♦ **Fixed 300kHz (MAX1887) or Selectable 200kHz/300kHz/550kHz (MAX1897) Switching Frequency**
- ♦ **Drive Large Synchronous-Rectifier MOSFETs**
- ♦ **525µA (typ) I_{CC} Supply Current**
- ♦ **20µA Standby Supply Current**
- ♦ **<1µA Shutdown (MAX1897) Supply Current**
- ♦ **Small 16-Pin QSOP (MAX1887) or Compact 20-Pin 5mm x 5mm QFN (MAX1897) Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1887EEE	-40°C to +85°C	16 QSOP
MAX1897EGP	-40°C to +85°C	20 QFN 5mm × 5mm

Pin Configuration



QFN 5mm x 5mm

Pin Configurations continued at end of data sheet.

Typical Operating Circuit appears at end of data sheet.

Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +30V
V_{CC}, V_{DD} to GND (Note 3) .....-0.3V to +6V
PGND to GND.....±0.3V
TRIG, LIMIT to GND .....-0.3V to +6V
$\overline{SHDN}$ to GND (MAX1897).....-0.3V to +6V
ILIM, CM+, CM-, CS+, CS-, COMP to GND.....-0.3V to (V_{CC} + 0.3V)
TON, POL to GND (MAX1897) .....-0.3V to (V_{CC} + 0.3V)
DL to PGND.....-0.3V to (V_{DD} + 0.3V)
BST to GND .....-0.3V to +36V
DH to LX.....-0.3V to (V_{BST} + 0.3V)
LX to BST.....-6V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
20-Pin 5mm x 5mm QFN (derate 20.0mW/°C above +70°C).....1.60W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = 5V, V_{OUT} = V_{COMP} = 1.2V, V_{CM+} = V_{CM-} = V_{CS+} = V_{CS-} = 1.2V, $\overline{SHDN}$ = V_{CC} (MAX1897), **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		Battery voltage, V+		4.0		28	V
		V_{CC}, V_{DD}		4.5		5.5	
On-Time (Note 1)	t_{ON}	MAX1887 (300kHz), V+ = 12V, V_{COMP} = 1.2V		320	355	390	ns
		MAX1897, V+ = 12V, V_{COMP} = 1.2V	TON = GND	171	190	209	
			TON = open	320	355	390	
			TON = V_{CC}	464	515	566	
Trigger Delay (Note 2)	t_{TRIG}				75		ns
SUPPLY CURRENTS							
Quiescent Supply Current (V+)	I+	Measured at V+; V_{ILIM} > 0.35V			25	40	µA
Quiescent Supply Current (V_{DD}) (Note 3)	I_{DD}	Measured at V_{DD}; V_{ILIM} > 0.35V	MAX1887		525	800	µA
			MAX1897		<1	5	
Quiescent Supply Current (V_{CC}) (MAX1897, Note 3)	I_{CC}	Measured at V_{CC}; V_{ILIM} > 0.35V			525	800	µA
Standby Supply Current (V+)		Measured at V+; ILIM = GND			<1	5	µA
Standby Supply Current (V_{DD}) (Note 3)		Measured at V_{DD}; ILIM = GND	MAX1887		20	40	µA
			MAX1897		<1	5	
Standby Supply Current (V_{CC}) (MAX1897, Note 3)		Measured at V_{CC}; ILIM = GND			20	40	µA
Shutdown Supply Current (V+) (MAX1897)		Measured at V+; V_{CC} = V_{DD} = 0 or 5V, $\overline{SHDN}$ = GND			<1	5	µA
Shutdown Supply Current (V_{DD}) (MAX1897, Note 3)		Measured at V_{DD}; $\overline{SHDN}$ = GND			<1	5	µA
Shutdown Supply Current (V_{CC}) (MAX1897, Note 3)		Measured at V_{CC}; $\overline{SHDN}$ = GND			<1	5	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = 5V, V_{OUT} = V_{COMP} = 1.2V, V_{CM+} = V_{CM-} = V_{CS+} = V_{CS-} = 1.2V, $\overline{SHDN}$ = V_{CC} (MAX1897), **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT SENSING							
On-Time Adjustment Range		0.42 < V_{COMP} < 2.8V, V_{OUT} ≥ 0.7V		-40		+40	%
COMP Output Current	I_{COMP}	Sink and source		30			µA
Current-Balance Offset		(V_{CM+} - V_{CM-}) - (V_{CS+} - V_{CS-}), I_{COMP} = 0, -100mV ≤ (V_{CM+} - V_{CM-}) ≤ +100mV	MAX1887	-1.25		+1.25	mV
			MAX1897	-1.25		+1.25	
Current-Balance Transconductance		(V_{CM+} - V_{CM-}) - (V_{CS+} - V_{CS-}) = ±25mV			1.2		mS
Current-Sense, Common-Mode Range		CM+, CM-, CS+, CS-		-0.2		+2.0	V
Current-Sense Input Current		CM+, CM-, CS+, CS-		-1		1	µA
Positive Current-Limit Threshold	V_{C_LIM}	V_{CM+} - V_{CM-} and V_{CS+} - V_{CS-}	V_{ILIM} = 0.5V	47.5	50	52.5	mV
			V_{ILIM} = 1V	97.5	100	102.5	
Negative Current-Limit Threshold		V_{CS+} - V_{CS-}	V_{ILIM} = 0.5V	-80	-75	-70	mV
			V_{ILIM} = 1V	-160	-150	-140	
ILIM Standby Threshold Voltage				0.2		0.3	V
ILIM Input Current				-100		100	nA
LIMIT Propagation Delay	t_{LIMIT}	Falling edge, 3mV over trip threshold			1.5		µs
LIMIT Output Low Voltage	$V_{OL(LIMIT)}$	I_{SINK} = 1mA				0.1	V
LIMIT Leakage Current	I_{LIMIT}	LIMIT forced to 5.5V			< 0.01	1	µA
FAULT PROTECTION							
V_{CC}/V_{DD} Undervoltage Lockout Threshold (Note 3)		Rising edge, hysteresis = 20mV, switching disabled below this level		3.45		3.85	V
Thermal Shutdown Threshold		Rising, hysteresis = 15°C (typ)			160		°C
GATE DRIVERS							
DH Gate Driver On-Resistance (Note 4)	$R_{ON(DH)}$	V_{BST} - V_{LX} forced to 5V	MAX1887		1.0	3.5	Ω
			MAX1897		1.0	4.5	
DL Gate Driver On-Resistance (Note 4)	$R_{ON(DL)}$	High state (pullup)	MAX1887		1.0	3.5	Ω
			MAX1897		1.0	4.5	
		Low state (pulldown)	MAX1887		0.4	1.0	
			MAX1897		0.4	2.0	
DH Gate Driver Source/Sink Current	I_{DH}	DH forced to 2.5V, V_{BST} - V_{LX} forced to 5V			1.3		A
DL Gate Driver Sink Current	I_{DL}	DL forced to 2.5V			4.0		A
DL Gate Driver Source Current	I_{DL}	DL forced to 2.5V			1.3		A
Dead Time		DL rising			35		ns
		DH rising			26		

Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = 5V, V_{OUT} = V_{COMP} = 1.2V, V_{CM+} = V_{CM-} = V_{CS+} = V_{CS-} = 1.2V, $\overline{SHDN}$ = V_{CC} (MAX1897), **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC							
Logic Input High Voltage (MAX1897)	V_{IH}	$\overline{SHDN}$, POL; V_{CC} = 4.5V to 5.5V		2.4			V
Logic Input Low Voltage (MAX1897)	V_{IL}	$\overline{SHDN}$, POL; V_{CC} = 4.5V to 5.5V				0.8	V
TRIG Logic Levels	V_{TRIG}	350mV hysteresis	High	3.0			V
			Low			1.2	
TON Logic Levels (MAX1897)	V_{TON}	Logic high (V_{CC}; 200kHz operation)		V_{CC} - 0.4			V
		Open (300kHz operation)		1.5		3.1	
		Logic low (GND; 550kHz operation)				0.5	
Logic Input Current		TRIG		-1		+1	µA
		$\overline{SHDN}$ (MAX1897)		-1		+1	
		POL (MAX1897)		-2		+1	
		TON = GND or V_{DD} (MAX1897)		-2		+3	

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = 5V, V_{OUT} = V_{COMP} = 1.2V, V_{CM+} = V_{CM-} = V_{CS+} = V_{CS-} = 1.2V, $\overline{SHDN}$ = V_{CC} (MAX1897), **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
On Time (Note 3)	t_{ON}	MAX1887 (300kHz), V+ = 12V, V_{COMP} = 1.2V		320		390	ns
		MAX1897, V+ = 12V, V_{COMP} = 1.2V	TON = GND (550kHz)	171		209	
			TON = open (300kHz)	320		390	
			TON = V_{CC} (200kHz)	464		566	
SUPPLY CURRENTS							
Quiescent Supply Current (V+)	I+	Measured at V+; V_{ILIM} > 0.35V				40	µA
Quiescent Supply Current (V_{DD}) (Note 3)	I_{DD}	Measured at V_{DD}; V_{ILIM} > 0.35V	MAX1887			800	µA
			MAX1897			5	
Quiescent Supply Current (V_{CC}) (MAX1897, Note 3)	I_{CC}	Measured at V_{CC}; V_{ILIM} > 0.35V				800	µA
Standby Supply Current (V+)		Measured at V+; ILIM = GND				5	µA
Standby Supply Current (V_{DD}) (Note 3)		Measured at V_{DD}; ILIM = GND	MAX1887			40	µA
			MAX1897			5	
Standby Supply Current (V_{CC}) (MAX1897, Note 3)		Measured at V_{CC}; ILIM = GND				40	µA
Shutdown Supply Current (V+) (MAX1897)		Measured at V+; V_{CC} = V_{DD} = 0 or 5V, $\overline{SHDN}$ = GND				5	µA
Shutdown Supply Current (V_{DD}) (MAX1897, Note 3)		Measured at V_{DD}; $\overline{SHDN}$ = GND				5	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = 5V, V_{OUT} = V_{COMP} = 1.2V, V_{CM+} = V_{CM-} = V_{CS+} = V_{CS-} = 1.2V, $\overline{SHDN}$ = V_{CC} (MAX1897), **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown Supply Current (V_{CC}) (MAX1897, Note 3)		Measured at V_{CC}; $\overline{SHDN}$ = GND				5	µA
CURRENT SENSING							
On-Time Adjustment Range		0.42 < V_{COMP} < 2.8V, V_{OUT} ≥ 0.7V		-40		+40	%
COMP Output Current	I_{COMP}	Sink and source		30			µA
Current Balance Offset		(V_{CM+} - V_{CM-}) - (V_{CS+} - V_{CS-}), I_{COMP} = 0, -100mV ≤ (V_{CM+} - V_{CM-}) ≤ +100mV	MAX1887	-2.0		+2.0	mV
			MAX1897	-2.0		+2.0	
Current-Sense, Common-Mode Range		CM+, CM-, CS+, CS-		-0.2		+2.0	V
Positive Current-Limit Threshold	V_{C_LIM}	V_{CM+} - V_{CM-} and V_{CS+} - V_{CS-}	V_{ILIM} = 0.5V	47.5		52.5	mV
			V_{ILIM} = 1V	97.5		102.5	
Negative Current-Limit Threshold		V_{CS+} - V_{CS-}	V_{ILIM} = 0.5V	-80		-70	mV
			V_{ILIM} = 1V	-160		-140	
ILIM Standby Threshold Voltage				0.2		0.3	V
FAULT PROTECTION							
V_{CC}/V_{DD} Undervoltage Lockout Threshold (Note 3)		Rising edge, hysteresis = 20mV, switching disabled below this level		3.45		3.85	V
GATE DRIVERS							
DH Gate Driver On-Resistance (Note 4)	$R_{ON(DH)}$	V_{BST} - V_{LX} forced to 5V	MAX1887			3.5	Ω
			MAX1897			4.5	
DL Gate Driver On-Resistance (Note 4)	$R_{ON(DL)}$	High state (pullup)	MAX1887			3.5	Ω
			MAX1897			4.5	
		Low state (pulldown)	MAX1887			1.0	
			MAX1897			2.0	
LOGIC							
TRIG Logic Levels	V_{TRIG}	350mV hysteresis	High	3.0			V
			Low			1.2	
TON Logic Levels (MAX1897)	V_{TON}	Logic high (V_{CC}; 200kHz operation)		V_{CC} - 0.4			V
		Open (300kHz operation)		1.5		3.1	
		Logic low (GND; 550kHz operation)				0.5	

Note 1: On-time and off-time specifications are measured from 50% point to 50% point at the DH pin with LX = PGND, V_{BST} = 5V, and a 500pF capacitor from DH to LX to simulate external MOSFET gate capacitance. Actual in-circuit times may be different due to MOSFET switching speeds.

Note 2: The trigger delay time, t_{TRIG}, is measured from the time the TRIG pin transitions to time when the DL pin goes low.

Note 3: The 20-pin MAX1897 has a separate analog PWM supply voltage input (V_{CC}) and gate-driver supply input (V_{DD}). For the 16-pin MAX1887 device, the analog PWM supply voltage input and the gate-driver supply voltage input are internally connected and named V_{DD}.

Note 4: Production testing limitations due to package handling require relaxed maximum on-resistance specifications for the MAX1897's QFN package. The MAX1887 and MAX1897 contain the same die, and the QFN package imposes no additional resistance in-circuit.

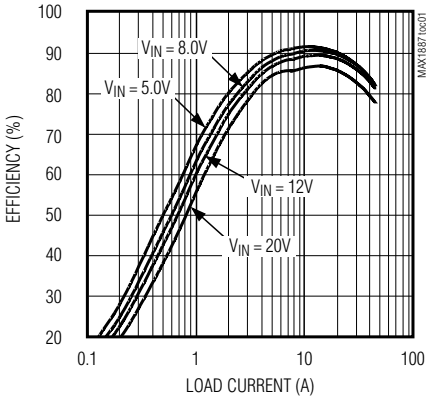
Note 5: Specifications to -40°C are guaranteed by design and not production tested.

Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

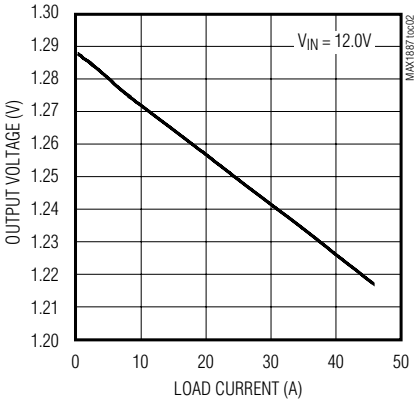
Typical Operating Characteristics

(Circuit of Figure 1, V+ = +12V, V_{CC} = V_{DD} = 5V, V_{OUT} = 1.3V (ZMODE = GND) and 1.0V (ZMODE = V_{CC}), $\overline{SHDN}$ = V_{CC} (MAX1897))

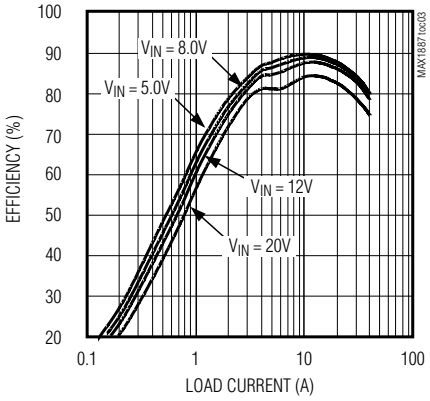
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.3V)



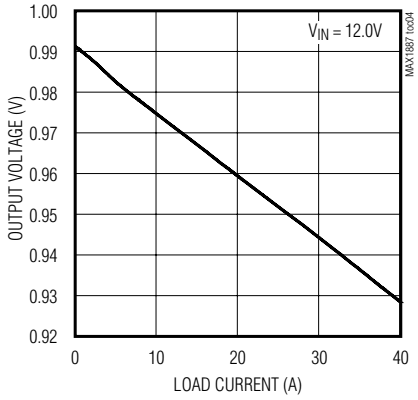
OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.3V, V_{OFFSET} = -10mV)



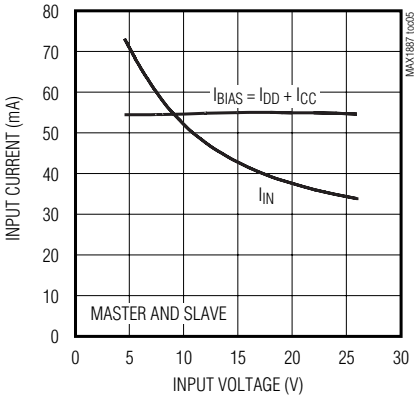
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.0V)



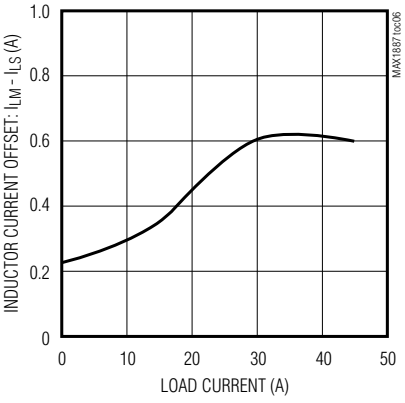
OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.0V, V_{OFFSET} = -10mV)



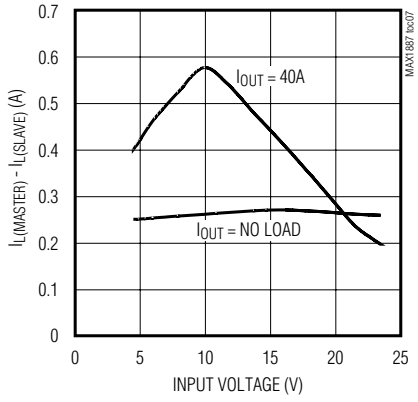
NO LOAD INPUT CURRENT vs. INPUT VOLTAGE



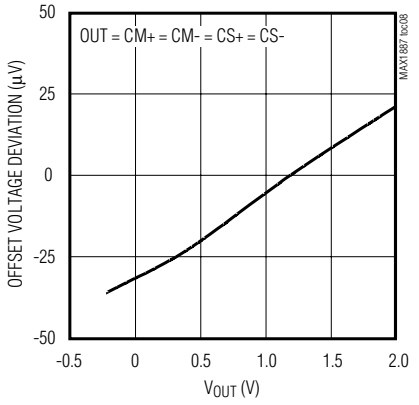
INDUCTOR CURRENT BALANCE vs. LOAD CURRENT



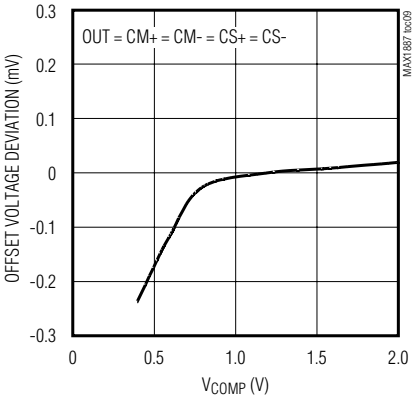
INDUCTOR CURRENT BALANCE vs. INPUT VOLTAGE



OFFSET VOLTAGE DEVIATION vs. CURRENT-SENSE COMMON-MODE VOLTAGE



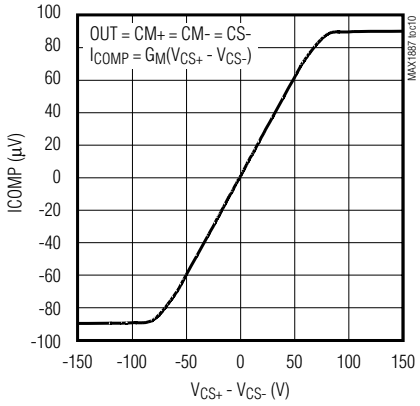
OFFSET VOLTAGE DEVIATION vs. COMPENSATION VOLTAGE



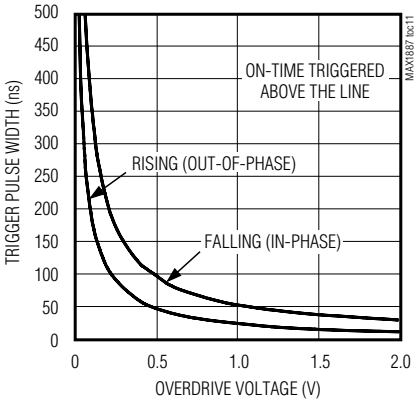
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V+ = +12V, V_{CC} = V_{DD} = 5V, V_{OUT} = 1.3V (ZMODE = GND) and 1.0V (ZMODE = V_{CC}), $\overline{SHDN}$ = V_{CC} (MAX1897))

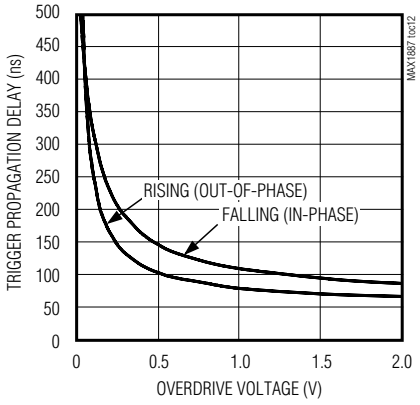
COMPENSATION OUTPUT CURRENT vs. CURRENT-SENSE VOLTAGE DIFFERENTIAL



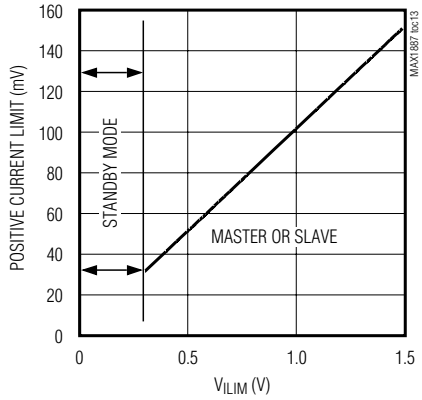
MINIMUM TRIGGER PULSE WIDTH vs. OVERDRIVE VOLTAGE



TRIGGER PROPAGATION DELAY vs. OVERDRIVE VOLTAGE



POSITIVE CURRENT-LIMIT THRESHOLD vs. ILIM VOLTAGE

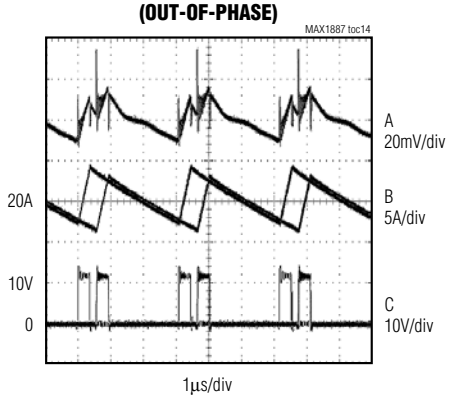


Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

Typical Operating Characteristics (continued)

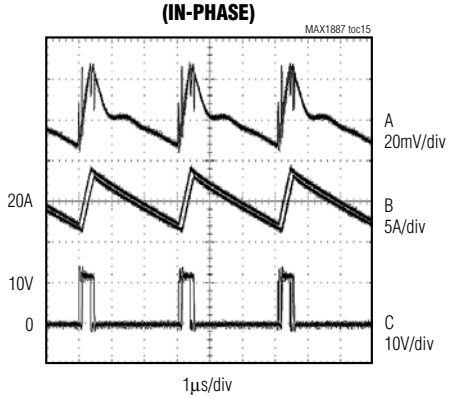
(Circuit of Figure 1, V+ = +12V, V_{CC} = V_{DD} = 5V, V_{OUT} = 1.3V (ZMODE = GND) and 1.0V (ZMODE = V_{CC}), $\overline{SHDN}$ = V_{CC} (MAX1897))

SWITCHING WAVEFORMS (OUT-OF-PHASE)



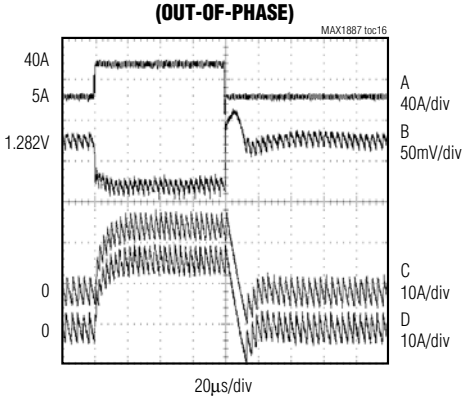
A. OUTPUT VOLTAGE, V_{OUT} = 1.290V (NO LOAD),
B. MASTER/SLAVE INDUCTOR CURRENTS
C. MASTER/SLAVE LX WAVEFORMS,
V_{IN} = 12.0V, I_{OUT} = 40A, POL = V_{CC} (MAX1897)

SWITCHING WAVEFORMS (IN-PHASE)



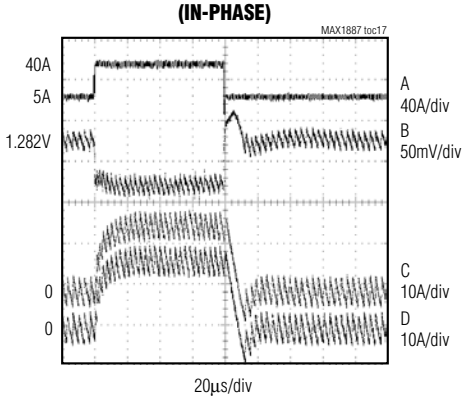
A. OUTPUT VOLTAGE, V_{OUT} = 1.290V (NO LOAD),
B. MASTER/SLAVE INDUCTOR CURRENTS
C. MASTER/SLAVE LX WAVEFORMS,
V_{IN} = 12.0V, I_{OUT} = 40A, POL = GND (MAX1897)

LOAD TRANSIENT (OUT-OF-PHASE)



A. LOAD CURRENT, I_{OUT} = 5A TO 40A
B. OUTPUT VOLTAGE, V_{OUT} = 1.290V (NO LOAD)
C. SLAVE INDUCTOR CURRENT
D. MASTER INDUCTOR CURRENT
V_{IN} = 12.0V, POL = V_{CC} (MAX1897)

LOAD TRANSIENT (IN-PHASE)

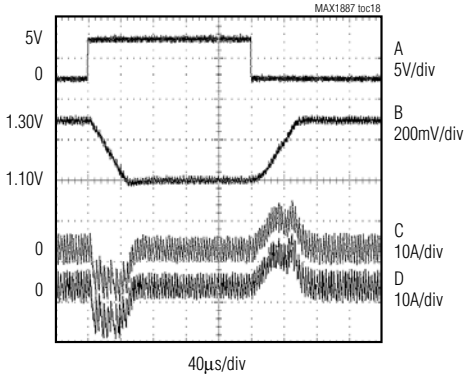


A. LOAD CURRENT, I_{OUT} = 5A TO 40A
B. OUTPUT VOLTAGE, V_{OUT} = 1.290V (NO LOAD)
C. SLAVE INDUCTOR CURRENT
D. MASTER INDUCTOR CURRENT
V_{IN} = 12.0V, POL = GND (MAX1897)

Typical Operating Characteristics (continued)

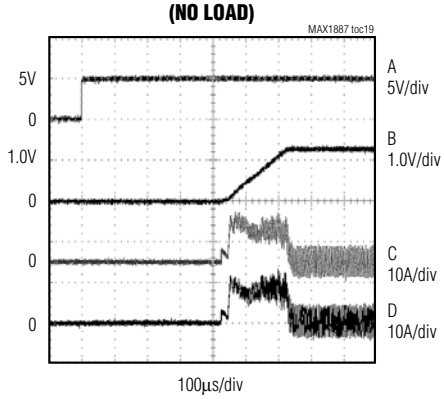
(Circuit of Figure 1, V+ = +12V, V_{CC} = V_{DD} = 5V, V_{OUT} = 1.3V (ZMODE = GND) and 1.0V (ZMODE = V_{CC}), $\overline{SHDN}$ = V_{CC} (MAX1897))

DYNAMIC OUTPUT VOLTAGE TRANSITION



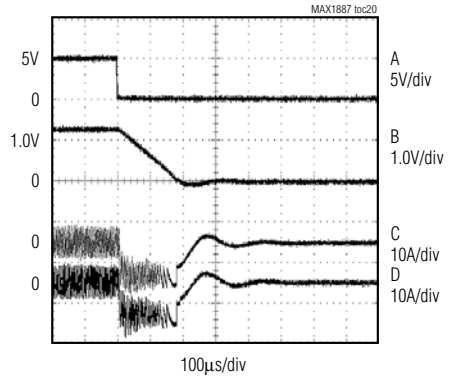
A. ZMODE = 0 TO 5V
B. OUTPUT VOLTAGE, V_{OUT} = 1.30V (ZMODE = GND) OR 1.10V (ZMODE = V_{CC})
C. SLAVE INDUCTOR CURRENT
D. MASTER INDUCTOR CURRENT

STARTUP WAVEFORM (NO LOAD)



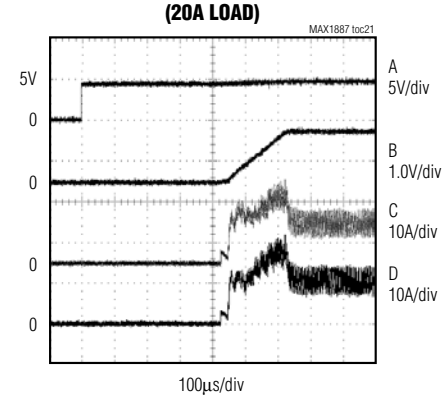
A. MASTER SHUTDOWN, $V_{\overline{SHDN}}$ = 0 TO 5V
B. OUTPUT VOLTAGE, V_{OUT} = 1.290V (NO LOAD)
C. SLAVE INDUCTOR CURRENT
D. MASTER INDUCTOR CURRENT

SHUTDOWN WAVEFORM



A. MASTER SHUTDOWN, $V_{\overline{SHDN}}$ = 5V TO 0
B. OUTPUT VOLTAGE, V_{OUT} = 1.290V (NO LOAD)
C. SLAVE INDUCTOR CURRENT
D. MASTER INDUCTOR CURRENT

STARTUP WAVEFORM (20A LOAD)



A. MASTER SHUTDOWN, $V_{\overline{SHDN}}$ = 0 TO 5V
B. OUTPUT VOLTAGE, V_{OUT} = 1.290V (NO LOAD)
C. SLAVE INDUCTOR CURRENT
D. MASTER INDUCTOR CURRENT
R_{OUT} = 65mΩ (I_{OUT} = 20A)

Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

Pin Description

PIN		NAME	DESCRIPTION
MAX1887	MAX1897		
1	19	ILIM	Dual-Mode Current-Limit Adjustment and Standby Input. The current-limit threshold voltage is 1/10 the voltage seen at ILIM (V_{ILIM}) over a 400mV to 1.5V range. If V_{ILIM} drops below 250mV, the slave controller enters a low-power standby mode, forcing DL high and DH low.
2	20	TRIG	Trigger Input. Connect to the master controller's low-side gate driver. For the MAX1887, a rising edge triggers a single cycle. For the MAX1897, the trigger input's polarity is pin selectable. POL = V_{CC} or floating triggers on the rising edge (out-of-phase operation), and POL = GND triggers on the falling edge (in-phase operation).
3	1	CM+	Master Controller's Positive Current-Sense Input
4	2	CM-	Master Controller's Negative Current-Sense Input
--	3	TON	On-Time Selection Control Input. This is a three-level input used to determine the DH on time (see *On-Time Control and Active Current Balancing*). For the MAX1897, connect TON as follows for the indicated switching frequencies: GND = 550kHz floating = 300kHz V_{CC} = 200kHz. For the MAX1887, the switching frequency is internally configured for 300kHz operation. The slave controller's switching frequency should be selected to closely match the frequency of the master PWM controller.
5	4	CS-	Slave Controller's Negative Current-Sense Input
6	5	CS+	Slave Controller's Positive Current-Sense Input
7	6	COMP	Current Balance Compensation. Connect a series resistor and capacitor between COMP and OUT. See the *Current Balance Compensation* section.
—	7	POL	TRIG Polarity Select Input. Connect POL to V_{CC} or float to trigger on the rising edge of TRIG (out-of-phase operation). Connect POL to GND to trigger on the falling edge of TRIG (in-phase operation). For the MAX1887, POL is internally connected to V_{CC}.
8	8	GND	Analog Ground. Connect the MAX1897's exposed pad to analog ground.
9	9	PGND	Power Ground
10	10	DL	Low-Side Gate-Driver Output. DL swings from PGND to V_{DD}. DL is forced high when the MAX1897 enters standby or shutdown mode.
11	11	V_{DD}	Supply Voltage Input for the DL Gate Driver. For the MAX1887, V_{DD} also serves as the analog supply voltage input that powers the PWM core. Connect to the system supply voltage (4.5V to 5.5V). Bypass to PGND with a 1µF or greater ceramic capacitor, as close to the IC as possible.
—	12	V_{CC}	Analog Supply Voltage Input for PWM Core. Connect V_{CC} to the system supply voltage (4.5V to 5.5V) through a series 10Ω resistor. Bypass to GND with a 0.22µF or greater ceramic capacitor, as close to the MAX1897 as possible.
—	13	$\overline{SHDN}$	Active-Low Shutdown Input. A logic low shuts down the MAX1897 slave controller, immediately pulling DL high and DH low. Connect to V_{CC} for normal operation.

Pin Description (continued)

PIN		NAME	DESCRIPTION
MAX1887	MAX1897		
12	14	DH	High-Side Gate-Driver Output. DH swings from LX to BST.
13	15	LX	Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver.
14	16	BST	Boost Flying-Capacitor Connection. Connect to an external capacitor and diode according to the *Standard Application Circuit* (Figure 1). An optional resistor in series with BST allows DH pullup current to be adjusted.
15	17	V+	Battery Voltage Sense Connection. Connect V+ to the input power source. V+ is used only for PWM one-shot timing (see *On-Time Control and Active Current Balancing*).
16	18	LIMIT	Open-Drain Current-Limit Output. Connect to the master controller's adjustable current-limit input (ILIM) according to the *Standard Application Circuit* (Figure 1). When the voltage across the master controller's current-sense resistor (V_{CM+} - V_{CM-}) exceeds the current-limit threshold (V_{ILIM}/10), the MAX1887/MAX1897 pulls LIMIT low.

Table 1. Component Selection for Standard Applications

COMPONENT	CIRCUIT OF FIGURE 1
Output Voltage	0.6V to 1.75V
Input Voltage Range	7V to 24V
Maximum Load Current	40A
Inductor (each phase)	0.6µH Sumida CDEP134H-0R6 or Panasonic ETQP6F0R6BFA
Frequency	300kHz (TON = float)
High-Side MOSFET (N_H, each phase)	International Rectifier (2) IRF7811W
Low-Side MOSFET (N_L, each phase)	International Rectifier (2) IRF7822 or Fairchild (3) FDS7764A or
Input Capacitor (C_{IN})	(6) 10µF 25V Taiyo Yuden TMK432BJ106KM or TDK C4532X5R1E106M
Output Capacitor (C_{OUT})	(8) 270µF 2.0V Panasonic EEFUE0E271R
Current-Sense Resistors (R_{CS} and R_{CM})	1.5mΩ
Voltage Positioning Gain (A_{VPS})	2

Detailed Description

The MAX1887/MAX1897 step-down slave controllers are intended for low-voltage, high-current, multiphase DC-to-DC applications. The MAX1887/MAX1897 slave controllers can be combined with any of Maxim's Quick-PWM step-down controllers to form a multiphase DC-to-DC converter. When compared to single-phase operation, multiphase conversion lowers the peak inductor current by distributing the load current between parallel power paths. This simplifies component selection, power distribution to the load, and thermal layout. Existing Quick-PWM controllers, such as the MAX1718, function as the master controller, providing accurate output voltage regulation, fast transient response, and multiple fault protection features. Synchronized to the master's low-side gate driver, the MAX1887/MAX1897 include a constant on-time controller, synchronous rectifier gate drive, active current balancing, and precision current-limit circuitry.

On-Time Control and Active Current Balancing

The MAX1887/MAX1897 slave controller uses a constant on-time, voltage feed-forward architecture similar to Maxim's Quick-PWM controllers (Figure 2). The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage and directly proportional to the compensation voltage (V_{COMP}). Another one-shot sets a minimum off-time (130ns typical). The on-time one-shot is triggered when the follow-

Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

Table 2. Component Suppliers

MANUFACTURER	PHONE [COUNTRY CODE]	WEBSITE
MOSFETS		
Fairchild Semiconductor	[1] 888-522-5372	www.fairchildsemi.com
International Rectifier	[1] 310-322-3331	www.irf.com
Siliconix	[1] 203-268-6261	www.vishay.com
CAPACITORS		
Panasonic	[1] 847-468-5624	www.panasonic.com
Sanyo	[65] 281-3226 (Singapore) [1] 408-749-9714	www.secc.co.jp
Taiyo Yuden	[03] 3667-3408 (Japan) [1] 408-573-4150	www.t-yuden.com
Kemet	[1] 408-986-0424	www.kemet.com
INDUCTORS		
Sumida	[1] 408-982-9660	www.sumida.com
Coilcraft	[1] 800-322-2645	www.coilcraft.com
Coiltronics	[1] 561-752-5000	www.coiltronics.com

ing conditions are satisfied: The slave detects a transition on the TRIG input, the slave controller's inductor current is below its current-limit threshold, and the minimum off time has expired. For the MAX1887, a rising edge on the trigger input (TRIG) initiates a new cycle. For the MAX1897, the trigger input's polarity is selected by connecting POL to V_{CC} (rising edge) or to GND (falling edge).

At the slave controller's core is the one-shot that sets the high-side switch's on-time. This fast, low-jitter one-shot adjusts the on-time in response to the input voltage and the difference between the inductor currents in the master and the slave. Two identical transconductance amplifiers (G_{MM} = G_{MS}) integrate the difference between the master and slave current-sense signals. The summed output is connected to COMP, allowing adjustment of the integration time constant with a compensation capacitor connected at COMP. The resulting compensation current and voltage may be determined by the following equations:

$$I_{COMP} = G_{MM}(V_{CM+} - V_{CM-}) - G_{MS}(V_{CS+} - V_{CS-})$$

$$V_{COMP} = V_{OUT} + I_{COMP}Z_{COMP}$$

where Z_{COMP} is the impedance at the COMP output.

The PWM controller uses this integrated signal (V_{COMP}) to set the slave controller's on time. When the master and slave current-sense signals (CM+ to CM- and CS+ to CS-) become unbalanced, the transconductance amplifiers adjust the slave controller's on time, allowing the slave inductor current to increase or decrease until the current-sense signals are properly balanced.

$$t_{ON} = K\left(\frac{V_{COMP}}{V_{IN}}\right)$$

$$= K\left(\frac{V_{OUT}}{V_{IN}}\right) + K\left(\frac{I_{COMP}Z_C}{V_{IN}}\right)$$

= (Master's on time) + (Slave's on-time correction due to current imbalance)

This control algorithm results in balanced inductor currents with the slave switching frequency synchronized to the master. Since the master operates at nearly constant frequency, the slave will as well. The benefits of a constant switching frequency are twofold: first, the frequency can be selected to avoid noise-sensitive regions of the spectrum; second, the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple.

Multiple phase switching effectively distributes the load among the external components, thereby improving the overall efficiency. Distributing the load current between multiple phases lowers the peak inductor current by the

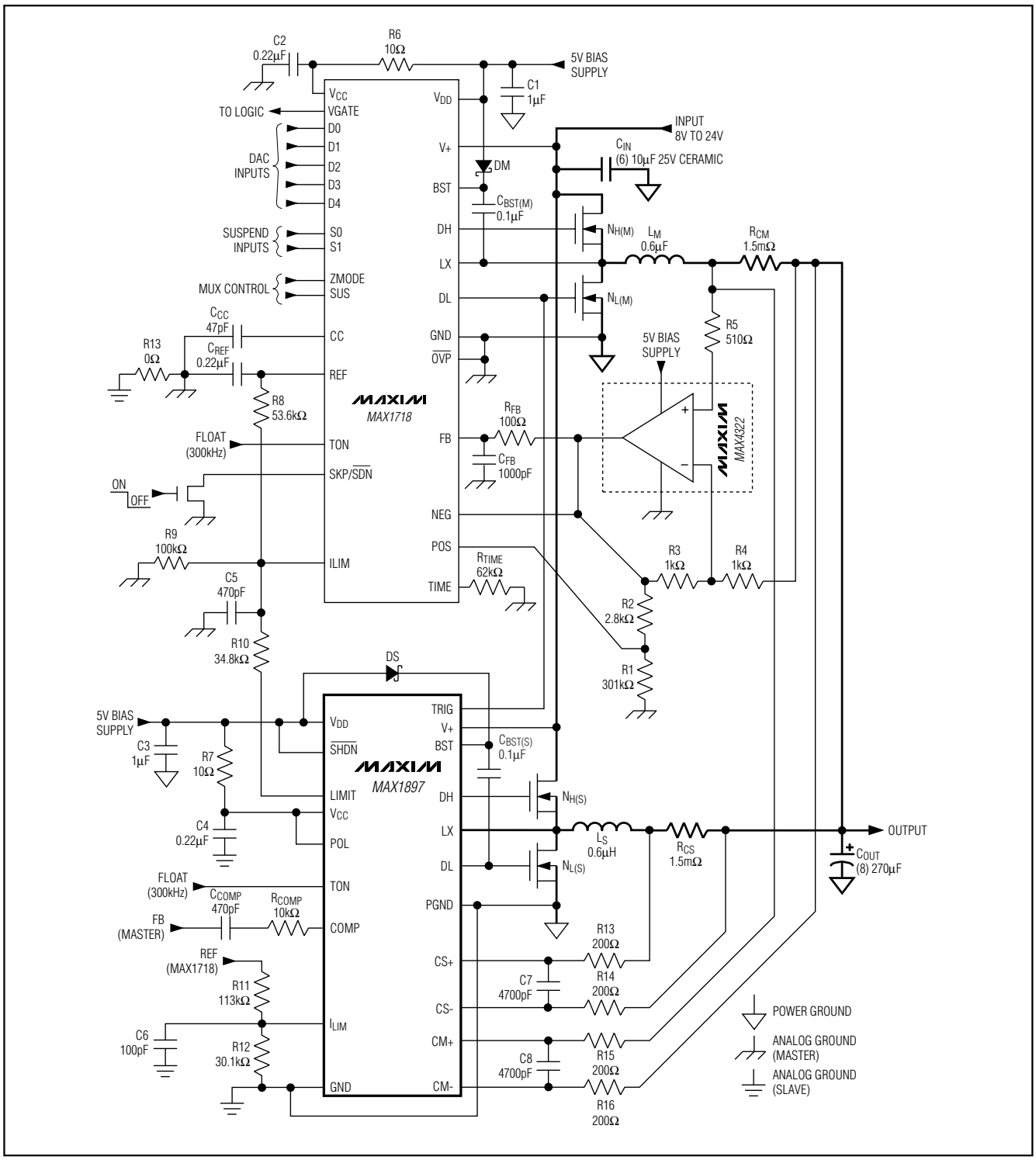


Figure 1. Standard Application Circuit

Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

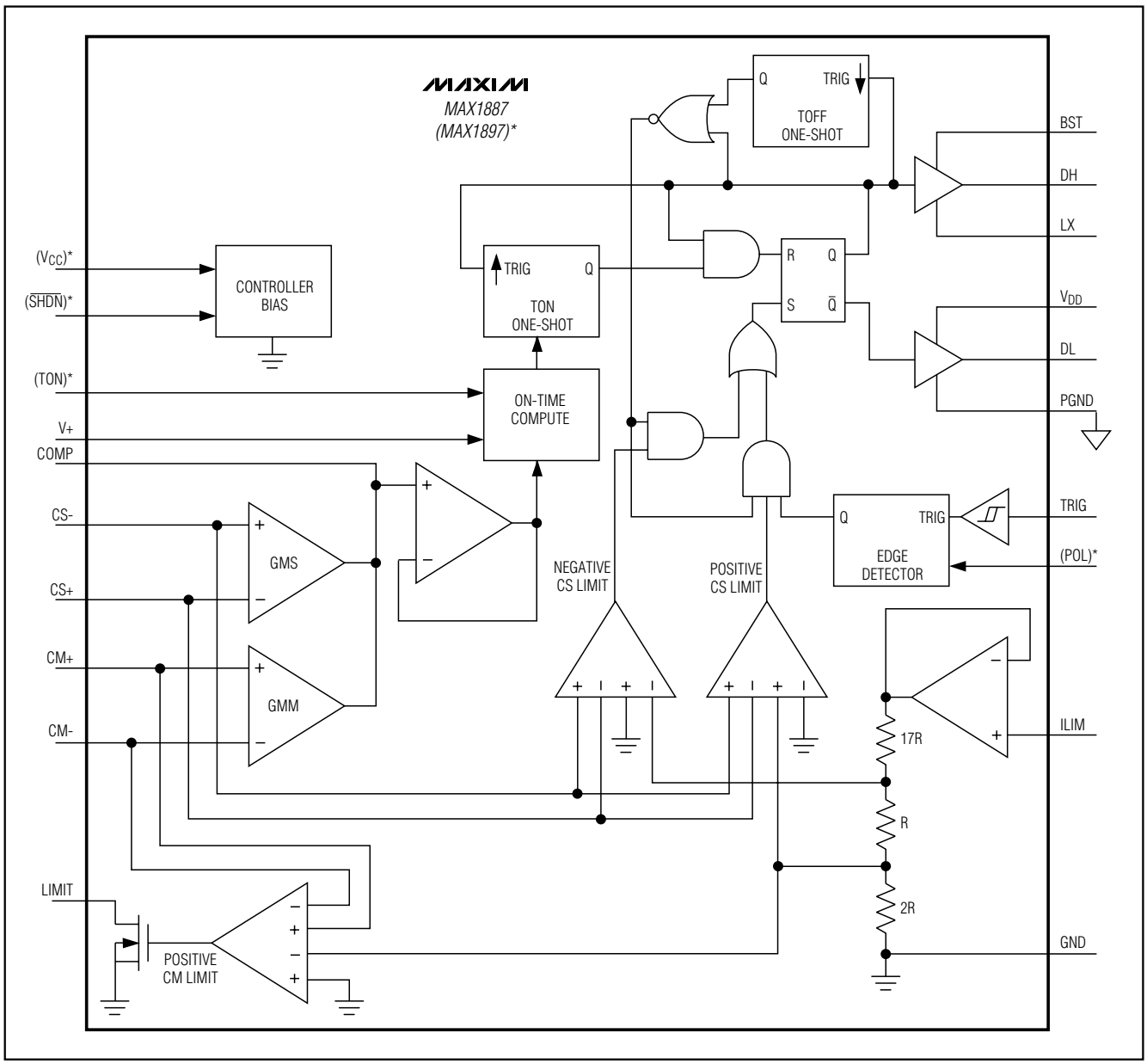


Figure 2. Functional Diagram

number of phases (1/η) when compared to a single-phase converter. This significantly reduces the I^2R losses across the inductor's series resistance, the MOSFETs on-resistance, and the board resistance.

In-Phase and Out-of-Phase Operation

Multiphase systems can stagger the on times of each phase (out-of-phase operation) or simultaneously turn on all phases at the beginning of a new cycle (in-phase operation). When configured for out-of-phase operation, high input-to-output differential voltages ($V_{IN} > \eta V_{OUT}$) prevent the on times from overlapping.

Therefore, the instantaneous input current peaks of each phase do not overlap, resulting in reduced input and output voltage ripple and RMS ripple current. This lowers the input and output capacitor requirements, which allows fewer or less expensive capacitors, and decreases shielding requirements for EMI. When the on-times overlap at low input-to-output differential voltages ($V_{IN} < \eta V_{OUT}$), the input currents of the overlapping phases may sum together, increasing the total input and output ripple voltage and RMS ripple current.

During in-phase operation, the input capacitors must support large, instantaneous input currents when the high-side MOSFETs turn on simultaneously, resulting in increased ripple voltage and current when compared to out-of-phase operation. The higher RMS ripple current degrades efficiency due to power loss associated with the input capacitor's effective series resistance (ESR). This typically requires a large number of low-ESR input capacitors in parallel to meet input ripple current ratings or minimize ESR-related losses.

For the MAX1897, the polarity select input (POL) determines whether rising edges (POL = V_{CC}) or falling edges (POL = GND) trigger a new cycle. For low duty-cycle applications (duty factor < 50%), triggering on the rising edge of the master's low-side gate driver prevents both high-side MOSFETs from turning on at the same time. Staggering the phases in this way lowers the input ripple current, thereby reducing the input capacitor requirements. For applications operating with approximately a 50% duty factor, out-of-phase operation (POL = V_{CC}) causes the slave controller to complete an on-pulse coincident to the master controller determining when to initiate its next on-time. The noise generated when the slave controller turns off its high-side MOSFET could compromise the master controller's feedback voltage and current-sense inputs, causing inaccurate decisions that lead to more jitter in the switching waveforms. Under these conditions, triggering off of the falling edge (POL = GND) of the master's low-side gate driver forces the controllers to operate in-phase, improving the system's noise immunity.

Forced-PWM Mode

The MAX1887/MAX1897 controllers do not allow light-load pulse skipping. Therefore, the master controller must be configured for forced-PWM operation. This PWM control scheme forces the low-side gate drive waveform to be the complement of the high-side gate drive waveform, allowing the inductor current to reverse. During negative load and downward output voltage transitions, forced-PWM operation allows the converter to sink current, rapidly pulling down the output voltage. Another benefit of forced-PWM operation, the switching frequency remains relatively constant over the full load and input voltage ranges.

+5V Bias Supply (V_{CC} and V_{DD})

The MAX1887/MAX1897 require an external +5V bias supply in addition to the battery. Typically this +5V bias supply is the notebook's 95% efficient +5V system supply. Keeping the bias supply external to the IC improves efficiency, eliminates power dissipation limitations, and removes the cost associated with the internal, +5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If standalone capability is needed, the +5V supply can be generated with an external linear regulator.

The 20-pin MAX1897 has a separate analog PWM supply voltage input (V_{CC}) and gate-driver supply input (V_{DD}). For the 16-pin MAX1887 device, the analog PWM supply voltage input and the gate-driver supply voltage input are internally connected and named V_{DD}. The battery input (V+) and +5V bias inputs (V_{CC} and V_{DD}) can be tied together if the input source is a fixed 4.5V to 5.5V supply.

The maximum current required from the +5V bias supply to power V_{CC} (PWM controller) and V_{DD} (gate-drive power) is:

$$I_{BIAS} = I_{CC} + f_{SW}(Q_{G1} + Q_{G2}) = 10mA \text{ to } 45mA \text{ (typ)}$$

where I_{CC} is 525µA typical, f_{SW} is the switching frequency, and Q_{G1} and Q_{G2} are the MOSFET data sheets' total gate charge specification limits at V_{GS} = 5V.

Shutdown (MAX1897 only)

When $\overline{SHDN}$ is driven low, the MAX1897 enters the micropower shutdown mode (Table 3). Shutdown immediately forces DL high, pulls DH low, and shuts down the PWM controller so the total supply current ($I_{CC} + I_{DD} + I+$) drops below 1µA. When $\overline{SHDN}$ is driven high, the MAX1897 operates normally with the PWM controller enabled.

Table 3. Approximate K-Factor Errors

TON CONNECTION (MAX1897)*	FREQUENCY SETTING (kHz)	K-FACTOR (µs)	MAX K-FACTOR ERROR (%)
V_{CC}	200	5	10
Float	300	3.3	10
GND	550	1.8	10

**The MAX1887 is internally preset for 300kHz operation.*

Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

Table 4. Operating Mode Truth Table

$\overline{SHDN}$	ILIM	DL	MODE	COMMENTS
GND	X	High	Shutdown	Micropower, shutdown mode (I_{CC} +I_{DD} < 1µA typ). DL forced high, DH forced low, and the PWM controller disabled.
V_{CC}	GND (< 0.25V)	High	Standby	Low-power, standby mode (I_{CC} + I_{DD} = 20µA typ). DL forced high, DH forced low, and the PWM controller disabled. However, the bias and fault protection circuitry remain active so the MAX1887/MAX1897 can continuously monitor the ILIM input.
V_{CC}	High (> 0.25V)	Switching	Normal Operation	Low-noise, fixed-frequency, PWM operation. The inductor current reverses with light loads.

X = Don't Care

Several Quick-PWM converters that may be used as the master controller ramp down the output voltage at a controlled slew rate when shut down. When combined with these master controllers, the MAX1897 must not be deactivated until the output voltage is fully discharged. Otherwise the slave's low side switch will turn on while the master is still attempting to regulate the output. In these applications, delay the shutdown input signal to the MAX1897 or permanently connect $\overline{SHDN}$ to V_{CC} and use standby mode to conserve power (see *Standby Mode*).

Standby Mode

The MAX1887/MAX1897 slave controllers enter a low-power standby mode when the ILIM voltage (V_{ILIM}) drops below 250mV (Table 4). Similar to shutdown mode, standby forces DL high, pulls DH low, and disables the PWM controller to inhibit switching; however, the bias and fault protection circuitry remain active so the MAX1887/MAX1897 can continuously monitor the ILIM input. When V_{ILIM} is driven above 250mV, the PWM controller is enabled.

When the slave controller's current-limit voltage (V_{ILIM}) is set through a resistive divider between the master controller's reference and GND (see *Current Limit Circuit*), the MAX1887/MAX1897 automatically enters low-power standby mode when the master controller shuts down. As the master's reference powers down, the resistive divider pulls ILIM below 250mV, automatically activating the MAX1887/MAX1897's low-power standby mode.

Current-Limit Circuitry

When the master's inductor current exceeds its valley current limit, the master extends its off time by forcing DL high until the inductor current falls below the current-limit threshold. Without a transition on the master's low-side gate driver, the slave cannot initiate a new on-time pulse so the slave's inductor current ramps down as well, maintaining the current balance. Therefore, the slave's valley current limit only needs to protect the slave controller if the current balance circuitry or the master current limit fails. The slave's ILIM input voltage should be selected to properly adjust the master's current-limit threshold.

Dual-Mode ILIM Input

The current-limit input (ILIM) features dual-mode operation, serving as both the standby mode control input and the current-limit threshold adjustment. The slave controller enters a low-power standby mode when the ILIM voltage (V_{ILIM}) is pulled below 250mV. For ILIM voltages from 400mV to 1.5V, the current-limit threshold voltage is precisely 0.1 × V_{ILIM}. The current-limit voltage may be accurately set with a resistive voltage-divider between the master controller's reference and GND, allowing the MAX1887/MAX1897 to automatically enter the low-power standby mode.

Slave Current Limit

The slave current-limit circuit employs a unique "valley" current-sensing algorithm. If the current-sense signal is above the current-limit threshold, the MAX1887/ MAX1897 will not initiate a new cycle (Figure 3). The actual peak inductor current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-limit threshold, inductor value, and input voltage. The reward for this uncertainty is robust, overcurrent sensing. When combined with master controllers that contain output undervoltage protection circuits, this current-limit method is effective in almost every circumstance.

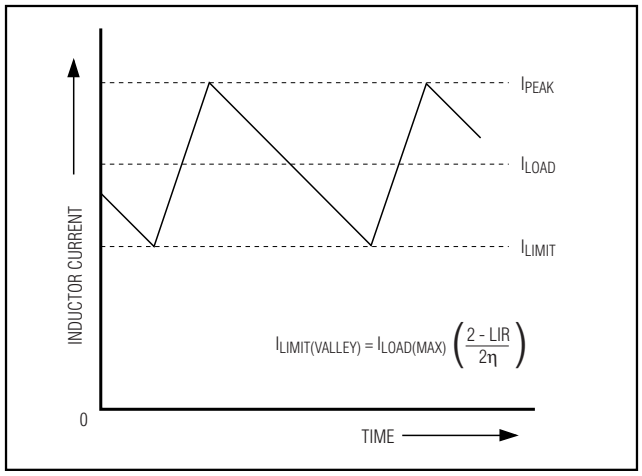


Figure 3. "Valley" Current-Limit Threshold Point

There also is a negative current limit that prevents excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 150% of the positive current-limit threshold, and tracks the positive current limit when ILIM is adjusted.

The MAX1887/MAX1897 uses CS+ and CS- to differentially measure the current across an external sense resistor (R_{CS}) connected between the inductor and output capacitors. This configuration provides precise current balancing, current limiting, and voltage positioning with a 1% current-sense resistor. Reducing the sense voltage decreases power dissipation but increases the relative measurement error.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors don't corrupt the current-sense signals measured at CS+ and CS-. The IC should be mounted relatively close to the current-sense resistor with short, direct traces making a Kelvin sense connection.

Master Current-Limit Adjustment (LIMIT)

The Quick-PWM controllers that may be used as the master controller typically use the low-side MOSFET's on-resistance as its current-sense element. This dependence on a loosely specified resistance with a large temperature coefficient causes inaccurate current limiting. As a result, high current-limit thresholds are needed to guarantee full-load operation under worst-case conditions. Furthermore, the inaccurate current limit mandates the use of MOSFETs and inductors with excessively high current and power dissipation ratings.

The slave includes a precision current-limit comparator that supplements the master's current-limit circuitry. The MAX1887/MAX1897 uses CM+ and CM- to differentially sense the master's inductor current across a current-sense resistor, providing a more accurate current limit. When the master's current-sense voltage exceeds the current limit set by ILIM in the slave (see *Dual-Mode ILIM Input*), the open-drain current-limit comparator pulls LIMIT low (Figure 2). Once the master triggers the current limit, a pulse-width-modulated output signal appears at LIMIT. This signal is filtered and used to adjust the master's current-limit threshold.

High-Side, Gate Driver Supply (BST)

The gate drive voltage for the high-side, N-channel MOSFET is generated by the flying capacitor boost circuit (Figure 4). The capacitor between BST and LX is alternately charged from the external 5V bias supply (V_{DD}) and placed in parallel with the high-side MOSFET's gate-source terminals.

On startup, the synchronous rectifier (low-side MOSFET) forces LX to ground and charges the boost capacitor to 5V. On the second half of each cycle, the switch-mode power supply turns on the high-side MOSFET by closing an internal switch between BST and DH. This provides the necessary gate-to-source voltage to turn on the high-side switch, an action that boosts the 5V gate drive signal above the system's main supply voltage (V+).

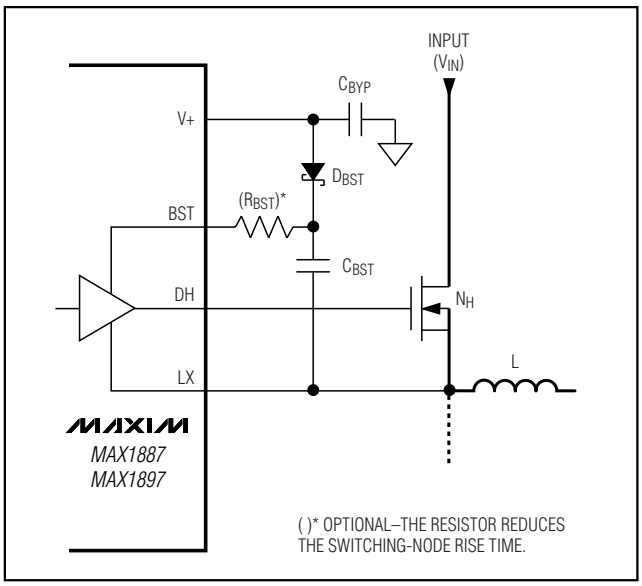


Figure 4. High-Side Gate Driver Boost Circuitry

Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

MOSFET Gate Drivers (DH, DL)

The DH and DL drivers are optimized for driving moderately sized, high-side and larger, low-side power MOSFETs. This is consistent with the low duty factor seen in the notebook CPU environment, where a large V_{IN} - V_{OUT} differential exists. An adaptive dead-time circuit monitors the DL output and prevents the high-side FET from turning on until DL is fully off. There must be a low resistance, low inductance path from the DL driver to the MOSFET gate in order for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry in the MAX1887/MAX1897 will interpret the MOSFET gate as "off" while there is actually charge still left on the gate. Use very short, wide traces (50mils to 100 mils wide if the MOSFET is 1 inch from the device). The dead time at the other edge (DH turning off) is determined by a fixed 35ns internal delay.

The internal pulldown transistor that drives DL low is robust, with a 0.4Ω (typ) on-resistance. This helps prevent DL from being pulled up during the fast rise-time of the LX node, due to capacitive coupling from the drain to the gate of the low-side synchronous-rectifier MOSFET. However, for high-current applications, some combinations of high- and low-side FETs may cause excessive gate-drain coupling, leading to poor efficiency, EMI, and shoot-through currents. This is often remedied by adding a resistor less than 5Ω in series with BST, which increases the turn-on time of the high-side FET without degrading the turn-off time (Figure 4).

Undervoltage Lockout

During startup, the V_{CC} undervoltage lockout (UVLO) circuitry forces the DL gate driver high and the DH gate driver low, inhibiting switching until an adequate supply voltage is reached. Once V_{CC} rises above 3.75V, valid transitions detected at the trigger input initiate a corresponding on-time pulse (see *On-Time Control and Active Current Balancing*). To ensure correct startup, the MAX1887/MAX1897 slave controller's undervoltage lockout voltage must be lower than the master controller's undervoltage lockout voltage.

If the V_{CC} voltage drops below 3.75V, it is assumed that there is not enough supply voltage to make valid decisions. To protect the output from overvoltage faults, DL is forced high in this mode—to force the output to ground. This results in large negative inductor current and possibly small negative output voltages. If V_{CC} is likely to drop in this fashion, the output can be clamped with a Schottky diode to PGND to reduce the negative excursion.

Thermal Fault Protection

The MAX1887/MAX1897 feature a thermal fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the standby logic, forces the DL low-side gate driver high, and pulls the DH high-side gate driver low. This quickly discharges the output capacitors, tripping the master controller's undervoltage lockout protection. The thermal sensor reactivates the slave controller after the junction temperature cools by 15°C.

Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

Input Voltage Range: The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.

Maximum Load Current: There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = I_{LOAD(MAX)} \times 80\%$.

For multiphase systems, each phase supports a fraction of the load, depending on the current balancing. The highly accurate current sensing and balancing implemented by the MAX1887/MAX1897 slave controller evenly distributes the load among each phase:

$$I_{LOAD(SLAVE)} = I_{LOAD(MASTER)} = \frac{I_{LOAD}}{\eta}$$

where η is the number of phases.

Switching Frequency: This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency also is a moving target, due to rapid improvements

in MOSFET technology that are making higher frequencies more practical.

Setting Switch On Time: The constant on-time control algorithm in the master results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. In the slave, the high-side switch on time is inversely proportional to V+ and directly proportional to the compensation voltage (V_{COMP}):

$$t_{ON} = K\left(\frac{V_{COMP}}{V_{IN}}\right)$$

where K is internally preset to 3.3µs for the MAX1887 or externally set by the TON pin-strap connection for the MAX1897 (Table 3)

Set the nominal on time in the slave to match the on time in the master. An exact match is not necessary because the MAX1887/MAX1897 have wide t_{ON} adjustment ranges (±40%). For example, if t_{ON} in the master is set to 250kHz, the slave can be set to either 200kHz or 300kHz and still achieve good performance. Care should be taken to ensure that the COMP voltage remains within its output voltage range (0.42V to 2.80V).

Inductor Operating Point: This choice provides tradeoffs between size vs. efficiency and transient response vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current.

Inductor Selection

The switching frequency and operating point (% ripple or LIR) determine the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT}) \times \eta}{V_{IN} \times f_{SW} \times I_{LOAD(MAX)} \times LIR}$$

where η is the number of phases. Example: η = 2, I_{LOAD} = 40A, V_{IN} = 12V, V_{OUT} = 1.3V, f_{SW} = 300kHz, 30% ripple current or LIR = 0.3:

$$L = \frac{1.3V \times (12V - 1.3V) \times 2}{12V \times 300kHz \times 40A \times 0.3} = 0.64\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)}\left(\frac{2 + LIR}{2\eta}\right)$$

where η is the number of phases.

Transient Response

The inductor ripple current affects transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag also is a function of the maximum duty factor, which can be calculated from the on time and minimum off time:

$$V_{SAG} = \frac{L\left(\Delta I_{LOAD(MAX)}\right)^2\left[\left(\frac{V_{OUT}K}{V_{IN}}\right) + t_{OFF(MIN)}\right]}{2\eta C_{OUT} V_{OUT}\left[\left(\frac{(V_{IN} - V_{OUT})K}{V_{IN}}\right) - t_{OFF(MIN)}\right]}$$

where $t_{OFF(MIN)}$ is the minimum off time (see *Electrical Characteristics*), η is the number of phases, and K is from Table 3.

The amount of overshoot due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 L}{2\eta C_{OUT} V_{OUT}}$$

Setting the Current Limits

The master and slave current-limit thresholds must be great enough to support the maximum load current, even under worst-case operating conditions. Since the master's current limit determines the maximum load (see *Current-Limit Circuitry*), the procedure for setting the current limit is sequential. First, the master's current limit is set based on the operating conditions and the characteristics of the low-side MOSFETs. Then the slave controller is configured to adjust the master's current-limit threshold based on the precise current-sense resistor value and variation in the MOSFET characteristics. Finally, the resulting valley current limit for the slave's inductor occurs above the master's current-limit

Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

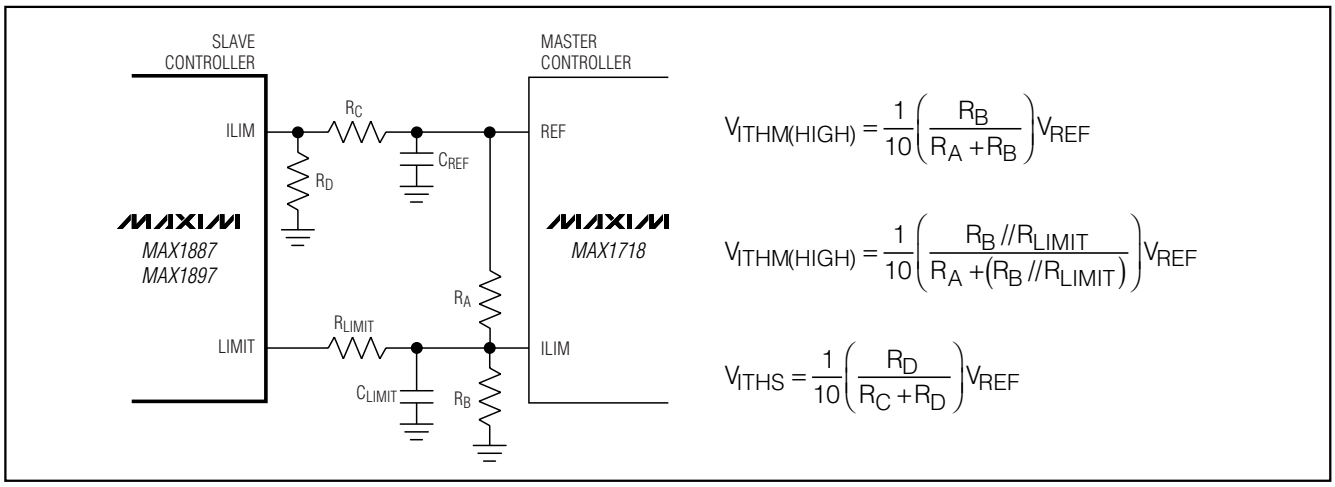


Figure 5. Setting the Adjustable Current Limits

threshold. This is acceptable since the slave's inductor current limit only serves as a fail-safe in case the master and slave inductor currents become significantly unbalanced during a transient.

The basic operating conditions are determined using the same calculations provided in any Quick-PWM regulator data sheet. The valley of the inductor current ($I_{LIMIT(VALLEY)}$) occurs at $I_{LOAD(MAX)}$ divided by the number of phases minus half of the peak-to-peak inductor current:

$$I_{LIMIT(VALLEY)} \geq \left(\frac{I_{LOAD(MAX)}}{\eta}\right) - \left(\frac{\Delta I_{INDUCTOR}}{2}\right)$$

where the peak-to-peak inductor current may be determined by the following equation:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} f_{SW} L}$$

The master's high current-limit threshold must be set high enough to support the maximum load current, even when the master's current-limit threshold is at its minimum tolerance value, as described in the master controller's data sheet. Most Quick-PWM controllers that may be chosen as the master controller use the low-side MOSFET's on-resistance to sense the inductor current. In these applications, the worst-case maximum value for $R_{DS(ON)}$ plus some margin for the rise in $R_{DS(ON)}$ over temperature must be used to determine the master's current-limit threshold. A good general rule is to allow 0.5% additional resistance for each °C of temperature rise. Set the master current-limit threshold to support the maximum load current for the maximum $R_{DS(ON)}$ and minimum current-limit tolerance value:

$$V_{ITHM(HIGH)} \geq (I_{LIMIT(VALLEY)})R_{DS(ON)(MAX)}$$

where V_{ITHM}, the master's current-limit threshold, is typically 1/10th the voltage seen at the master's ILIM input (V_{ITHM} = 0.1 x $V_{LIM(MASTER)}$, see the master controller's data sheet). Connect a resistive voltage-divider from the master controller's internal reference to GND, with the master's ILIM input connected to the center tap (Figure 5). Use 1% tolerance resistors in the divider with 10µA to 20µA DC bias current to prevent significant errors due to the ILIM pin's input current:

$$\frac{V_{ILIM(MASTER)}}{20\mu A} \leq R_B \leq \frac{V_{ILIM(MASTER)}}{10\mu A}$$

$$R_A = \left[\left(\frac{V_{REF(MASTER)}}{V_{ILIM(MASTER)}}\right) - 1\right]R_B$$

Configure the slave controller so its LIMIT output begins to roll off after the master current-limit threshold occurs:

$$V_{ITHS} \geq R_{CM}\left(\frac{V_{ITHM(HIGH)}}{R_{DS(ON)(MAX)}} + \Delta I_{INDUCTOR}\right)$$

where V_{ITHS}, the slave's current-limit threshold, is precisely one-tenth the voltage seen at the slave's ILIM input (V_{ITHS} = 0.1 × $V_{ILIM(SLAVE)}$). Connect a second resistive voltage-divider from the master controller's internal reference to GND, with the slave's ILIM input connected to the center tap (Figure 5). The external adjustment range of 400mV to 1.5V corresponds to a

current-limit threshold of 40mV to 150mV. Use 1% tolerance resistors in the divider with 10µA to 20µA DC bias current to prevent significant errors due to the ILIM pin's input current. Reducing the current-limit threshold voltage lowers the sense resistor's power dissipation, but this also increases the relative measurement error:

$$\frac{V_{ILIM(SLAVE)}}{20\mu A} \le R_D \le \frac{V_{ILIM(SLAVE)}}{10\mu A}$$

$$R_C = \left[\left(\frac{V_{REF(MASTER)}}{V_{ILIM(SLAVE)}}\right) - 1\right] R_D$$

Now, set the current-limit adjustment ratio (A_{ADJ} = $V_{ITHM(HIGH)}/V_{ITHM(LOW)}$) greater than the maximum to minimum on-resistance ratio (A_{RDS} = $R_{DS(ON)(MAX)}/R_{DS(ON)(MIN)}$):

$$A_{ADJ} \ge A_{ROS}$$

$$1 + \left(\frac{R_A // R_B}{R_{LIMIT}}\right) \ge \frac{R_{DS(ON)(MAX)}}{R_{DS(ON)(MIN)}}$$

Increasing A_{ADJ} improves the master's current-limit accuracy but also increases the current limit's noise sensitivity. Therefore, R_{LIMIT} may be selected using the following equation:

$$R_{LIMIT} \le \frac{(R_A // R_B) R_{DS(ON)(MIN)}}{R_{DS(ON)(MAX)} - R_{DS(ON)(MIN)}}$$

Finally, verify that the total load on the master's reference does not exceed 50µA:

$$I_{BIAS(TOTAL)} = \left(\frac{V_{REF}}{R_A + (R_B // R_{LIMIT})}\right) + \left(\frac{V_{REF}}{R_C + R_D}\right) \le 50\mu A$$

Current Limit Design Example

For the typical application circuit shown in Figure 1: V_{IN} = 12V, V_{OUT} = 1.3V, f_{SW} = 300kHz, η = 2, $I_{LOAD(MAX)}$ = 50A, L = 0.6µH, $R_{DS(ON)(MAX)}$ = 6mΩ, $R_{DS(ON)(MIN)}$ = 3mΩ

1) Determine the peak-to-peak inductor current and the valley current limit:

$$\Delta I_{INDUCTOR} = \frac{1.3V \times (12V - 1.3V)}{12V \times 300kHz \times 0.6\mu H} = 6.4A$$

$$I_{LIMIT(VALLEY)} = \left(\frac{50A}{2}\right) - \left(\frac{1}{2} \times 6.4A\right) = 21.8A$$

2) Determine the master's current-limit threshold from the valley current limit and low-side MOSFETs' maximum on-resistance over temperature:

$$V_{ITH(MASTER)} \ge 21.8A \times 6m\Omega = 130mV$$

Now select the resistive-divider values (R_A and R_B in Figure 5) to set the appropriate voltage at the master's ILIM input:

$$R_B = \left(\frac{10 \times 130mV}{20\mu A}\right) to \left(\frac{10 \times 130mV}{10\mu A}\right) = 65k\Omega \text{ to } 130k\Omega$$

Selecting R_B = 100kΩ ±1% provides the following value for R_A:

$$R_A = \left(\frac{2.0V}{10 \times 130mV} - 1\right) \times 100k\Omega \approx 54k\Omega$$

3) Determine the slave's current-limit threshold:

$$V_{ITHS} \ge 1.5m\Omega \times \left(\frac{130mV}{6m\Omega} + 6.4A\right) \approx 42mV$$

Select the resistive-divider values (R_C and R_D in Figure 5) to set the appropriate voltage at the slave's ILIM input:

$$R_D = \left(\frac{10 \times 42mV}{20\mu A}\right) to \left(\frac{10 \times 42mV}{10\mu A}\right) = 21k\Omega \text{ to } 42k\Omega$$

Selecting R_D = 30.1kΩ ±1% provides the following value for R_A:

$$R_C = \left(\frac{2.0V}{10 \times 42mV} - 1\right) \times 30.1k\Omega \approx 113k\Omega$$

4) Determine R_{LIMIT} (Figure 5) from the above equation:

$$R_{LIMIT} \le \frac{(53.6k\Omega // 100k\Omega) \times 3m\Omega}{6m\Omega - 3m\Omega} \approx 35k\Omega$$

5) Finally, verify that that the total bias currents do not exceed the 50µA maximum load of the master's reference:

$$I_{BIAS(TOTAL)} = \left(\frac{2.0V}{54k\Omega + (100k\Omega // 34.8k\Omega)}\right) + \left(\frac{2.0V}{30.1k\Omega + 113k\Omega}\right) = 36\mu A$$

Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

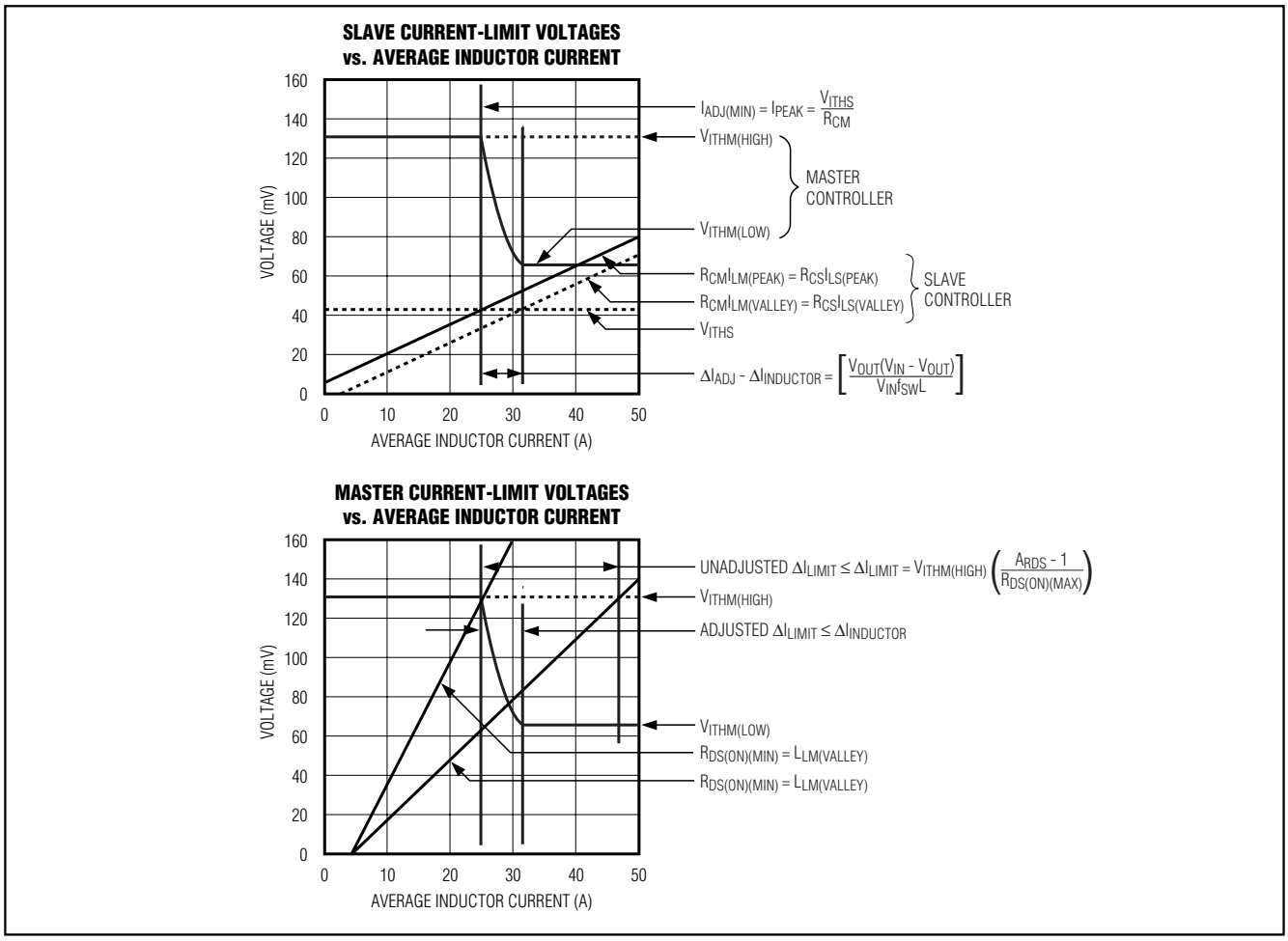


Figure 6. Master/Slave Current-Limit Thresholds

When unadjusted, the on-resistance variation of the low-side MOSFETs results in a maximum current-limit variation (ΔI_{LIMIT}) determined by the following equation:

$$\text{Unadjusted}\,\Delta I_{LIMIT} = V_{ITHM(HIGH)}\left(\frac{A_{RDS} - 1}{R_{DS(ON)(MAX)}}\right)$$

where $A_{RDS} = R_{DS(ON)(MAX)}/R_{DS(ON)(MIN)}$. Using the MAX1887/MAX1897 to adjust the master's current-limit threshold results in a maximum current-limit variation less than the peak-to-peak inductor current:

$$\text{Adjusted}\,\Delta I_{LIMIT} \le \Delta I_{INDUCTOR}$$

As shown in Figure 6, the resulting current-limit variation of the master is dramatically reduced. For the above example, this control scheme reduces the current-limit variation from 21.7A (unadjusted) to less than 6.4A (adjusted).

Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

In CPU V_{CORE} converters and other applications where the output is subject to large load transients, the output capacitor selection typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor selection often depends on how much ESR is needed to maintain an acceptable level of output ripple voltage. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. When operating multiphase systems out-of-phase, the peak inductor currents of each phase are staggered, resulting in lower output ripple voltage by reducing the total inductor ripple current. For out-of-phase operation, the maximum ESR to meet ripple requirements is:

$$R_{ESR} \le \frac{V_{RIPPLE}}{\left(\frac{\eta}{L}\right)\left[\left(\frac{V_{IN} - \eta V_{OUT}}{f_{SW}}\right)\left(\frac{V_{OUT}}{V_{IN}}\right) - (\eta - 1)V_{OUT}t_{TRIG}\right]}$$

This equation may be rewritten as the single phase ripple current minus a correction due to the additional phases:

$$R_{ESR} \le \frac{V_{RIPPLE}}{\left[I_{LOAD(MAX)}LIR - \eta(\eta - 1)\left(\frac{V_{OUT}}{L}\right)(t_{ON} + t_{TRIG})\right]}$$

where t_{TRIG} is the MAX1887/MAX1897's trigger propagation delay, η is the number of phases, and K is from Table 3. When operating the MAX1897 in-phase (POL = GND), the high-side MOSFETs turn on together, so the output capacitors must simultaneously support the combined inductor ripple currents of each phase. For in-phase operation, the maximum ESR to meet ripple requirements is:

$$R_{ESR} \le \frac{V_{RIPPLE}}{I_{LOAD(MAX)}LIR} = \frac{V_{RIPPLE}}{\left(\frac{\eta}{f_{SW}L}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)(V_{IN} - V_{OUT})}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, and other electrolytics).

When using low-capacity filter capacitors such as ceramic or polymer types, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section).

Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{SW}}{\pi}$$

where $f_{ESR} = \frac{1}{2\pi R_{ESR}C_{OUT}}$

For a standard 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum, Sanyo POSCAP, and Panasonic SP capacitors in wide-spread use at the time of publication have typical ESR zero frequencies below 30kHz. In the standard application used for inductor selection, the ESR needed to support a 30mVp-p ripple is 30mV/(40A x 0.3) = 2.5mΩ. Eight 270µF/2.0V Panasonic SP capacitors in parallel provide 1.9mΩ (max) ESR. Their typical combined ESR results in a zero at 39kHz.

Don't put high-value ceramic capacitors directly across the output without taking precautions to ensure stability. Ceramic capacitors have a high ESR zero frequency and may cause erratic, unstable operation. However, it's easy to add enough series resistance by placing the capacitors a couple of centimeters downstream from the junction of the inductor and FB pin.

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and feedback loop instability. Double-pulsing occurs due to noise on the output or because the ESR is so low that there isn't enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor

Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

the switching waveforms (V_{LX} and/or $I_{INDUCTOR}$). Don't allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. The MAX1887/MAX1897 multiphase slave controllers operate out-of-phase (MAX1897 POL = V_{CC} or float), staggering the turn-on times of each phase. This minimizes the input ripple current by dividing the load current among independent phases:

$$I_{RMS} = \left(\frac{I_{LOAD}}{\eta}\right)\left(\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}\right)$$

for out-of-phase operation.

When operating the MAX1897 in-phase (POL = GND), the high-side MOSFETs turn on simultaneously, so input capacitors must support the combined input ripple currents of each phase:

$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}\right)$$

for in-phase operation.

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred because of their resistance to inrush surge currents typical of systems with a mechanical switch or connector in series with the input. If the MAX1887/MAX1897 is operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both of these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of N_H. Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of N_H. If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two SO-8s, DPAK or D^2PAK), and is reasonably priced. Make sure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems may occur.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

$$PD(N_H\,Resistive) = \left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{LOAD}}{\eta}\right)^2 R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation often limits how small the MOSFET can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses don't usually become an issue until the input is greater than approximately 15V.

Calculating the power dissipation of the high-side MOSFET (N_H) due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD(N_H\,Switching) = \frac{\left(V_{IN(MAX)}\right)^2 C_{RSS} f_{SW} I_{LOAD}}{I_{GATE}\eta}$$

where C_{RSS} is the reverse transfer capacitance of N_H and I_{GATE} is the peak gate-drive source/sink current (1A typ).

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter

voltages are applied, due to the squared term in the C × V_{IN}^2 × f_{SW} switching-loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum input voltage:

$$PD(N_L\ Resistive) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right]\left(\frac{I_{LOAD}}{\eta}\right)^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, "overdesign" the circuit to tolerate:

$$I_{LOAD} = \eta I_{VALLEY(MAX)} + \left(\frac{I_{LOAD(MAX)} LIR}{2}\right)$$

where $I_{VALLEY(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. The MOSFETs must have a good-sized heatsink to handle the overload power dissipation.

Choose a Schottky diode (D1) with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to 1/(3η) of the load current. This diode is optional and can be removed if efficiency is not critical.

Current Balance Compensation (COMP)

The current balance compensation capacitor (C_{COMP}) integrates the difference of the master and slave current-sense signals, while the compensation resistor improves transient response by increasing the phase margin. This allows the user to optimize the dynamics of the current balance loop. Excessively large capacitor values increase the integration time constant, resulting in larger current differences between the phases during transients. Excessively small capacitor values allow the current loop to respond cycle by cycle but can result in small DC current variations between the phases. Likewise, excessively large series resistance can also cause DC current variations between the phases. Small series resistance reduces the phase margin, resulting in marginal stability in the current balance loop. For most applications, a 470pF capacitor and 10kΩ series resistor from COMP to the converter's output voltage works well.

The compensation network can be tied to V_{OUT} to include the feed-forward term due to the master's on time. (See *On-time Control and Active Current Balancing*.) To reduce noise pick-up in applications that have a widely distributed layout, it is sometimes helpful to connect the compensation network to quiet analog ground rather than V_{OUT}.

Applications Information

Voltage Positioning and Effective Efficiency

Powering new mobile processors requires careful attention to detail to reduce cost, size, and power dissipation. As CPUs became more power hungry, it was recognized that even the fastest DC-DC converters were inadequate to handle the transient power requirements. After a load transient, the output instantly changes by $ESR_{COUT} \times \Delta I_{LOAD}$. Conventional DC-DC converters respond by regulating the output voltage back to its nominal state after the load transient occurs (Figure 7). However, the CPU only requires that the output voltage remain above a specified minimum value. Dynamically positioning the output voltage to this lower limit allows the use of fewer output capacitors and reduces power consumption under load.

For a conventional (nonvoltage-positioned) circuit, the total voltage change is:

$$Vp\text{-}p1 = 2 \times (ESR_{COUT} \times \Delta I_{LOAD}) + V_{SAG} + V_{SOAR}$$

where V_{SAG} and V_{SOAR} are defined in Figure 8. Setting the converter to regulate at a lower voltage when under load allows a larger voltage step when the output current suddenly decreases (Figure 7). So the total voltage change for a voltage-positioned circuit is:

$$Vp\text{-}p2 = (ESR_{COUT} \times \Delta I_{LOAD}) + V_{SAG} + V_{SOAR}$$

where V_{SAG} and V_{SOAR} are defined in the *Design Procedure*. Since the amplitudes are the same for both circuits (Vp-p1 = Vp-p2), the voltage-positioned circuit tolerates twice the ESR. Since the ESR specification is achieved by paralleling several capacitors, fewer units are needed for the voltage-positioned circuit.

An additional benefit of voltage positioning is reduced power consumption at high load currents. Since the output voltage is lower under load, the CPU draws less current. The result is lower power dissipation in the CPU, although some extra power is dissipated in R_{SENSE}. For a nominal 1.6V, 22A output (R_{LOAD} = 72.7mΩ), reducing the output voltage 2.9% gives an

Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

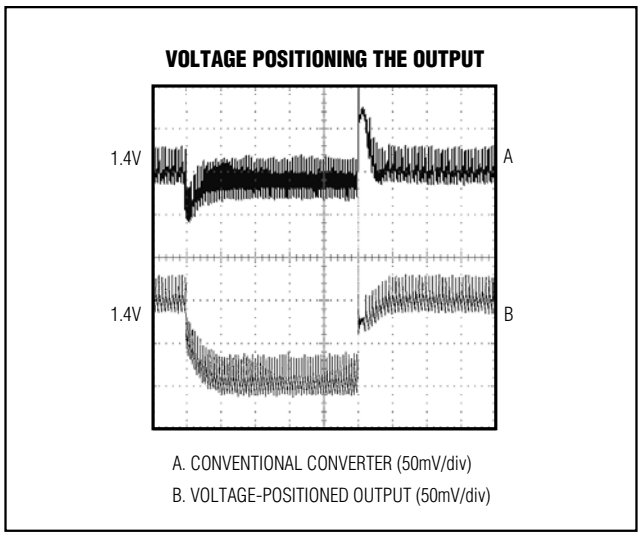


Figure 7. Voltage Positioning the Output

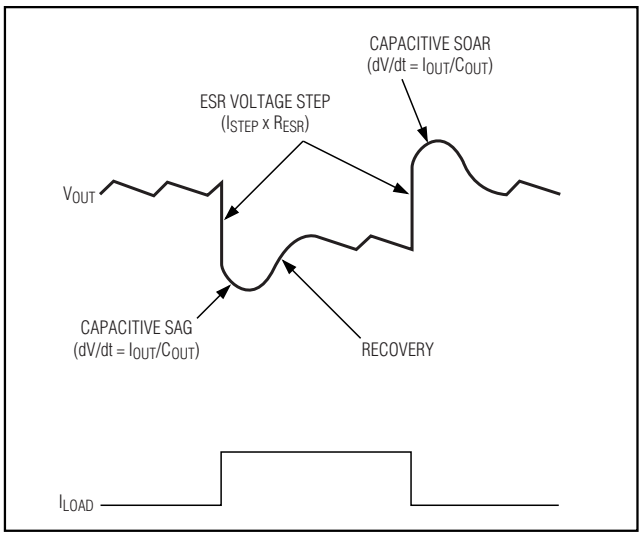


Figure 8. Transient Response Regions

output voltage of 1.55V and an output current of 21.3A. Given these values, CPU power consumption is reduced from 35.2W to 33.03W. The additional power consumption of R_{SENSE} is:

$$50mV \times 21.3A = 1.06W,$$

which results in an overall power savings of:

$$35.2W - (33.03W + 1.06W) = 1.10W.$$

In effect, 2.2W of CPU dissipation is saved and the power supply dissipates much of the savings, but both the net savings and the transfer of dissipation away from the hot CPU are beneficial. Effective efficiency is defined as the efficiency required of a nonvoltage-positioned circuit to equal the total dissipation of a voltage-positioned circuit for a given CPU operating condition.

Calculate effective efficiency as follows:

1) Start with the efficiency data for the positioned circuit (V_{IN}, I_{IN}, V_{OUT}, I_{OUT}).
2) Model the load resistance for each data point:

$$R_{LOAD} = V_{OUT} / I_{OUT}$$

3) Calculate the output current that would exist for each R_{LOAD} data point in a nonpositioned application:

$$I_{NP} = V_{NP} / R_{LOAD}$$

where V_{NP} = 1.6V (in this example).

4) Calculate effective efficiency as:

   Effective efficiency = $(V_{NP} \times I_{NP}) / (V_{IN} \times I_{IN})$ = calculated nonpositioned power output divided by the measured voltage-positioned power input.

5) Plot the efficiency data point at the nonpositioned current, I_{NP}.

The effective efficiency of voltage-positioned circuits is shown in the *Typical Operating Characteristics*.

One-Stage (Battery Input) Versus Two-Stage (5V Input) Applications

The MAX1887/MAX1897 can be used with a direct battery connection (one stage) or can obtain power from a regulated 5V supply (two-stage). Each approach has advantages, and careful consideration should go into the selection of the final design.

The one-stage approach offers smaller total inductor size and fewer capacitors overall due to the reduced demands on the 5V supply. Due to the high input voltage, the one-stage approach requires lower DC input currents, reducing input connection/bus requirements and power dissipation due to input resistance. The transient response of the single stage is better due to the ability to ramp the inductor current faster. The total efficiency of a single stage is better than the two-stage approach.

The two-stage approach allows flexible placement due to smaller circuit size and reduced local power dissipation. The power supply can be placed closer to the CPU for better regulation and lower I^2R losses from PC board traces. Although the two-stage design has slow-

er transient response than the single stage, this can be offset by the use of a voltage-positioned converter.

Ceramic Output Capacitor Applications

Ceramic capacitors have advantages and disadvantages. They have ultra-low ESR and are noncombustible, relatively small, and nonpolarized. However, they are also expensive and brittle, and their ultra-low ESR characteristic can result in excessively high ESR zero frequencies. In addition, their relatively low capacitance value can cause output overshoot when stepping from full-load to no-load conditions, unless a small inductor value is used (high switching frequency), or there are some bulk tantalum or electrolytic capacitors in parallel to absorb the stored inductor energy. In some cases, there may be no room for electrolytics, creating a need for a DC-DC design that uses nothing but ceramics.

The MAX1887/MAX1897 can take full advantage of the small size and low ESR of ceramic output capacitors in a voltage-positioned circuit. The addition of the positioning resistor increases the ripple at FB, lowering the effective ESR zero frequency of the ceramic output capacitor.

Output overshoot (V_{SOAR}) determines the minimum output capacitance requirement (see *Output Capacitor Selection*). Often the switching frequency is increased to 550kHz, and the inductor value is reduced to minimize the energy transferred from inductor to capacitor during load-step recovery. The efficiency penalty for operating at 550kHz is about 3% when compared to the 300kHz circuit, primarily due to the high-side MOSFET switching losses.

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 9). If possible, mount all of the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

1) Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation
2) Connect all analog grounds to a separate solid copper plane, which connects to the GND pin of the MAX1887/MAX1897. This includes the V_{CC} bypass capacitor, COMP components, and the resistive-divider connected to ILIM.
3) The master controller also should have a separate analog ground. Return the appropriate noise sensitive components to this plane. Since the reference in the master is sometimes connected to the slave, it may be necessary to couple the analog ground in the master to the analog ground in the slave to prevent ground offsets. A low value (≤10Ω) resistor is sufficient to link the two grounds.
4) Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
5) Keep the high-current gate-driver traces (DL, DH, LX, and BST) short and wide to minimize trace resistance and inductance. This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents.
6) CS+, CS-, CM+, and CM- connections for current limiting and balancing must be made using Kelvin sense connections to guarantee the current-sense accuracy.
7) When trade-offs in trace lengths must be made, it's preferable to allow the inductor charging path to be made longer than the discharge path. For example, it's better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
8) Route high-speed switching nodes away from sensitive analog areas (COMP, ILIM). Make all pin-strap control input connections ($\overline{SHDN}$, ILIM, POL) to analog ground or V_{CC} rather than power ground or V_{DD}.

Layout Procedure

1) Place the power components first, with ground terminals adjacent (low-side MOSFET source, C_{IN}, C_{OUT}, and D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET. The DL gate trace must be short and wide (50mils to 100mils wide if the MOSFET is 1 inch from the controller IC).
3) Group the gate-drive components (BST diode and capacitor, V_{DD} bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in Figure 1. This diagram can be viewed as

Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

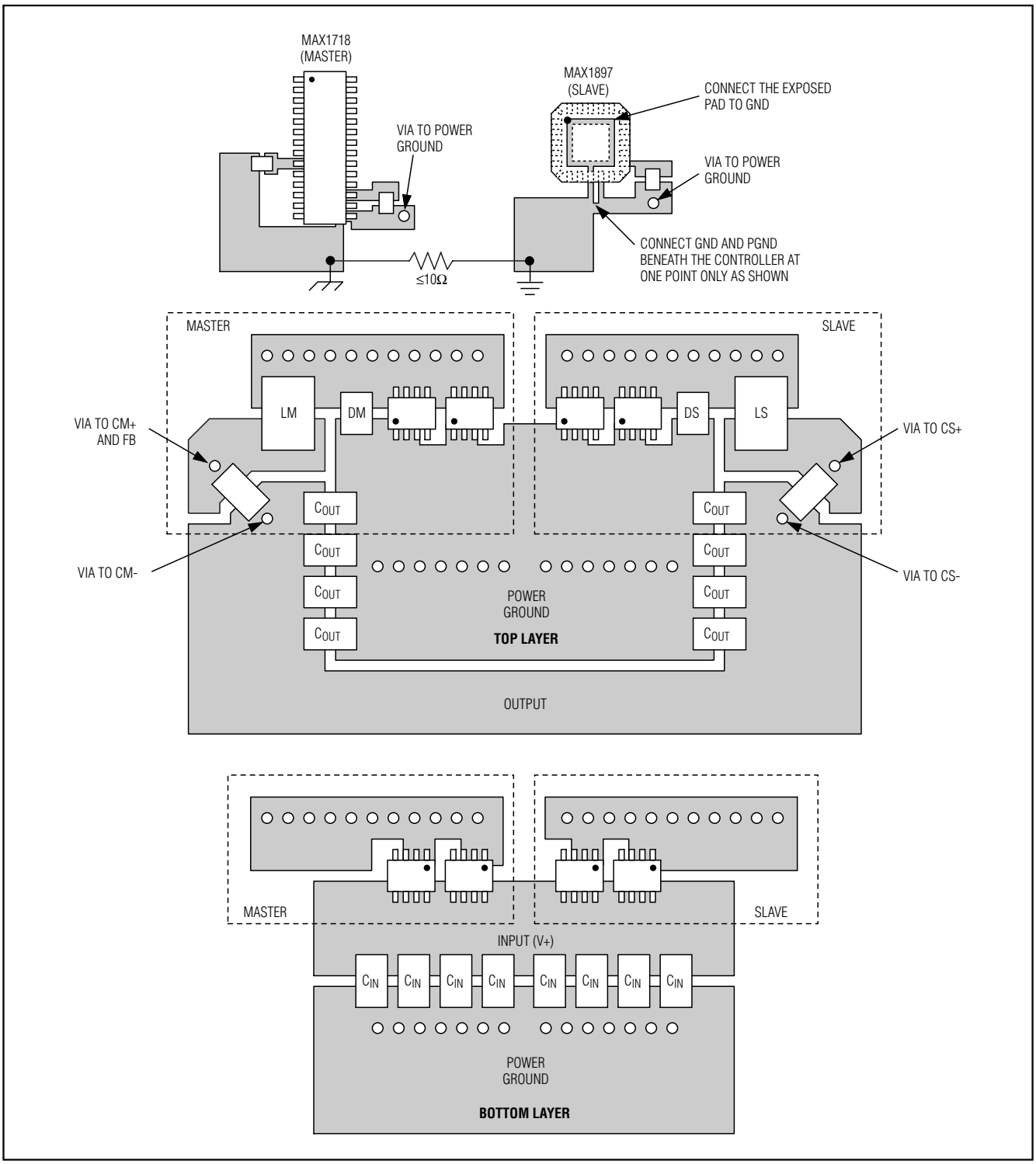
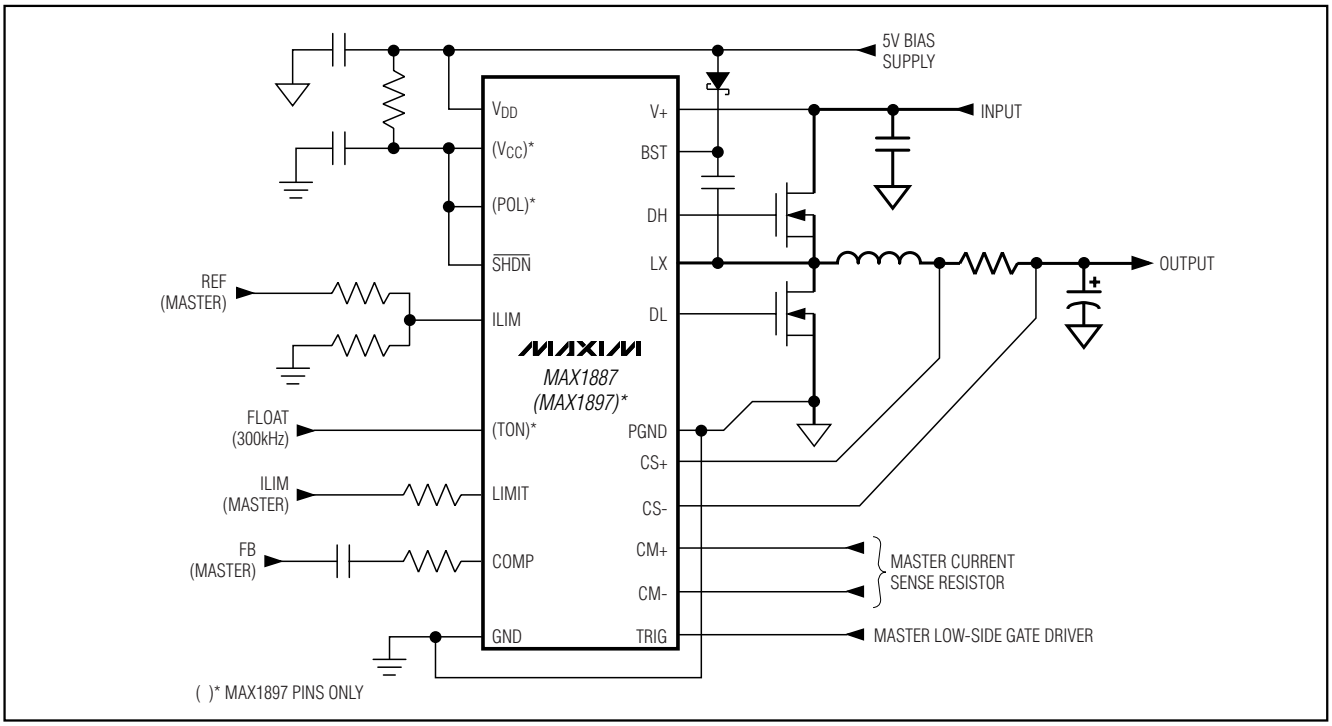


Figure 9. Power-Stage PC Board Layout Example

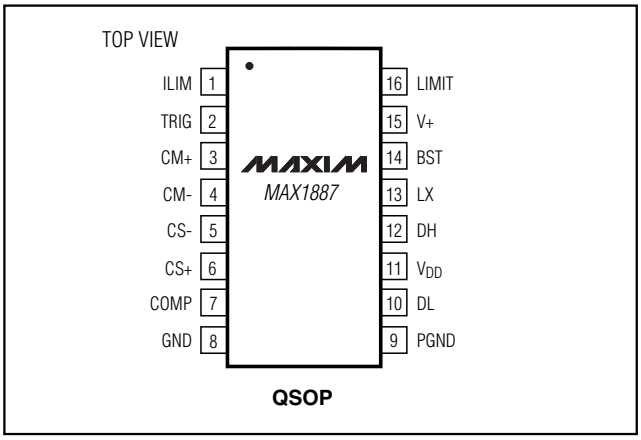
Typical Operating Circuit



having four separate ground planes: input/output ground, where all the high-power components go; the power ground plane, where the PGND pin and V_{DD} bypass capacitor go; the master's analog ground plane where sensitive analog components, the master's GND pin and V_{CC} bypass capacitor go; and the slave's analog ground plane where the slave's GND pin, and V_{CC} bypass capacitor go. The master's GND plane must meet the PGND plane only at a single point directly beneath the IC. Similarly, the slave's GND plane must meet the PGND plane only at a single point directly beneath the IC. The respective master and slave ground planes should connect to the high-power output ground with a short metal trace from PGND to the source of the low-side MOSFET (the middle of the star ground). This point must also be very close to the output capacitor ground terminal.

5) Connect the output power planes (V_{CORE} and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the CPU as is practical.

Pin Configurations (continued)



Chip Information

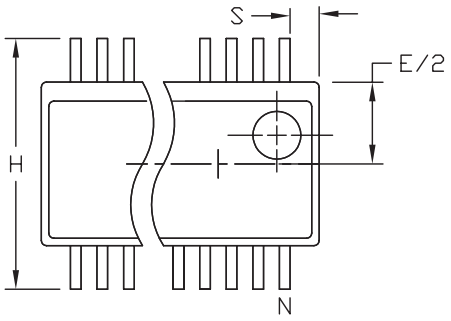
TRANSISTOR COUNT: 1422

PROCESS: BiCMOS

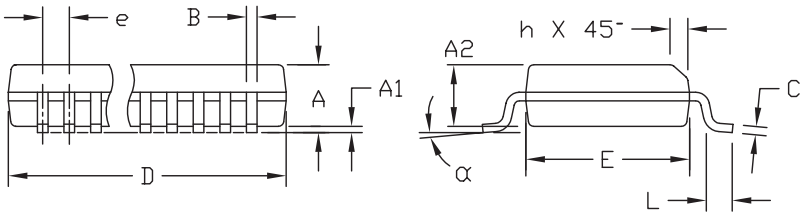
Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

Package Information

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		

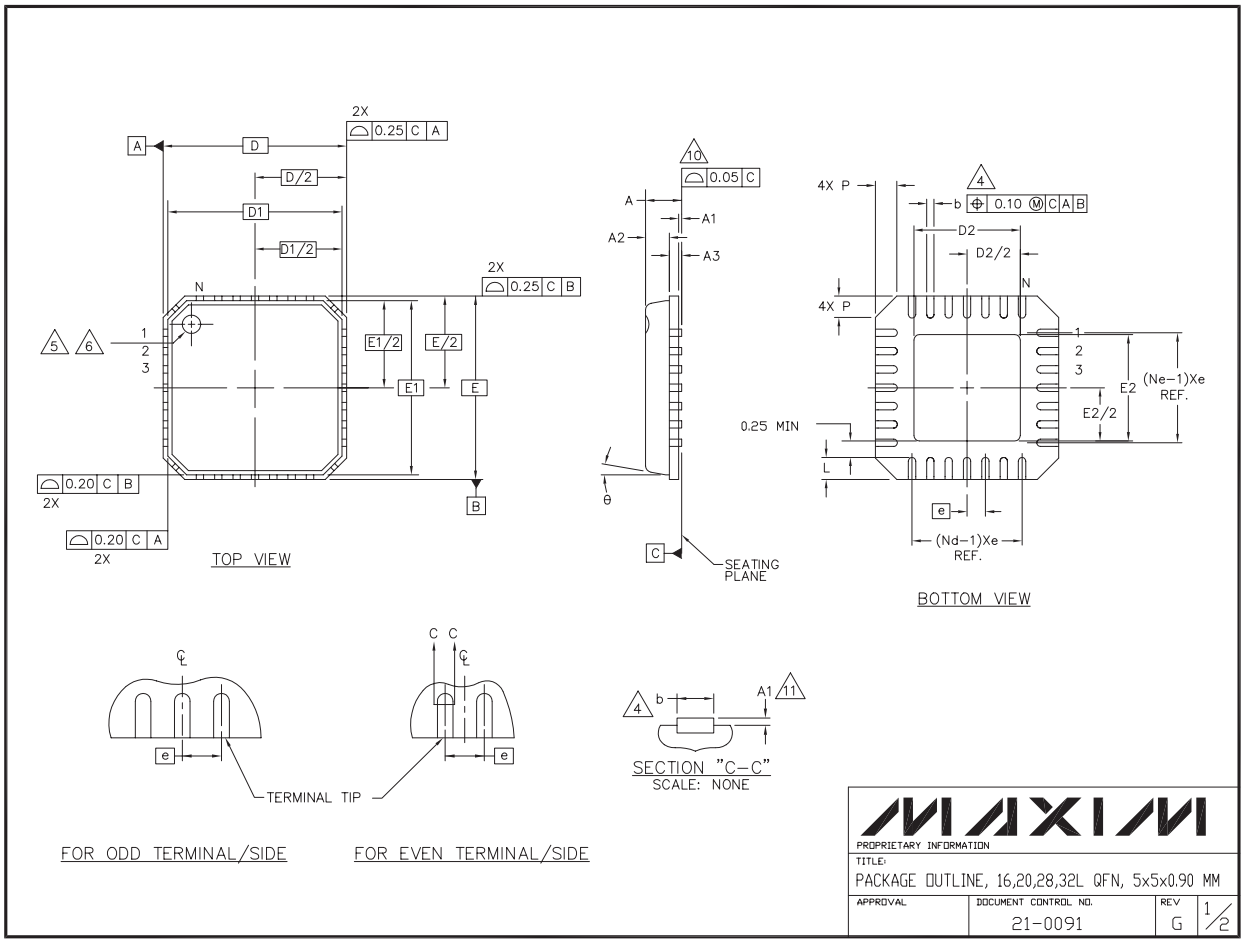
NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	D	1/1

Package Information (continued)



Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies

Package Information (continued)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/ LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES) AND TO SAW SINGULATION (STRAIGHT SIDES) QFN STYLES.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	1.00	
A3		0.20 REF.		
D		5.00 BSC		
D1		4.75 BSC		
E		5.00 BSC		
E1		4.75 BSC		
θ	0°	–	12°	
P	0		0.60	
D2	1.25	–	3.25	
E2	1.25	–	3.25	

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e		0.80 BSC		
N		16		3
Nd		4		3
Ne		4		3
L	0.35	0.55	0.75	
b	0.28	0.33	0.40	4

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e		0.65 BSC		
N		20		3
Nd		5		3
Ne		5		3
L	0.35	0.55	0.75	
b	0.23	0.28	0.35	4

SYMBOL	PITCH VARIATION C			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		28		3
Nd		7		3
Ne		7		3
L	0.35	0.55	0.75	
b	0.18	0.23	0.30	4

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		32		3
Nd		8		3
Ne		8		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0091	G	2/2