SCOPE: Complete, 8-Channel, 12-Bit Data Acquisition Systems

Device Type	Generic Number		
01	MAX180AM(x)/883B	04	MAX181AM(x)/883B
02	MAX180BM(x)/883B	05	MAX181BM(x)/883B
03	MAX180CM(x)/883B	06	MAX181CM(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
JL	GDIP1-T40	40 LEAD CERDIP	J40
DL	CDIP2-T40	40-Pin SIDEBRAZE	D40

Absolute Maximum Ratings

V_{DD} to DGND ..... -0.3V to +7V
V_{SS} to DGND ..... -0.3V to -17V
AGND to DGND ..... -0.3V to (V_{DD} +0.3V)
AIN_, MUXOUT, ADCIN, REFADJ, OFFADJ to REFIN ..... -0.3V to (V_{DD} +0.3V)
OFFADJ to REFIN ..... -0.3V to (V_{DD} +0.3V)
REFIN to DGND ..... +0.3V to (V_{SS} -0.3V)

$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, CLK A2-A0, BIP, DIFF, HBEN to DGND..... -0.3V to (V_{DD} +0.3V)

$\overline{BUSY}$, D0-D11 to DGND ..... -0.3V to (V_{DD} +0.3V)

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +160°C

Continuous Power Dissipation ..... T_A=+70°C
40 pin CERDIP(derate 20mW/°C above +70°C) 1600mW
40 pin Sidebraze(derate 25mW/°C above +70°C) 2000mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
40 pin CERDIP..... 25°C/W
40 pin Sidebraze ..... 15°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
40 pin CERDIP..... 50°C/W
40 pin Sidebraze ..... 40°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Supply Voltage (V_{CC})..... +4.75V to +5.25V
Supply Voltage (V_{SS})..... -11.4V to -15.75V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V_{DD}=+5V±5%, V_{SS}=-12V ±5% or -15V±5%, REFIN=-5V, f_{CLK}=1.6MHz 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
ACCURACY 2/							
Resolution	N			All	12		Bits
Integral Nonlinearity	INL		1,2,3	01,04		±0.5	LSB
				02,03, 05,06		±1.0	
Differential Nonlinearity	DNL		1,2,3	All		±1.0	LSB
Unipolar Offset Error	V_{OS}	NOTE 3	1,2,3	All		±4.0	LSB
Bipolar Offset Error	AE	NOTE 3	1,2,3	All		±6.0	LSB
Unipolar Gain Error			1,2,3	All		±10.0	LSB
Bipolar Gain Error			1,2,3	All		±15.0	LSB
Gain Error Tempco		NOTE 4,5		All		±5.0	ppm/°C
DYNAMIC TESTS		NOTE 2					
Signal-to-Noise Plus Distortion Ratio	SINAD	10kHz input signal, 100kHz sampling rate, bipolar mode	9	All	70		dB
Total Harmonic Distortion	THD	10kHz input signal, 100kHz sampling rate, bipolar mode. Up to the 5th harmonic.	9	All		-80	dB
Spurious Free Dynamic Range	SFDR		9	All	80		dB
Full-Power Sampling Bandwidth NOTE 5		In track mode, under-sampled waveform		All		6	MHz
Track-and-Hold Acquisition Time	t_{ACQ}	NOTE 5		All	1.875		µs
Conversion Time	t_{CONV}	Asynchronous hold mode Note 5		All	7.500	8.125	µs
		ROM Slow-Memory and I/O Port Modes; 15-16 clock cycles	9,10,11		9.375	10.0	
ANALOG INPUT							
Voltage Range		AIN_, MUXOUT, and ADCIN	1,2,3	All	REFIN	V_{DD}	V
Unipolar, Single-Ended Range		AIN_ to AGND	1,2,3	All	0	5.0	V
Unipolar, Differential Range		AIN_+ to AIN_-	1,2,3	All	0	5.0	V
Bipolar, Single-Ended Range		AIN_ to AGND	1,2,3	All	-2.5	2.5	V
Bipolar, Differential Range		AIN_+ to AIN_-	1,2,3	All	-2.5	2.5	V
Input Current		AIN_	1,2,3	01,02,03		±1.0	µA
Input Current		ADCIN_	1,2,3	04,05,06		±0.1	µA
Mux-On Resistance	R_{ON}	AIN_=2.5V, I_{MUXOUT}=1.25mA	1,2,3	04,05,06		2	kΩ
Mux-On Leakage Current	I_{ON}	AIN_=MUXOUT=±5V	1,2,3	04,05,06		±100	nA
Mux-Off Leakage Current	I_{IN}(OFF) I_{OUT}(OFF)	AIN_=±5V, V_{OUT}=±5V AIN_=±5V, V_{OUT}=±5V	1,2,3	04,05,06		±100	nA

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V_{DD}=+5V±5%, V_{SS}=-12V ±5% or -15V±5%, REFIN=-5V, f_{CLK}=1.6MHz 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Input Capacitance 5/	CIN	AIN_, ADCIN MUXOUT		04,05,06		35 45	pF
REFERENCE INPUT							
Input Range		NOTE 5		All	-4.92	-5.08	V
Input Current			1,2,3	All		-2	mA
Input Resistance			1,2,3	All	2.5		kΩ
REFERENCE OUTPUT							
V_{REF} Output Voltage			1	All	-4.98	-5.02	V
V_{REF} Output Tempco		NOTE 6	1,2,3	01,02, 04,05		25	ppm/°C
V_{REF} Output Tempco		NOTE 6	1,2,3	03,06		45	ppm/°C
Load Regulation NOTE 7		0mA<I_{OUT}<5mA	1	All		1.0	mV/mA
REFADJ, OFFADJ							
Input Current		V_{REFADJ}, V_{OFFADJ}=V_{DD} to REFIN	1,2,3	All		±1	µA
Disable Threshold			1,2,3	All	4.5		V
REFADJ Adjustment Range		REFIN<REFADJ<AGND	1,2,3	All	±60		mV
OFFADJ Adjustment Range		REFIN<REFADJ<AGND	1,2,3	All	±15		LSB
LOGIC INPUTS							
Logic High Voltage	V_{IH}	MODE CLK, A2-A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DIFF, BIP, HBEN	1,2,3	All	4.5 2.4		V
Logic Low Voltage	V_{IL}	MODE CLK, A2-A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DIFF, BIP, HBEN	1,2,3	All		0.5 0.8	V
Input Mid-Level Voltage	V_{MID}	MODE	1,2,3	All	1.5	3.5	V
Input Floating Voltage	V_{FLT}	MODE NOTE 5		All		2.5	V
Input Current	I_{IN}	MODE	1,2,3	All		±100	µA
Input Current	I_{IN}	CLK, A2-A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DIFF, BIP, HBEN	1 2,3	All		±1 ±10	µA
Input Capacitance	C_{IN}	NOTE 5		All		15	pF
LOGIC OUTPUTS							
Output High Voltage	V_{OH}	I_{SOURCE}=360µA, D11-D0, RDY, BUSY	1,2,3	All	4.0		V
Output Low Voltage	V_{OL}	I_{SINK}=1.6mA, D11-D0, RDY, BUSY	1,2,3	All		0.4	V
Floating-State Leakage Current	I_{LKG}	D11-D0, V_{OUT}=0V to V_{DD}	1,2,3	All		±10	µA
Floating-State Output Capacitance NOTE 5	C_{OUT}		1,2,3			15	pF

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V_{DD}=+5V±5%, V_{SS}=-12V ±5% or -15V±5%, REFIN=-5V, f_{CLK}=1.6MHz 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
POWER REQUIREMENTS							
Supply Voltage NOTE 1	V_{DD}		1,2,3	All	4.75	5.25	V
	V_{SS}				-11.40	-15.75	
Supply Current	I_{DD}	V_{DD}=5V	1,2,3	All		7.0	mA
	I_{SS}	V_{SS}=-12V				10.0	
Power Dissipation	PD	V_{DD}=5V, V_{SS}=-15V	1,2,3	All		155	mW
Power-Supply Rejection with Internal Reference	PSR	Input near FS, V_{SS}=-12V, V_{DD}=4.75V to 5.25V	1,2,3	All		±1.0	LSB
Power-Supply Rejection with Internal Reference	PSR	Input near FS, V_{DD}=5V, V_{SS}=-14.25V to -15.75V	1,2,3	All		±0.5	LSB
Power-Supply Rejection with Internal Reference	PSR	Input near FS, V_{DD}=5V, V_{SS}=-11.4V to -12.6V	1,2,3	All		±0.5	LSB
TIMING		**NOTE 8**					
$\overline{CS}$ to $\overline{RD}$ Setup time	t_1	NOTE 5		All	0		ns
$\overline{CS}$ to $\overline{RD}$ Hold time	t_2		9,10,11	All	0		ns
$\overline{CS}$ to $\overline{WR}$ Setup time	t_3		9,10,11	All	0		ns
$\overline{CS}$ to $\overline{WR}$ Hold time	t_4	NOTE 5		All	0		ns
$\overline{WR}$ Low Pulse Width	t_5		9,10,11	All	120		ns
$\overline{WR}$ High Pulse Width	t_6	MODE=0 or 1, NOTE 5		All	200		ns
DATA IN to $\overline{WR}$ Setup Time	t_7		9 10,11	All	80 120		ns
DATA IN to $\overline{WR}$ Hold Time	t_8		9,10,11	All	0		ns
$\overline{WR}$ Rising to $\overline{BUSY}$ Delay	t_9	C_L=50pF, MODE=1	9 10,11	All		160 200	ns
$\overline{WR}$ Falling to $\overline{BUSY}$ Delay	t_{10}	C_L=50pF, MODE=open	9 10,11	All		220 280	ns
$\overline{RD}$ Low Pulse Width	t_{11}		9 10,11	All	100 150		ns
$\overline{RD}$ High Pulse Width	t_{12}	NOTE 5		All	200		ns
DATA IN to $\overline{RD}$ Setup Time	t_{13}		9 10,11	All	80 120		ns

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V_{DD}=+5V±5%, V_{SS}=-12V ±5% or -15V±5%, REFIN=-5V, f_{CLK}=1.6MHz 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
DATA IN to $\overline{RD}$ Hold Time	t_{14}		9,10,11	All	0		ns
$\overline{RD}$ to $\overline{BUSY}$ Fall Delay	t_{15}	C_L=50pF	9 10,11	All		150 200	ns
$\overline{RD}$ to Data Out Valid	t_{16}	C_L=100pF, NOTE 9	9 10,11	All		100 150	ns
$\overline{RD}$ to Data Out Three-State	t_{17}	NOTE 9, 10	9 10,11	All		50 75	ns
HBEN to $\overline{RD}$ or $\overline{WR}$ Setup Time	t_{18}		9 10,11	All	80 120		ns
HBEN to $\overline{RD}$ or $\overline{WR}$ Hold Time	t_{19}		9,10,11	All	0		ns
$\overline{CS}$ to $\overline{READY}$ Fall Delay	t_{20}	C_L=50pF	9 10,11	All		110 150	ns
$\overline{BUSY}$ to Data Out Valid	t_{21}	C_L=100pF, NOTE 9	9 10,11	All		125 170	ns
$\overline{CS}$, $\overline{RD}$, or $\overline{WR}$ to CLK Setup time for 15 clock conversion	t_{22}	NOTE 5		All	220		ns
$\overline{CS}$, $\overline{RD}$, or $\overline{WR}$ to CLK Setup time for 16 clock conversion	t_{23}	NOTE 5		All	0		ns

NOTE 1: Internal Reference Mode, Bipolar Mode, Slow-Memory Mode. Performance at power-supply tolerance limits guaranteed by power-supply rejection test.
NOTE 2: V_{DD}=+5V, V_{SS}=-15V, FS=+5V, REFIN=-5V.
NOTE 3: Typical change over temperture is ±1LSB.
NOTE 4: FS Tempco=ΔFS/ΔT, where ΔFS is full-scale change from 25°C to +125°C or -55°C.
NOTE 5: Guaranteed by design. Not subject to test.
NOTE 6: REFIN TC = ΔREFIN/ΔT, where ΔREFIN is reference voltage change from 25°C to +125°C or -55°C.
NOTE 7: Load current should remain constant during conversion. This current is in addition to the DAC input current.
NOTE 8: All inputs are 0V to +5V swing with t_R=t_F=5ns (10% to 90% of 5V) and timed from voltage level of +1.6V.
NOTE 9: t_{16} and t_{21} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
NOTE 10: t_{17} is defined as the time required for the data lines to change 0.5V when the circuit load is as shown in Figure 2.
FIGURES 1 and 2: See Commercial Datasheet.

Package	ORDERING INFORMATION:		
40 pin CERDIP	MAX180AMJL/883B	MAX180BMJL/883B	MAX180CMJL/883B
40 pin Sidebraze	MAX180AMDL/883B	MAX180BMDL/883B	MAX180CMDL/883B

Package	ORDERING INFORMATION:		
40 pin CERDIP	MAX181AMJL/883B	MAX181BMJL/883B	MAX181CMJL/883B
40 pin Sidebraze	MAX181AMDL/883B	MAX181BMDL/883B	MAX181CMDL/883B

TERMINAL CONNECTIONS:

	MAX180	MAX181	
1	AIN0	AIN0	Analog Input to the MUX, 0V to +5V Unipolar, -2.5V to +2.5V bipolar
2	AIN1	AIN1	Analog Input, 0V to +5V Unipolar
3	AIN2	AIN2	Analog Input
4	AIN3	AIN3	Analog Input
5	AIN4	AIN4	Analog Input
6	AIN5	AIN5	Analog Input
7	AIN6	MUXOUT	Multiplexer Output (MAX181)
8	AIN7	ADCIN	Analog Input to Track and Hold (MAX181)
9	REFIN	REFIN	Reference Input
10	AGND	AGND	Analog Ground
11	REFOUT	REFOUT	-5V Reference Output
12	REFADJ	REFADJ	-5V Reference Adjust. Connect to V_{DD} if not required.
13	OFFADJ	OFFADJ	Offset adjust. Connect to V_{DD} if not required.
14	MODE	MODE	Interface Mode Select pin.
15	V_{SS}	V_{SS}	Negative Supply, -12V or -15V.
16	D11	D11	Three-State Data Outputs, MSB=D11
17	D10	D10	Three-State Data Outputs
18	D9	D9	Three-State Data Outputs
19	D8	D8	Three-State Data Outputs
20	GND	GND	Digital Ground
21	D7	D7	Three-State Data Outputs, LSB=D0
22	D6	D6	Three-State Data Outputs
23	D5	D5	Three-State Data Outputs
24	D4	D4	Three-State Data Outputs
25	D3	D3	Three-State Data Outputs
26	D2	D2	Three-State Data Outputs
27	D1	D1	Three-State Data Outputs
28	D0	D0	Three-State Data Outputs
29	CLKIN	CLKIN	Clock Input, TTL/CMOS compatible
30	HBEN	HBEN	High-Byte Enable Input
31	$\overline{RD}$	$\overline{RD}$	$\overline{READ}$ Input
32	$\overline{WR}$	$\overline{WR}$	$\overline{WRITE}$ Input (MODE=1 or Open) $\overline{READY}$ Output (MODE=0)
33	$\overline{CS}$	$\overline{CS}$	$\overline{CHIP\text{-}SELECT}$ Input
34	$\overline{BUSY}$	$\overline{BUSY}$	$\overline{BUSY}$ Output
35	DIFF	DIFF	Single-Ended Mode: DIFF=0, Differential Mode: DIFF=1
36	BIP	BIP	Unipolar Mode: BIP=0, Bipolar Mode: BIP=1
37	A0	A0	Multiplexer Channel Address Input: A2=MSB, A0=LSB
38	A1	A1	Multiplexer Channel Address Input: A2=MSB, A0=LSB
39	A2	A2	Multiplexer Channel Address Input: A2=MSB, A0=LSB
40	V_{DD}	V_{DD}	Positive Supply, +5V Input (substrate connected to V_{DD})

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 4**, 9
Group A Test Requirements Method 5005	1, 2, 3, 4**, 9
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroup 4 shall be tested at initial qualification and upon redesign. Sample size will be 116 units.