RELIABILITY REPORT

FOR

MAX1714xEEx

PLASTIC ENCAPSULATED DEVICES

September 16, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX1714 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1714 pulse-width modulation (PWM) controller provides the high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high-voltage batteries to generate low-voltage CPU core or chip-set/RAM supplies in notebook computers.

Maxim's proprietary Quick-PWM™ quick-response, constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The MAX1714 achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Efficiency is further enhanced by an ability to drive very large synchronous-rectifier MOSFETs.

Single-stage buck conversion allows these devices to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, two-stage conversion (stepping down the +5V system supply instead of the battery) at a higher switching frequency allows the minimum possible physical size.

The MAX1714 is intended for CPU core, chipset, DRAM, or other low-voltage supplies as low as 1V. The MAX1714A is available in a 20-pin QSOP package and includes overvoltage protection. The MAX1714B is available in a 16-pin QSOP package with no overvoltage protection.

B. Absolute Maximum Ratings

Item	Rating
V+ to AGND (Note 1)	-0.3V to +30V
V_{DD}, V_{CC} to AGND (Note 1)	-0.3V to +6V
PGND to AGND (Note 1)	±0.3V
/SHDN, PGOOD, OUT to AGND (Note 1)	-0.3V to +6V
ILIM, FB, REF, /SKIP,TON to AGND (Notes 1,2)	-0.3V to (V_{CC} + 0.3V)
DL to PGND (Note 1)	-0.3V to (V_{DD} + 0.3V)
BST to AGND (Note 1)	-0.3V to +36V
DH to LX	-0.3V to (BST + 0.3V)
LX to BST	-6V to +0.3V
Storage Temp.	-65°C to +165°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
20 Lead QSOP	727mW
16 Lead QSOP	667mW
Derates above +70°C	
20 Lead QSOP	9.1mW/°C
16 Lead QSOP	8.3mW/°C

Note 1: /Skip may be forced below -0.3V, temporarily exceeding the absolute maximum rating, for the purpose of debugging prototype breadboards using the no-fault test mode. Limit the current drawn to -5mA maximum.

II. Manufacturing Information

A. Description/Function:	High-Speed, Digitaly adjusted Step-Down Controller for Notebook CPUs
B. Process:	12 (SG1.2) - Standard 1.2 micron silicon gate CMOS
C. Number of Device Transistors:	3675
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	October, 1998

III. Packaging Information

A. Package Type:	**20 Lead QSOP**	**16 Lead QSOP**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1101-0113	Buildhsheet # 05-1101-0126
H. Flammability Rating:	Class UL94-V0	Class UL94-V0

IV. Die Information

A. Dimensions:	105 X 79 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Si
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 240 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 4.52 \times 10^{-9}$ $\lambda = 4.52$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (#06-5425) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PX63Z-1 die type has been found to have all pins able to withstand a transient pulse of ±400V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX1714xEEx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		240	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	16-Pin QSOP 20-Pin QSOP		0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the package.
Note 2: Generic Package/Process data

Attachment #3

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

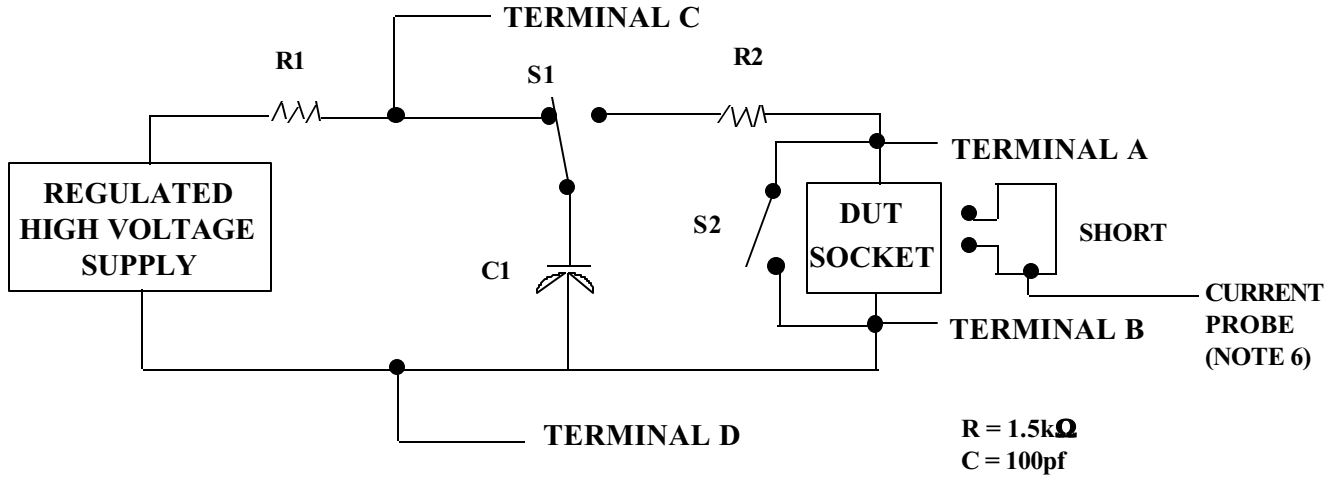
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

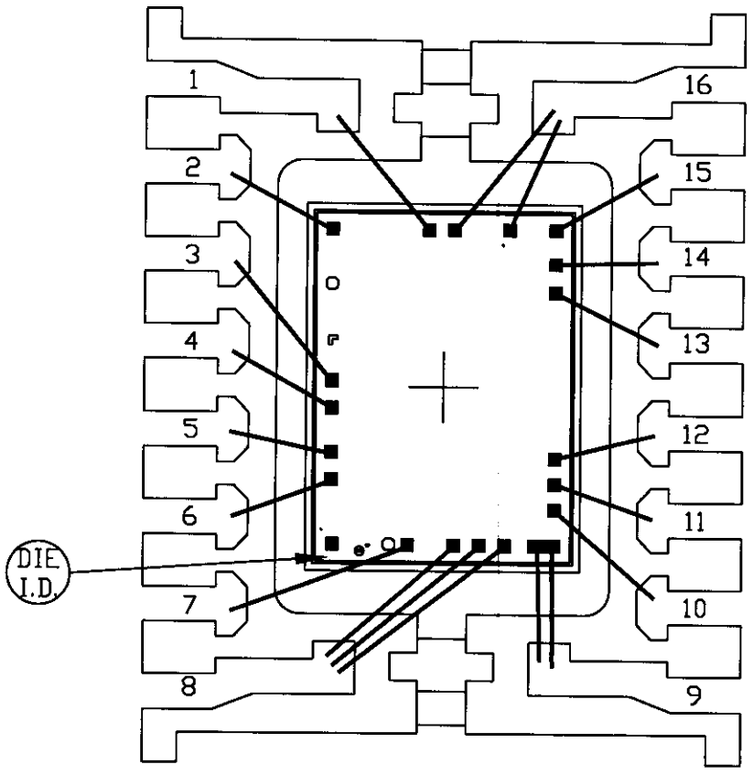
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

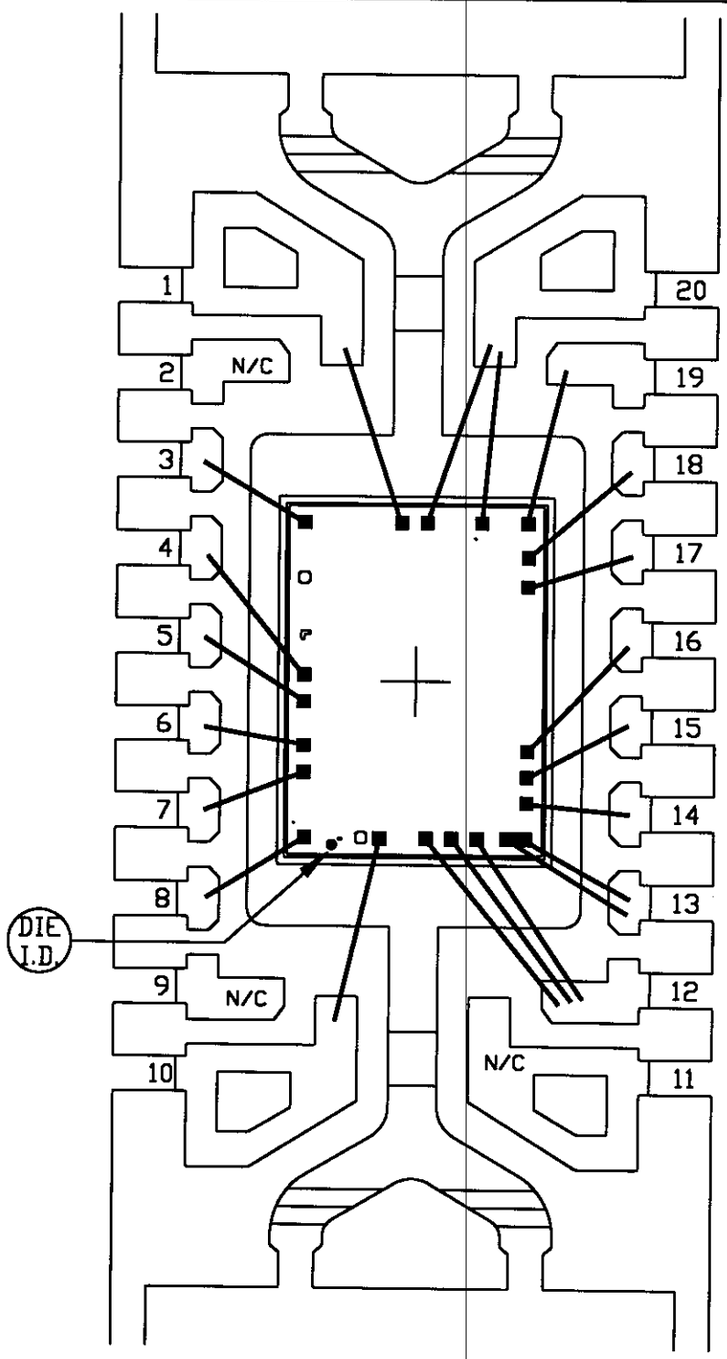
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.



c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



PKG.CODE: E16-1		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 96X130	PKG.		10/14/99	BUILDSHEET NUMBER: 05-1101-0126	REV.: B
	DESIGN		10/12/99		



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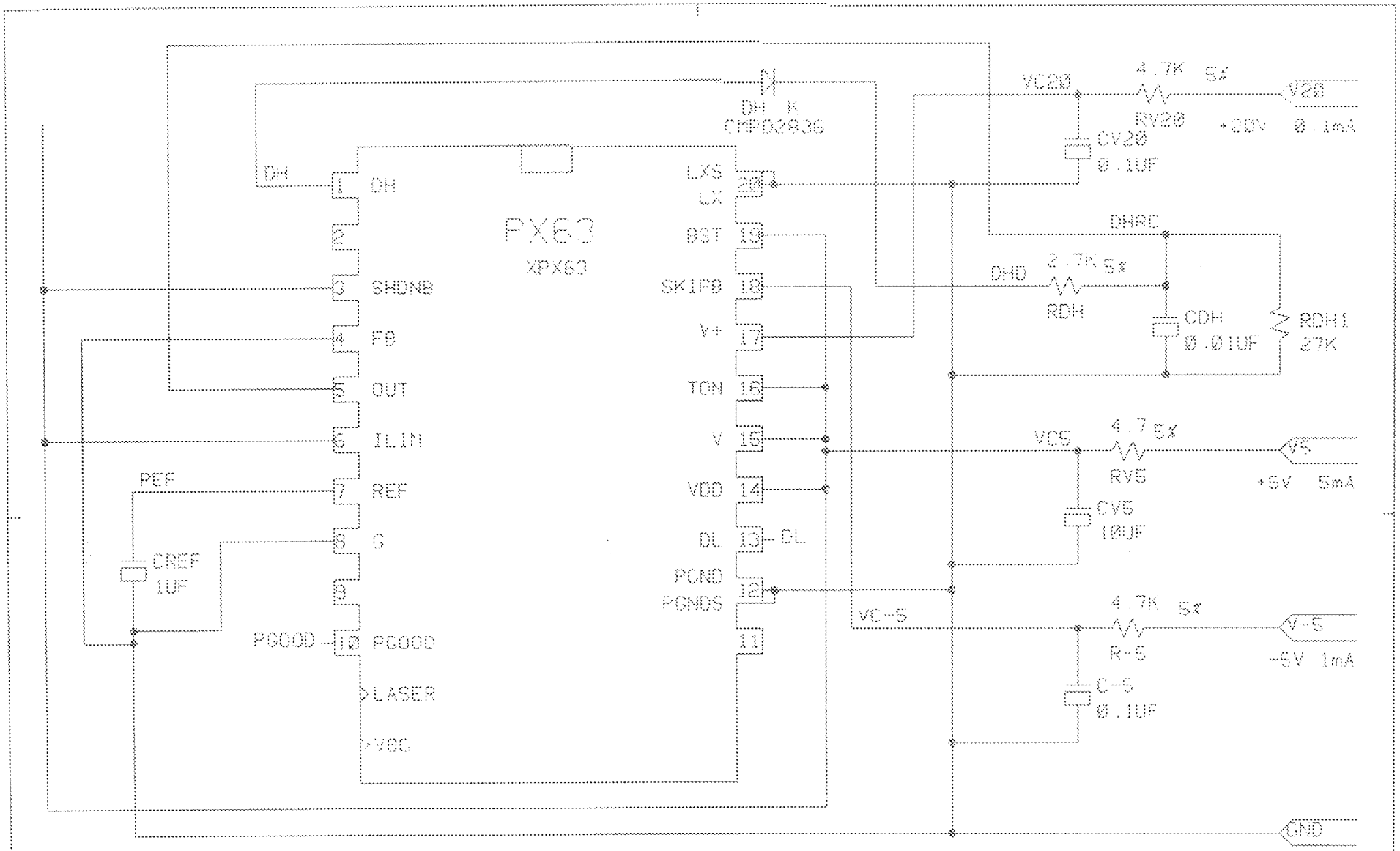
CAV./PAD SIZE: 96X140	PKG.	R.J.C	3/15/99	BUILDSHEET NUMBER: 05-1101-0113	REV.: B
	DESIGN	M. [illegible]	3/15/99		



MAXIM	CREATED: 12/31/97	BY: MC	ENG1: Mike Grimm	ENG2: —
	LAST SAVED: 08:58:01 05-25-99		SIZE A	REVISION 00/00/00
BBOARD	PROJECT: PX51			DWG NO: —
	DESC: BURN-IN BOARD		FILE: BBOARD.DRW	SHEET 1 OF 1