SCOPE: CMOS, 8-BIT, 8-CHANNEL DATA ACQUISITION SYSTEM

Device Type	Generic Number
01	MAX161A(x)/883B
02	MAX161B(x)/883B
03	MAX161C(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
JI	GDIP1-T28 or CDIP2-T28	28 LEAD CERDIP	J28
LI	CQCC1-N28	28 Leadless Carrier	LCC

Absolute Maximum Ratings

V_{DD} to AGND ..... +7V
V_{DD} to DGND..... +7V
AGND to DGND ..... -0.3V, V_{DD}
Clock Input Voltage to DGND ..... -0.3V to V_{DD}
Digital Input Voltage to DGND ..... -0.3V to V_{DD}
Digital Output Voltage to DGND ..... -0.3V to V_{DD}
V_{REF} to AGND ..... ±25V
V_{BOFS} to AGND ..... ±17V
V_{AINS} ..... ±17V

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
28 pin CERDIP(derate 16.7mW/°C above +70°C) 1333mW
28 pin LCC(derate 10.2mW/°C above +70°C) 816mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
28 pin CERDIP..... 25°C/W
28 pin LCC ..... 15°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
28 pin CERDIP..... 60°C/W
28 pin LCC ..... 98°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Reference Voltage, V_{REF} ..... -5V to -15V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V_{DD}=+5V, V_{REF}=-10V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
ACCURACY (At f_{CLK}=4MHz)							
Resolution	RES			All	8		Bits
Relative Accuracy	RA		1,2,3	01 02 03		±1.875 ±0.75 ±0.50	LSB
Differential Nonlinearity	DNL		1,2,3	01 02 03		±1.875 ±0.875 ±0.75	LSB
Offset Error	V_{OS}	NOTE 1 Adjustable to zero	1,2,3	01 02 03		±120 ±60 ±40	mV
Gain Error, Worst Channel	AE	NOTE 2 Adjustable to zero	1,2,3	01 02 03		±6 ±4 ±2	LSB
Gain Match Between Channels	AM	Figure 5. Adjustable to zero	1,2,3	01 02 03		±3 ±2 ±1	LSB
ANALOG INPUTS	RM						
Input Resistance	R_{IN}	At V_{REF}, B_{OFS}, $A_{IN.}$ NOTE 3 AIN7-AIN0	1,2,3	All	10	30	kΩ
V_{REF} (for specified performance)	V_{REF}		1,2,3	All	-10.5	-9.5	V
Nominal Analog Input Range		+Unipolar Mode -Unipolar Mode Bipolar Mode	1,2,3	All	0 $-V_{REF}$ $-V_{BOFS}$	$+V_{REF}$ 0 $\lvert V_{REF} \rvert$ $-V_{BOFS}$	V
DIGITAL INPUTS		$\overline{CS}$, ALE, CLK, A0-A2)					
Logic High Threshold	V_{IH}		1,2,3	All	+2.4		V
Logic Low Threshold	V_{IL}		1,2,3	All		+0.8	V
Input Leakage Current	I_{IN}	V_{IN}=0V or V_{DD}	1,2,3	All		+1.0	µA
Digital Input Capacitance	C_{IN}	NOTE 4	4	All		5.0	pF
DIGITAL OUTPUTS		(STAT, DB0-DB7)					
Output High Voltage	V_{OH}	I_{SOURCE}=40µA	1,2,3	All	4.5		V
Output Low Voltage	V_{OL}	I_{SINK}=1.6mA	1,2,3	All		0.6	V
Floating State Leakage	I_{LKG}	DB0-DB7	1 2,3	All		+10.0	µA
Floating State Capacitance	C_{OUT}	DB0-DB7, V_{OUT}=0V to V_{DD}	4	All		10.0	pF
POWER REQUIREMENTS							
Supply Voltage	V_{DD}		1,2,3	All	+4.5	+5.5	V
Supply Current	I_{DD}	Static Dynamic (f_{CLK}=4.0MHz)	1,2,3 4,5,6	All		5.0 5.0	mA
TIMING		CL=100pF					
ALE Pulse Width	t_H		9,10,11	All	50		ns
Address Valid to Latch Setup Time	t_{ALS}		9,10,11	All	45		ns

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V_{DD}=+5V, V_{REF}=-10V, CL=100pF Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Address Valid to Latch Hold Time	t_{ALH}		9,10,11	All	10		ns
__ Address Latch to CS Setup Time	t_{LCS}		9,10,11	All	10		ns
__ CS to Output Propagation Delay	t_{ACC}		9,10,11	All		200	ns
__ CS Pulse Width	t_{CW}		9,10,11	All	250		ns
__ CS to Output Float Propagation Delay	t_{CF}		9,10,11	All		50	ns
__ CS to Low Impedance	t_{CLZ}		9,10,11	All		100	ns
Clock Frequency	t_{CLK}	NOTE 5	9,10,11	All		4.0	MHz

NOTE 1: Typical offset temperature coefficient is ±25µV/°C.

NOTE 2: Gain error is measured after offset calibration. Maximum full scale change for any channel from 25°C to +125°C or -55°C is ±2LSBs.

NOTE 3: R_{BOFS}/R_{AIN} mismatch causes transfer function rotation about positive full scale. The effect is an offset and a gain term when using the circuits of Figures 7 and 9.

NOTE 4: Guaranteed but not 100% tested. Tested at initial release and redesign.

NOTE 5: Guaranteed conversion time for stated accuracy of 20µs/channel with 4.0MHz.

FIGURES 5, 7, 9: See Commercial Datasheet.

TRUTH TABLE FOR CHANNEL SELECTION:

A2	A1	A0	ALE	CHANNEL DATA TO BE READ
0	0	0	1	Channel 0
0	0	1	1	Channel 1
0	1	0	1	Channel 2
0	1	1	1	Channel 3
1	0	0	1	Channel 4
1	0	1	1	Channel 5
1	1	0	1	Channel 6
1	1	1	1	Channel 7

TERMINAL CONNECTIONS:

	28 PIN CDIP/LCC		28PIN CDIP/LCC		28PIN CDIP/LCC		28PIN CDIP/LCC
1	B_{OFS}	8	A_{IN1}	15	CLK	22	DB5
2	A_{IN7}	9	A_{IN0}	16	ALE	23	DB4
3	A_{IN6}	10	V_{REF}	17	A0	24	DB3
4	A_{IN5}	11	AGND	18	A1	25	DB2
5	A_{IN4}	12	_____ STAT	19	A2	26	DB1
6	A_{IN3}	13	___ CS	20	DB7 (MSB)	27	DB0(LSB)
7	A_{IN2}	14	DGND	21	DB6	28	V_{DD}

Package		ORDERING INFORMATION:	
28 pin CERDIP	MAX161AMJI/883B	MAX161BMJI/883B	MAX161CMJI/883B
28 pin LCC	MAX161AMLI/883B	MAX161BMLI/883B	MAX161CMLI/883B

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 4, 5, 6, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 4, 5, 6, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.