RELIABILITY REPORT

FOR

MAX1481xUB

PLASTIC ENCAPSULATED DEVICES

November 7, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX1481 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description
II.Manufacturing Information
III.Packaging Information
IV.Die Information

I. Device Description

A. General

The MAX1481 provides software-selectable, full duplex, low-power, slew-rate-limited, and high speed (12Mbps) RS-485/RS-422 operation.

The MAX1481 is designed for space-constrained, full-duplex RS-422 applications.

This part contains one driver and one receiver and features a 1/8-unit-load receiver input impedance, allowing up to 256 transceivers on the bus. The MAX1481 features reduced-slew-rate driver that minimizes EMI and reduces reflections caused by improperly terminated cables, allowing error-free data transmission up to 250kbps.

The MAX1481 draws only 300μA of supply current. This device has a low-power shutdown mode that reduces supply current to only 0.1μA. This device operates from a single 5V supply.

The MAX1481's driver is output short-circuit current limited and is protected against excessive power dissipation by thermal-shutdown circuitry that places the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

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B. Absolute Maximum Ratings

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<u>item</u>	Rating
Supply Voltage (V _{CC})	+7V
Control Input Voltage (/RE, DE, H//F)	$-0.3V$ to $(V_{CC} + 0.3V)$
Driver Input Voltage (DI)	$-0.3V$ to $(V_{CC} + 0.3V)$
Driver Output Voltage (A, B, Y, Z)	-8V to +12.5V
Receiver Input Voltage, Half Duplex (Y, Z)	-8V to +12.5V
Receiver Input Voltage, Full Duplex (A, B)	-8V to +12.5V
Receiver Output Voltage (RO)	$-0.3V$ to $(V_{CC} + 0.3V)$
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
10-Pin uMax	444mW
Derates above +70°C	
10-Pin uMax	5.6mW/°C

II. Manufacturing Information

A. Description/Function: Software-Selectable, Full-Duplex, Slew-Rate-Limited, 12Mbps, RS-485/RS-422 Transceiver

B. Process: SG3 - Standard 3 micron silicon gate CMOS

C. Number of Device Transistors: 396

D. Fabrication Location: California or Oregon, USA

E. Assembly Location: Philippines, Thailand or Malaysia

F. Date of Initial Production: April, 1997

III. Packaging Information

A. Package Type: 10 Lead Micro Max (μΜΑΧ)

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-1901-0171

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity

per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 87 x 61 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 3 microns (as drawn)

F. Minimum Metal Spacing: 3 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)

Bryan Preeshl (Executive Director of QA)

Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 320 \times 2}$$
 (Chi square value for MTTF upper limit)
$$\lambda = 3.39 \times 10^{-9}$$
 Temperature Acceleration factor assuming an activation energy of 0.8eV
$$\lambda = 3.39 \times 10^{-9}$$

$$\lambda = 3.39 \text{ F.I.T.}$$
 (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5308) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1L).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The RS57 die type has been found to have all pins able to withstand a transient pulse of ± 2000 V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 150 mA and/or ± 20 V.

Table 1Reliability Evaluation Test Results

MAX1481xUB

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Tes	t (Note 1)			
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	320	0
Moisture Testi	ng (Note 2)			
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality (generic test vehicle)	299	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality (generic test vehicle)	77	0
Mechanical Str	ress (Note 2)			
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Micro Max package.

Note 2: Generic Package/Process Data

TABLE II. Pin combination to be tested. 1/2/

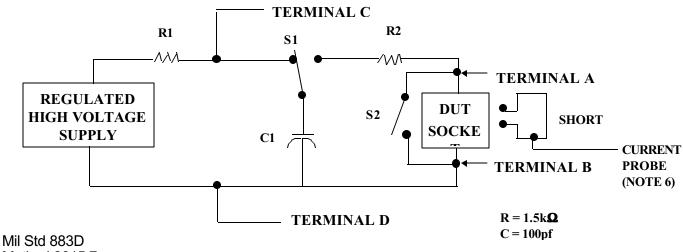
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} 3/	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- 3/ Repeat pin combination I for each named Power supply and for ground

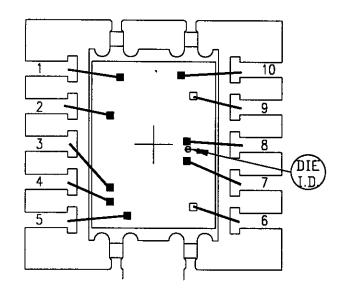
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{S1}, or V_{S2} or V_{S3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D Method 3015.7 Notice 8



PKG.CODE: U10-2		APPROVALS	DATE	NIXIXI	/VI
CAV./PAD SIZE:	PKG.	RAJ. C	5/21/98	BUILDSHEET NUMBER:	REV:
68X94	DESIGN	Polen	5-22-98	05-1901-0171	В

