RELIABILITY REPORT

FOR

MAX1293xxEx

PLASTIC ENCAPSULATED DEVICES

August 7, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX1293 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1293 low-power, 12-bit analog-to-digital converters (ADCs) feature a successive-approximation ADC, automatic power-down, fast wake-up (2µs), an on-chip clock, +2.5V internal reference, and a high-speed, byte-wide parallel interface. It operates with a single +3V analog supply and feature a V_{LOGIC} pin that allows it to interface directly with a +1.8V to +5.5V digital supply.

Power consumption is only 5.7mW ($V_{DD} = V_{LOGIC}$) at the maximum sampling rate of 250ksps. Two software-selectable power-down modes enable the MAX1293 to be shut down between conversions; accessing the parallel interface returns it to normal operation. Powering down between conversions can cut supply current to under 10µA at reduced sampling rates.

The MAX1293 offers software-configurable analog inputs for unipolar/bipolar and single-ended/pseudo-differential operation. In single-ended mode, the MAX1293 has 4 input channels (2 input channels, when in pseudo-differential mode).

Excellent dynamic performance and low power combined with ease of use and small package size make this converter ideal for battery-powered and data-acquisition applications or for other circuits with demanding power consumption and space requirements.

The MAX1293 is available in a 24-pin QSOP. For pin-compatible +5V, 12-bit versions, refer to the MAX1290/MAX1292 data sheet.

B. Absolute Maximum Ratings

Item	Rating
V_{DD} to GND	-0.3V to +6V
Vlogic to GND	-0.3V to 6V
CH0-CH7, COM to GND	-0.3V to (V_{DD} + 0.3V)
REF, REFADJ to GND	-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND	-0.3V to +6V
Dgital Output to GND	-0.3V to (Vlogic +0.3V)
Continuous Power Dissipation ($T_A = +70^0C$)	
Storage Temp.	-65°C to +150°C
Lead Temp. (soldering, 10 sec.)	+300°C
Power Dissipation	
24 Lead QSOP	762mW
Derates above +70°C	
24 Lead QSOP	9.5mW/°C

II. Manufacturing Information

A. Description/Function: +2.7V to +5.25V, Low-Power, 10-Bit Serial ADC

B. Process: S12 (SG1.2) - Standard 1.2 micron silicon gate CMOS

C. Number of Device Transistors: 5781

D. Fabrication Location: California or Oregon, USA

E. Assembly Location: Thailand

F. Date of Initial Production: October, 1999

III. Packaging Information

A. Package Type: **24 Lead QSOP**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-0101-0489

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 85 x 110 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Si

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn)

F. Minimum Metal Spacing: 1.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliability Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83 \text{ (Chi square value for MTTF upper limit)}}{192 \times 4389 \times 160 \times 2}$$

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 6.69 \times 10^{-9}$ $\lambda = 6.79$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5426) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L)**.

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AD92 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1

Reliability Evaluation Test Results

MAX1293xxEx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	160	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	280	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Small Outline package.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

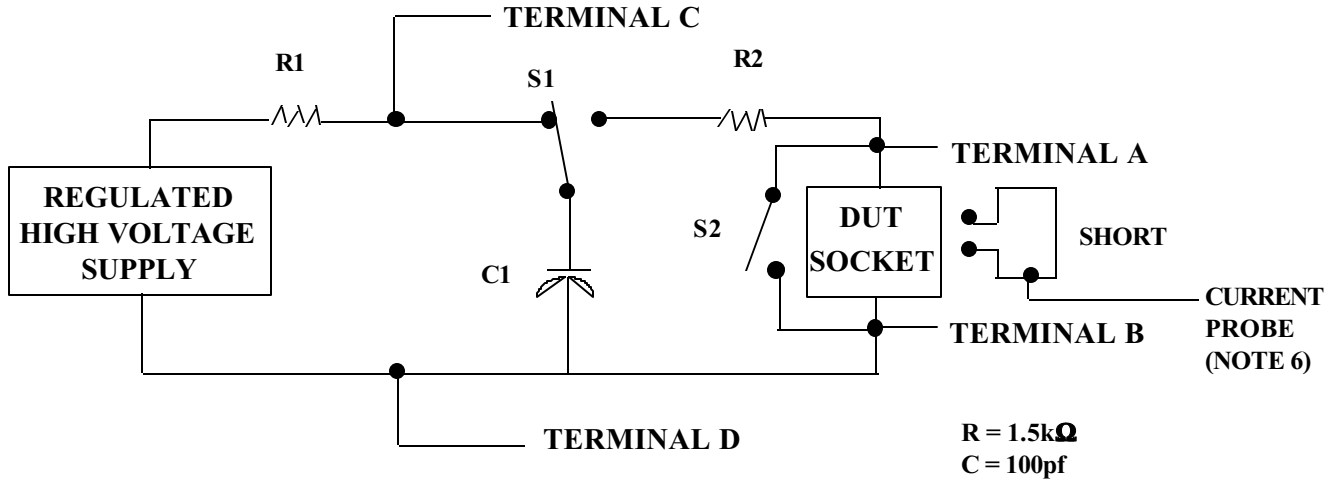
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

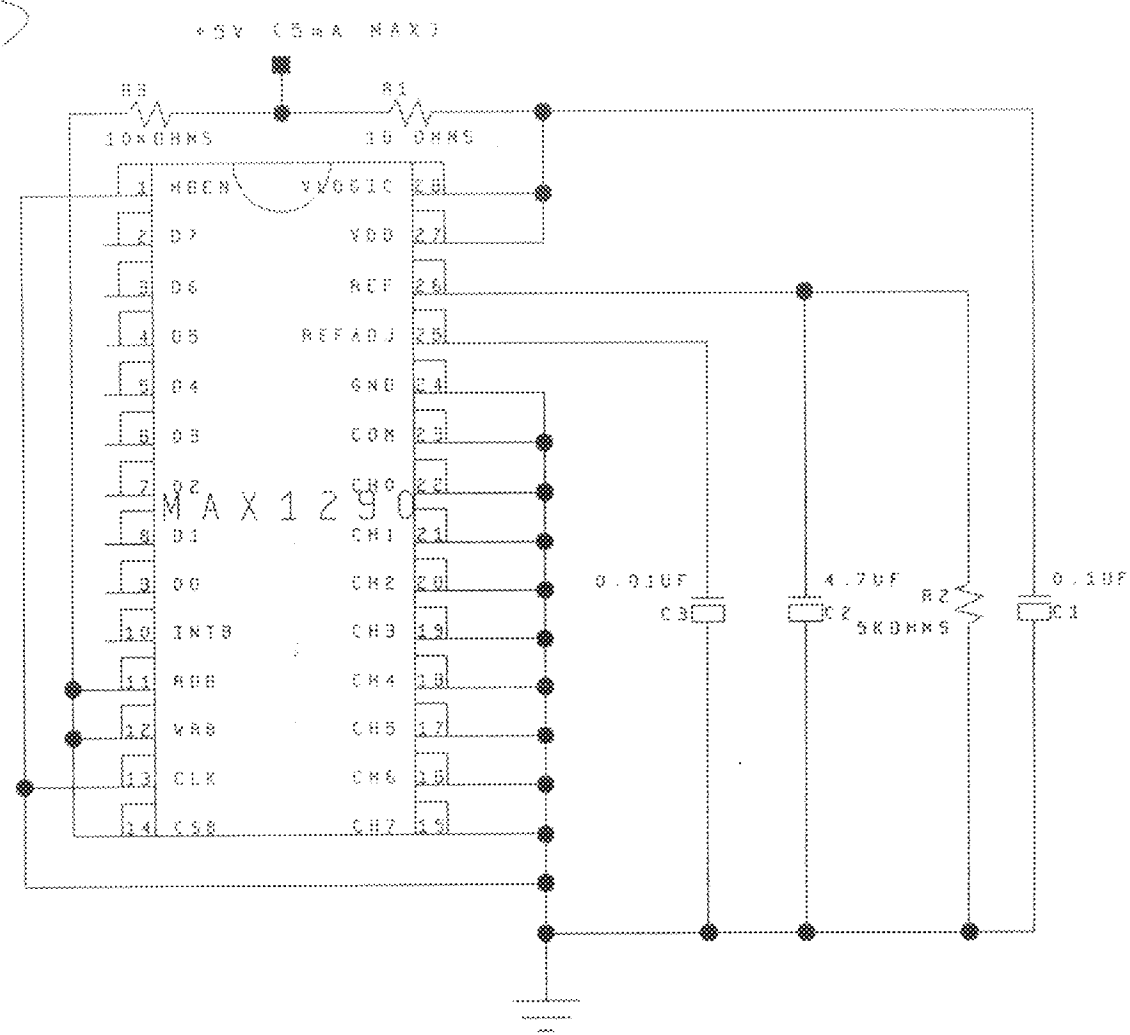
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Use MAX1290AEEI
28-pin QSOP
Chad Steward
x6960
7/2/99



NOTE:
1. Max power dissipation is 25mW per package.
2. All resistors are 1/4W, +/-5%.
3. Burn-in board may use fuses in supply lines for multiple packages.

06-5426

MAXIM CONFIDENTIAL	CREATED: 00/00/00	BY: CTS	ENG1: CHAD STEWARD	ENG2: RAMIN CHOWDHURY
	LAST SAVED: 7-2-1999_17:32	SIZE A	REVISION A 00/00/00	DWG NO. --
BID28	PROJECT: AD92Z			
	DESC.: BURN-IN BOARD 28-PIN	PACKAGE: bb1230		SHEET 1 OF 1