GEC PLESSEY
SEMICONDUCTORS

MARCH 1995
PRELIMINARY INFORMATION
DS3826-3.6

MA31754

PERIPHERAL SUPPORT CHIP (PSC)

The MA31754 is a Peripheral Support Chip (PSC) designed to provide those features which are commonly required in an MA31750 processor system. It can be used to replace much of the external logic associated with wait state generation, bus arbitration and address decoding. This reduces the power consumption, weight, complexity and cost of the system, whilst increasing its performance and overall reliability.

FEATURES

- Radiation Hard CMOS SOS Technology
- Versatile Decoding Scheme for IO Address Space
- Support for Non-Volatile Memory Management Including On-Circuit Board Programming/Reprogramming
- System Bus Arbiter and Ready State Generator
- Support for EDAC Testing
- Independent Watchdog Timer
- On-Board Mission Timer and Real Time Clock Function
- System Reset Generator
- Two Simple Serial Interfaces

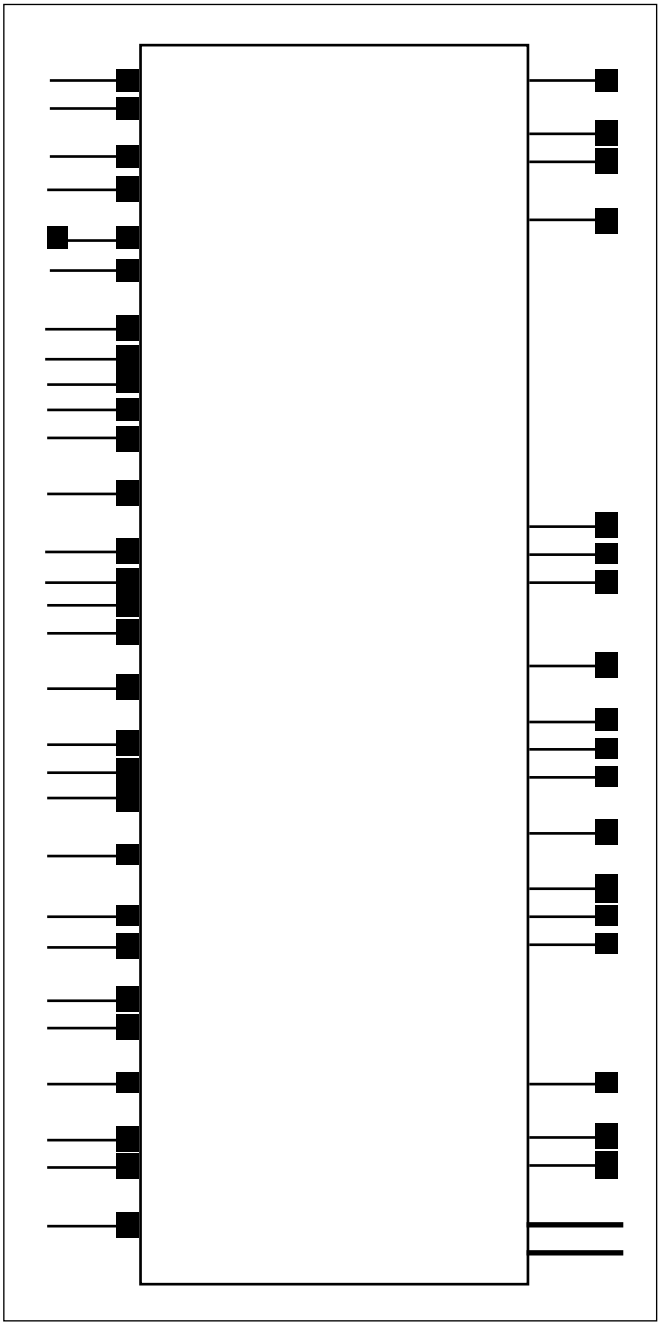


Figure 1: Pin Connections - Top View

1. FUNCTIONAL DESCRIPTION

The MA31754 Processor Support Chip (PSC) is a single chip device providing much of the support circuitry for systems based on the MA31750 microprocessor. The PSC is capable of supporting system with the additional, optional configurations of MMU/ BPU (MA31751), EDAC (MA31755), parity, DMA controller (MA31753) and external system bus interface.

1.1 RESET GENERATION

The PSC generates system reset to the CPU and any other associated logic which requires a reset. The system reset output pin becomes active (low) whenever the RESETN input to the PSC becomes active and remains low 10 clock cycles after RESETN has become inactive. Alternatively, should the ROMWRN input be active during RESETN low, then the system reset output will remain active until both RESETN and ROMWRN have become inactive, or for 10 clock cycles - whichever is the longer.

SYSRESETN will also be set active low if there is no response to the WD interrupt after a timeout period has elapsed. Again, SYSRESETN stays low for 10 clock cycles or until ROMWRN goes high - whichever is the longer.

1.2 CONFIGURATION SENSING

Upon reset the processor determines the hardware configuration of the system by reading a configuration register on the local data bus. At the same time the PSC samples the same configuration data for its own use. A description of the bit allocation within the CPU configuration word is shown following in figure 2.

Bit No.	Meaning
0	MMU select bit 0
1	BPU select bit 0
2	Console select
3	MMU select bit 1
4	Level / Edge sensitive interrupts
5	MMU select bit 2
6	Parity odd / even
7	Built in Test on reset
8	Start up ROM present
9	DMA present
10	1750A/B select
11	Instruction Set Expansion
12	BPU Select 1
13	BPU Select 2
14	Reserved
15	External system interface accesses (physical or logical)

Figure 2: Configuration Register Bit Allocation

1.3 READY GENERATION

The PSC incorporates a programmable RDYN generator which is used to drive the CPU RDYN input indicating the completion of bus access cycles.

For each memory block (defined by a CSAREAN signal going active low), it is possible to independently define 0 to 15 wait states for read accesses and 0 to 15 wait states for write accesses, for both MMU cache hit and miss occurrances.

The correct number of memory wait states which are to be inserted, should be programmed into the Memory Ready (MR) Registers. There are 4 of these MR registers, one for each of the chip selected areas CSAREAN[0:3]. Each has the same basic structure shown in figure 3.

Read/Write Address for CS0 MR Register - 0x9F13/0x1F13
Read/Write Address for CS1 MR Register - 0x9F14/0x1F14
Read/Write Address for CS2 MR Register - 0x9F15/0x1F15
Read/Write Address for CS3 MR Register - 0x9F16/0x1F16

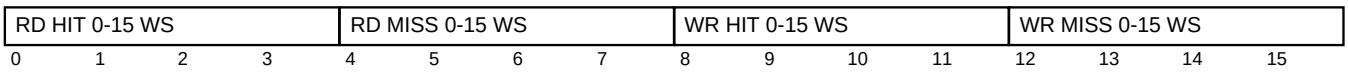


Figure 3: Memory Ready Register Structure

The mapping of these registers onto physical memory is done by external address decoding logic which outputs the Chip select inputs to the PSC.

Note: The HIT/MISS reference is so that different numbers of wait states can be added depending on whatever the cycle is an MMU cache hit or cache miss (determined by the HIT/MISSN signal input to the PSC).

Extra wait states can be added by taking the EXTRDYINN signal high. The wait state count does not start until EXTRDYINN goes low, ie. RDYN goes low, the programmed number of wait states after EXTRDYINN has gone low.

RDYN is also generated for accesses to User IO address space. The required number of waitstates is programmed in the User IO Control Register.

When SYSRESETN and ROMWRN are low, the ready generator automatically inserts 15 waitstates into every external cycles. These cycles can be used for programming an EEPROM device across the external interface.

1.4 ADDRESS RANGE VALIDATION

The following conditions will all cause the PSC to send an ‘External Address Error’ (EXADEOUTN) signal to the CPU:

- Any attempt to address the User IO areas where the address is beyond the Last Implemented User IO Address specified in the User IO Command Register.
- All non-implemented IO commands. Also 1750B mode commands will be illegal in 1750A mode.
- Any attempt to address the Unimplemented Spare IO areas unless the enable bit in the User IO Command Register is set.
- The input EXADEINN being active low.

1.5 FIRST-FAILING PHYSICAL ADDRESS CAPTURE CONTROL SIGNALS (FFPAEN AND FFPAS)

A First Failing Physical Address (FFPA) Register can be implemented as an external register in the system. The enable signal, FFPAEN, can be used as the output enable signal. FFPAEN becomes active when the FFPA register is read. The strobe, FFPAS, can be used to clock the address information into the latch. FFPAS latches the address into the register at the end of every external machine cycle until a relevant error is detected. The latching then stops until the FFPA register has been read. Any of the following signals sampled active low will cause the FFPAS to stop latching the FFPA register: EXADEOUTN, CERRN, NCERRN, PEN, MPROEN. An error code and transfer type could also be recorded in this register - see below for suggestions.

Suggested First Failing Physical Address Register - Read Address 0x9F0B

EA(3:10)								EA(0:2)			CPUGNTN	DMAGNTN	EXTGNTN	Users	
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

1.6 BUS ARBITRATION

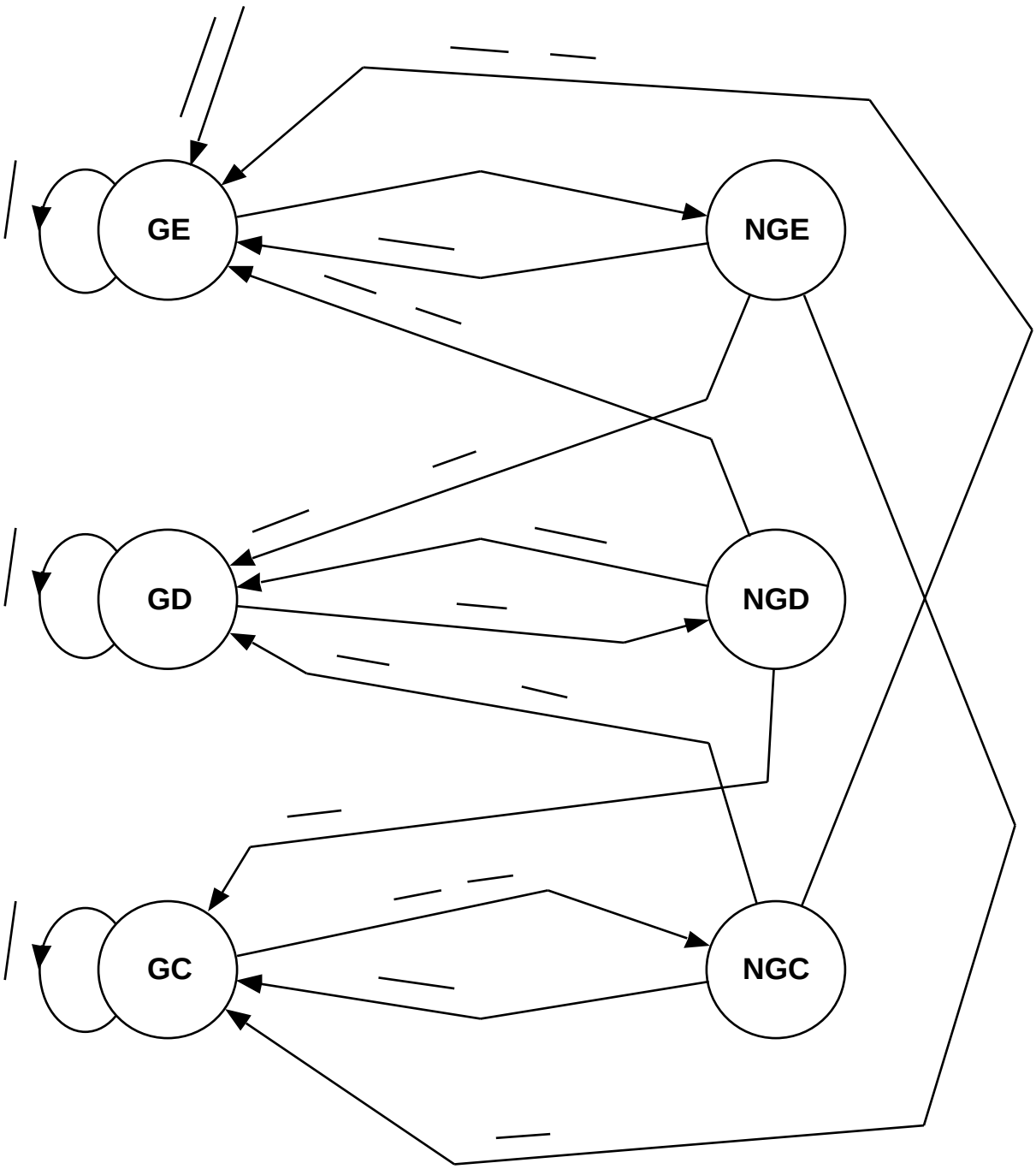
The PSC contains a Bus Arbiter which allocates the system bus to up to three different bus-units. These are, in order of priority, highest first:

1. An external controller working with logical or physical addresses and having a request/grant protocol not using the system clock.
2. A local system DMA controller.
3. The CPU.

Any unit which is configured in the system can request control of the bus by asserting the relevant RQN signal low. In the case of the external interface and the local DMA controller, the incoming RQN signal is sampled on negative going clock edges.

When the current bus cycle finishes (and there are no grant signals issued), the request lines are checked. The request from the highest priority bus-unit is acknowledged by the Arbiter by asserting the relevant GNTN signal low, thus granting the unit use of the next bus cycle. This unit will be granted the bus until either it ceases to request the bus or a request of higher priority is detected. If no incoming requests are waiting when the current cycle ends, the CPU is granted the bus.

At reset, the Arbiter grants the system bus to the External Interface. The external interface remains granted until SYSRESETN goes inactive. The “grant by request” system then starts.



When in state GE EXTGNT_N = 0
When in state GD DMAGNT_N = 0
When in state GC CPUGNT_N = 0
When in state NGX no grant signals issued
SLOCK_N is LOCK_N sampled on negative clock edges
ASNEG is ASTROBE sampled on negative clock edges
RQEN is EXTREQ_N sampled on negative clock edges
RQDN is DMAREQ_N sampled on negative clock edges

Figure 4: State Diagram for the Bus Arbitration Block

1.7 INTERRUPT SYNCHRONISATION AND ACKNOWLEDGE

There are 3 interrupts output from the PSC. The WDINTN is not sampled and cannot be masked or disabled. The active interrupt is cleared by the INTAKN signal indicating that the WD interrupt is being serviced.

The EDACINTN can be set by CERRN, NCERRN or PEN going active. CERRN and NCERRN are sampled as they come from combinational logic which may glitch. EDACINTN can be masked and/or disabled by the relevant bits in the PSC Interrupt Register. The interrupt is cleared by the relevant INTAKN going active.

The UARTINTN is activated by signals generated internally within the PSC. This interrupt can be masked or disabled by the PSC Interrupt Register. The interrupt is activated when any one of the FE, OE, PE, BD, RxBF or TxBE bits are set in the UART control and status register. The bit set in the interrupt register will indicate whether the error occured in UART 1 or 2. UART1 and UART2 are both masked by MASK and enabled by EU. They both cause UARTINTN to go active if they are unmasked and enabled. UARTINTN is cleared by the relevant INTAKN going active.

The functionality of this block is derived from the “Interrupt Masking and Allocation” register (figure 5). The mapping of the PSC interrupts onto the CPU interrupts is defined by the “Interrupt Mapping” register (figure 6).

Interrupt Allocation Register - Read/Write Address - 0x9F09/0x1F09

EDAC Interrupt Status and Control								UART Interrupt Status and Control							
CE	NCE	PE	ECE	ENCE	EPE	Mask	-	CE	NCE	UART1	ECE	ENCE	EU	Mask	UART2
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

CE	EDAC Correctable Error status	Can set both interrupts. If this bit is set then the PSC has sampled an error on the CERRN input.
NCE	EDAC Non-correctable Error status	Can set both interrupts. If this bit is set then the PSC has sampled an error on the NCERRN input.
PEN	PSC Parity Error status	Can set EDACINTN only. If this bit is set then the PSC has sampled an error on the PEN input.
UART	PSC UART error status	Can set UARTINTN only. If this bit is set then an internal UART error has occurred.
ECE	Enable Correctable Error	Enable EDAC Correctable Error to interrupt output.
ENCE	Enable Non-correctable Error	Enable EDAC Non-correctable Error to interrupt output.
EPEN	Enable Parity ERROR	Enable Parity Error to interrupt output (EDACINTN only).
EU	Enable UART Error	Enable UART Error to interrupt output (UARTINTN only).
MASK	Mask interrupt	If either of these bits are set high, then the relevant interrupt cannot be issued. As soon as the mask bit is cleared, the interrupt will go active if a fault has occurred. The interrupt outputs are automatically masked during EDAC online memory testing.

Figure 5: Bit Allocation for Interrupt Allocation Register

Interrupt Mapping Register - Read/Write Address - 0x9F17/0x1F17

Res				UART LP				EDAC LP				WD LP			
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Figure 6: Interrupt Mapping Register

If the interrupts are level sensitive and are to be cleared by INTAKN going active, it is necessary to define which interrupt inputs on the CPU are driven by which interrupt outputs from the PSC. This enables the correct interrupt (the one being serviced) to be cleared. Bits 11:14 of the linkage pointer of the relevant interrupts should be entered into the mapping register. Eg. If the WDINTN output on the PSC is connected to the PWRDN input on the CPU, the bits 0000 should be entered into bits 12:15 of the mapping register. This is derived from the PWRDN linkage pointer 0x0020. If UARTINTN is connected to INT15N, the mapping register has 1111 in bits 4:7 (from the LP 0x003E). The full list of available (external interrupt) linkage pointers and code for the mapping register is shown in figure 7.

CPU Interrupt	Linkage Pointer	Map Code
PWRDN	0x0020	0000
INT02N	0x0024	0010
INT08N	0x0030	1000
INT10N	0x0034	1010
INT11N	0x0036	1011
IOI1N	0x0038	1100
INT13N	0x003A	1101
IOI2N	0x003C	1110
INT15N	0x003E	1111

Figure 7: Mapping PSC Interrupts onto CPU Interrupts

1.8 WATCHDOG TIMER

The PSC implements a watchdog timer/counter which is driven by a 1kHz clock, typically implemented as a simple R-C oscillator. The counter, which is implemented as bits 8-15 of the Watchdog Timer register, is loaded upon reset or when an XIO write to the watchdog refresh register is performed. The value loaded into the counter is held in the watchdog time-out register. Subsequently the counter is decremented until it reaches zero, at which point the counter is stopped and a watchdog interrupt is generated. The watchdog counter will be re-loaded and restarted once an interrupt acknowledge has been received. An additional control bit - WD Reset - allows the watchdog Elapse timer to reset the system should a timeout have occurred and no interrupt response have been received within a further 16ms.

Following a reset the WD time-out register is preset to 255 and the counter is thus enabled for 255ms. During operation this limit may be reprogrammed to any 8 bit value under software control - thus varying the time-out period between 1 and 255ms.

The WD function may be inhibited either by asserting the WDinhibit input or by setting the WDinhibit bit in the PSC control register. The inhibit becomes the logical OR of either of these two. Whilst inhibited the WD counter is frozen and no WD interrupts will be generated. Once both inhibit signals are inactive, the operation of the WD timer will resume as normal. STOPN going low will also stop the WD timer from incrementing.

A time-out may also be forced via software by setting the WDForceElapse control bit whilst the WD inhibit is inactive.

Watchdog Control Register - Read/Write Address - 0x9F01/0x1F01

FoEl	WDER	Mask	IntS	IntC	Inhb	Stat	Res	Watchdog Timeout Limit							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

FoEl	Force Elapse	Forces WD timer to the elapsed state (if inhibit not set). This will trigger an interrupt if the WD interrupt mask bit is not set.
WDER	WD Elapse Reset	When this bit is set and the WD counter reaches zero a WD elapse interrupt is issued. If no system response is performed during the following 16ms the system is restarted by asserting the SYSRESETN line low.
Mask	Mask WD Interrupt	The Elapse reset counter is not started until this interrupt is asserted.
IntS	WD Interrupt Status	This bit is set low when a WD interrupt becomes active. It is cleared again on the INTAKN signal used to clear the interrupt.
IntC	WD Interrupt Clear	Writing a 1 to this bit clears the WD interrupt and restarts the WD timer.
Inhb	Inhibit Count	Halts the WD counter at its current state and resets the WD interrupt.
Stat	Status	Set to 0 to indicate the WD is in the RUN state and all Inhibited states. 1 indicates any other state (WD not OK).

Figure 8: Watchdog Control Register Bit Allocation

Watchdog Timer Register - Read/Write Address - 0x9F0A/0x1F0A

								Current Watchdog Timer Value							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Writing any data to this register causes the watchdog timer to restart. The register will be loaded with the Watchdog Timeout Limit in the WD control register. A read access to this register reads the current WD timer value.

1.9 PSC CONTROL REGISTER

The PSC Control Register collects together some miscellaneous control bits as shown.

PSC Control Register - Read/Write Address 0x9F00/0x1F00

RES	RES	ECBE	RES	RES	EExt	RES	RES	RES	SC/2	Timer clock divider					
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

RES	Reserved
ECBE	EDAC Check Bit Write Enable Bit. Active high to enable the write
EExt	1 Enables External Interface accesses to the local 31750 system
SC/2	Serial clock divide by 2 (UART - 19200/9600 baud). 1 gives 9600 baud
Timer clock divider	System clock is divided by 5 times the value in this register to produce TCLK

Figure 9: PSC Control Register Bit Allocation

1.10 USER IO CONTROL REGISTER

User IO Control Register - Read/Write Address - 0x9F03/0x1F03

IO RDY 0-15 Wait States				DACh	SExp	User IO Address, Read: 0000-03FF/Write: 8000-83FF									
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

IO RDY 0-15 WS		Defines number of wait states required when accessing User IO space and the First Failing Physical Address Register.
DACh	Disable Address Check	Disables User IO address checking when asserted high.
SExp	Enable Spare IO areas	The Unimplemented Spare IO command area is made available to the user when this bit is asserted.
User IO Address	Address of Last Implemented User IO command	An EXADEOUTN fault is generated if an attempted access to the User IO area has an address greater than that specifed here. This value limits the User IO space to between 0000 and 03FF for reads and 8000 and 83FF for writes.

Figure 10: Bit Allocation for User IO Control Register

1.11 CLOCKS AND TIMERS

3 clocks are input to the PSC. The WDCLK is an independant clock, input only to the watchdog timer. CLKOUT is the input clock (output from the CPU). This is divided by the value programmed in the control register to produce the 100KHz TCLK output.

OBTCLKIN should be a clock with a very tight specification on the frequency. This is divided by the factor in the OBT Prescale Register to provide the OBTCLK output. The OBTCLK is then further scaled by the value in the Real Time Clock Division Register to produce the RTCLK output. The OBTCLK also increments the two 16-bit On-Board Timer Registers, (these make up a 32-bit counter). These OBT Registers are cleared when the OBT Prescaler Register is written. When STOPN goes active low, the PSC goes into test mode. In this mode, the OBT counter registers can be written to enable testing procedures. STOPN active also inhibits the OBTCLK, RTCLK and TCLK outputs.

On-Board Timer Register 1 - Read/Write Address - 0x9F0F/0x1F0F

OBT (16 most significant bits)															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

On-Board Timer Register 2 - Read/Write Address - 0x9F10/0x1F10

OBT (16 least significant bits)															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

OBT Prescale Register - Read/Write Address - 0x9F11/0x1F11

Prescale Factor															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Real Time Clock Division Register - Read/Write Address - 0x9F12/0x1F12

RTC Division Factor															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

1.12 SERIAL INTERFACES

Two simple bidirectional interfaces are provided, allowing asynchronous receive and transmit with a standard communications protocol (RS-232). The baud rate is user-definable and is produced from the system clock by an on-chip divider network.

UART 1 and 2 Control & Status Register

LEcE	SPE	SPAR	ERR	SBRK	RxE	StB	TxE	BD	RxBF	FE	OE	PE	TxBE	RxRY	TxRY
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

UART Transmit Data Register

-	-	-	-	-	-	-	-	Transmit Serial Data							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

UART Received Data Register

0	0	0	0	0	0	0	0	Receive Serial Data							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

LEcE	Local Echo Enable. When this bit is high, the UART transmit data will echo the receive data.
SPE	Serial line Parity is Enabled when this bit is high.
SPAR	0 = serial line Parity is even. 1 = serial line Parity is odd.
ERR	Error Reset - FE, OE, and PE are cleared when this bit is set high.
SBRK	Force Break Interrupt - when this bit is high, the UART interrupt is forced active.
RxE	UART receive enable.
StB	0 = 2 stop bits on the serial line. 1 = 1 stop bit on the serial line.
TxE	UART transmit enable.
BD	Break Detect. This bit is set high when a break character is received.
RxBF	Receive Buffer Full.
FE	1 = Framing Error.
OE	1 = Overrun Error.
PE	1 = Parity Error.
TxBE	Transmitter Buffer Empty.
RxRY	Receiver Ready.
TxRY	Transmitter Ready.

Serial Data Format

The serial line is held high if no data is present. The start of a data byte is marked by a low start bit. This is immediately followed by 8 data bits, a parity bit (when enabled) and one or two stop bits (both high).

Receiver

There is a 32-byte long buffer on the receiver, to allow incoming data to be faster than the UART can output parallel data. The receiver checks for the following errors:

(i) Parity errors (PE is set if error found).
(ii) Framing errors (FE is set if the number of stop bits is incorrect).
(iii) Overrun errors (OE is set if the receiver buffer is full).

Transmitter

There is also a 32-byte long buffer on the transmitter. This allows the incoming data from the parrallel data bus to be faster than the UART can transmit. The transmitter adds a start bit, a parity bit and 1/2 stop bits according to the defined configuration. When the local echo is enabled, the transmitter outputs the received data.

Break Detect and Force

If the receiver detects a break, it causes a UART interrupt to be set. A break is defined as a low on the serial line for at least the duration of the start bit, the data bits and the programmed number of parity and stop bits. It is possible to transmit a break from the UART by setting the SBRK bit in the UART status and control register. Once this bit is set, the transmitter will continue to output break characters until the bit is cleared or until the PSC is reset.

Baud Rate

The PSC has an on-board baud rate generator which is programmable to work at 9600 or 19200 baud. The baud rate is generated from CLKOUT. The programming is done in the control register.

1.13 EDAC TEST FACILITY

The PSC output, EDACCBWRN, should be used as the write strobe for the check bit memory. If this is done, the EDAC can be tested by independantly writing the data and check bit memories, eg. A normal write, with check bits, is executed. The ECBE bit in the control register is then reset to zero to disable the check bit write strobe. The data memory is then re-written with 1 or 2 errors. ECBE is set high and the data word is read back through the EDAC. If 1 error was set, the correction facility on the EDAC is checked. If 2 errors were set, the EDAC detection facility is checked.

1.14 THE STOP FUNCTION

When STOPN is asserted low, the PSC stops all internal timers and clock outputs. This allows testing of the watchdog and on-board timers under software control.

2. PSC REGISTER ADDRESS SUMMARY AND INITIALISATION DATA

The PSC registers are placed in IO space and may be accessed via XIO or VIO commands issued by the CPU. The register addresses and their default (start-up) values are shown in figure 11.

Output	Input	Register	Initial State
1F00	9F00	(PSC) Control Register	0x 247F
1F01	9F01	Watchdog Control Register	0x 50FF
N/A	9F02	System Configuration Register	As CPU configuration register
1F03	9F03	User IO Control Register	0x F3FF
1F06	9F06	UART 1 Control & Status Register	0x 0204
1F07	N/A	UART 1 Transmit Data Register	0x 0000
N/A	9F08	UART 1 Receive Data Register	0x 0000
1F09	9F09	Interrupt Allocation Register	0x 0C04
1F0A	9F0A	Watchdog Timer Register	0x 00FF
N/A	9F0B	First Failing Physical Address Register	0x 0000
1F0C	9F0C	UART 2 Control & State Register	0x 0204
1F0D	N/A	UART 2 Transmit Data Register	0x 0000
N/A	9F0E	UART 2 Receive Data Register	0x 0000
1F0F	9F0F	On-Board Timer Register 1 (MSBs)	0x 0000
1F10	9F10	On-Board Timer Register 2 (LSBs)	0x 0000
1F11	9F11	USO Prescaler Register	0x 0001
1F12	9F12	Real-Time Clock Division Register	0x C350
1F13	9F13	CS0 Memory Ready Register	0x FFFF
1F14	9F14	CS1 Memory Ready Register	0x FFFF
1F15	9F15	CS2 Memory Ready Register	0x FFFF
1F16	9F16	CS3 Memory Ready Register	0x FFFF
1F17	9F17	Interrupt Mapping Register	0x 0D20

Figure 11: PSC Register Allocation Map

3. PIN DESCRIPTIONS

Busses

D[0:15]	I/O	System data bus. D00 is the most significant bit.
A[0:15]	I	System address bus (active high).

Strobes

AS	I	System address strobe. Indicates the presence of address information on the system address bus. This signal is produced by the current bus master.
MION	I	Memory/IO select. Asserted high by the current bus master during a memory access, low during an IO transfer.
RDWN	I	Read/Write select. Asserted high by the current bus master when data is being read into the bus master, low when data is being written from the bus master.
RDN	I	Read strobe. The rising edge of this signal indicates that data is being read by the current bus master.
WRN	I	Write strobe. The rising edge of this signal indicates that data is being written by the current bus master.
EDACCBWRN	O	Active low write strobe used for check bit memory writing. Can be disabled for EDAC test purposes.
FFPAS	O	Active high strobe used to latch the first failing Physical Address Register. Disabled after a fault has occurred until the FFPAR has been read.

Clock Signals

TCLK	O	Timer clock signal.
WDCLK	I	Oscillator input used by the watchdog timer.
OBTCLKIN	I	Ultra Stable clock oscillator input used for the On-Board Timer function.
OBTCLK	O	On-Board Timer clock output.
RTCLK	O	Real Time clock output.
CLKOUT	I	From the CPU, this clock is used as the PSC input clock.

Chip Select Signals

CSAREAN[0:3]	I	Active low indicates which area of memory is currently chip selected.
IOSELN	O	User IO area select. This output is asserted low to allow access to the user IO area as defined in MIL-STD-1750. The area is programmable within the PSC.

Bus Control

CPUGNTN	O	CPU bus grant. Sampled by the CPU on CLKOUT falling, an active low informs the processor that it has control of the system. If no other devices is granted, system control defaults to the CPU.
DMAGNTN	O	DMA bus grant. Sampled by the DMA on CLK falling, this pin is asserted low to inform the DMA that it is the current bus master.
EXTGNTN	O	External bus grant. This pin is asserted low to inform an external system that it is the current bus master.
LOCKN	I/O	Bus lock. This signal is sampled on each falling CLKOUT edge. If low, the bus arbiter will not allow the busses to be reassigned to another bus master.
DMAREQN	I	DMA bus request. This active low signal is driven low by an external DMA controller when it requests the bus, and is sampled on falling CLKOUT edges.
EXTREQN	I	External bus request. This active low signal is driven low by an external bus master when it requests the bus, and is sampled on falling CLKOUT edges.

Interrupts

WDINTN	O	Watchdog interrupt. This output is asserted low if an internal watchdog timeout occurs.
UARTINTN	O	Internal UART interrupt. This output is asserted low by either of the internal UARTs (or by an EDAC or parity error). The interrupt must be unmasked if it is to go active.
EDACINTN	O	EDAC interrupt. This output is asserted low if the NCERRN, CERRN or PEN inputs become active when enabled, and the interrupt is unmasked.
INTAKN	I	Interrupt acknowledge. This active low signal is asserted low by the CPU following receipt of an interrupt. It is used within the PSC to reset level sensitive interrupts.

Figure 12: Pin Descriptions

Faults

MPROEN	I	Memory protect error. Sampled on falling AS.
PEN	I	Parity Error input. Indicates that a parity fault has occurred on the most recent data bus transaction (input sampled on rising DSN).
EXADENINN	I	External address error. This active low input indicates that a memory access is outside the decoded address space.
EXADEOUTN	O	This active low output indicates that a memory or IO access error has occured. It can be activated by EXADEINN going low (memory error) or by the internal IO address decode flagging an error.
NCERRN	I	Non-correctable error. (active low) The system EDAC asserts this signal to indicate that a non-correctable error has occurred. Sampled on rising DSN.
CERRN	I	Correctable error. (active low) The system EDAC asserts this signal to indicate that a correctable error has occurred. The EDAC will have corrected the data if the EDAC 'correct' bit is set. Sampled on rising DSN.

UARTS:

RXDATA1	I	Serial interface received data, input to UART 1.
RXDATA2	I	Serial interface received data, input to UART 1.
TXDATA1	O	Serial interface transmit data, output from UART1.
TXDATA2	O	Serial interface transmit data, output from UART2.

Miscellaneous:

CONFWN	I	Configuration word read strobe.
SYSRESETN	O	System reset (active low). Held active either 10 clock cycles or until ROMWRN is inactive - whichever is the longer.
RESETN	I	Reset input for system (active low). Rising edge starts the SYSRESETN count.
WDINHIBITN	I	Disables (suspends) the watchdog timeout function.
EXRDYINN	I	External ready signal (active low) - forces RDYN low.
RDYN	O	Goes low to indicate that the current bus cycle can terminate.
ROMWRN	I	Non volatile memory write enable. If this signal is active low at reset, the external interface is granted and SYSRESETN is extended. If asserted after reset, the signal enables writing to non-volatile memory (Start-Up-ROM is enabled). Asynchronous, sampled on negative CLKOUT edges.
STOPN	I	This active low input is sampled on negative CLKOUT edges. When asserted, the WD timer and the OBT stop and the TCLK output is inhibited.
FFPAEN	O	Active low, this output should be used to enable the data from the first failing Physical Address Register onto the data bus. The enable goes active during a read of XIO address 0x 9F0B.

Figure 12: Pin Descriptions (continued)

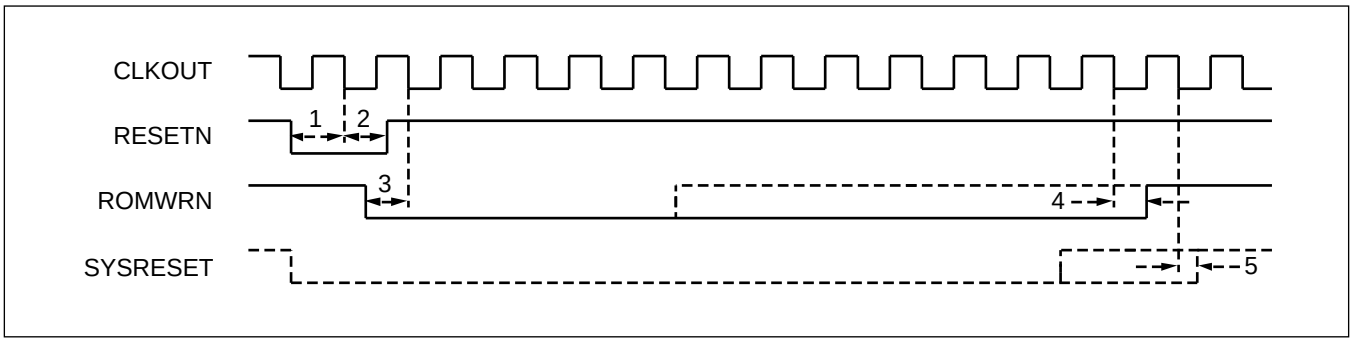


Figure 13: Reset Logic

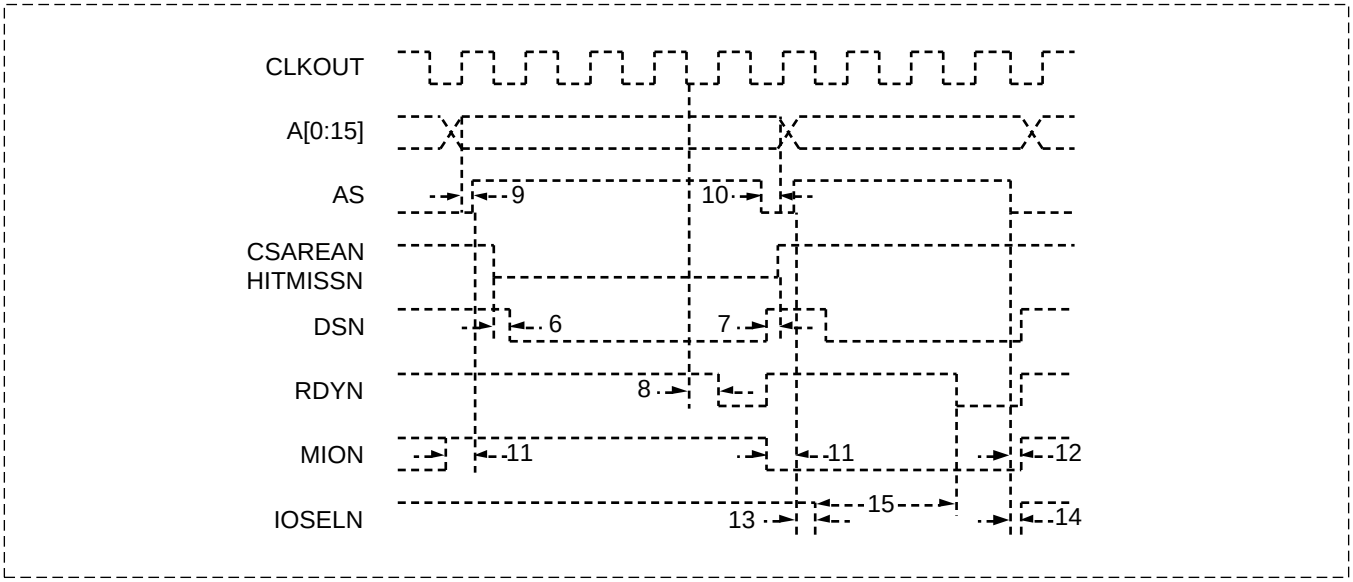


Figure 14: Wait State Generator

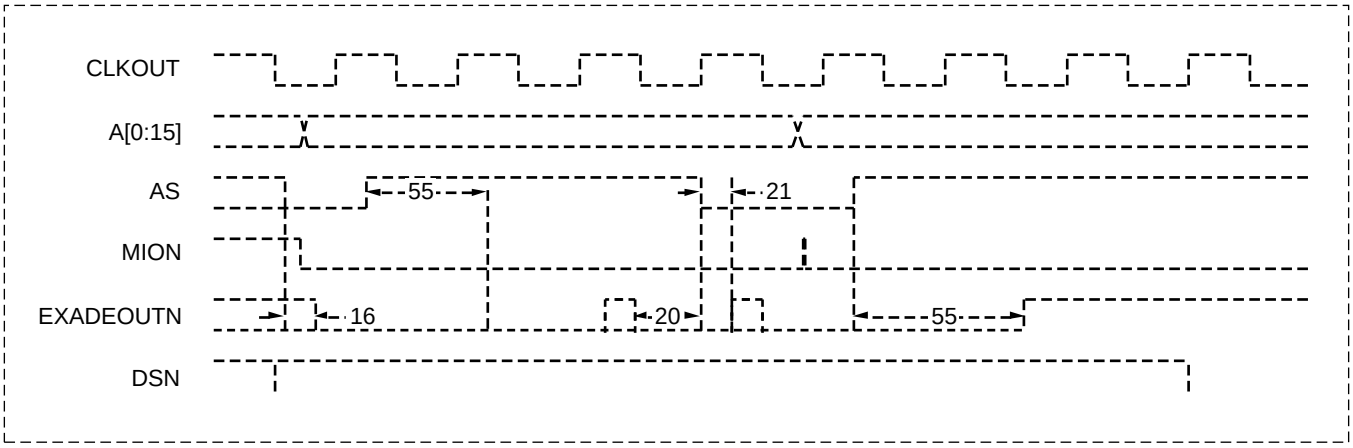


Figure 15: IO Address Range Validation

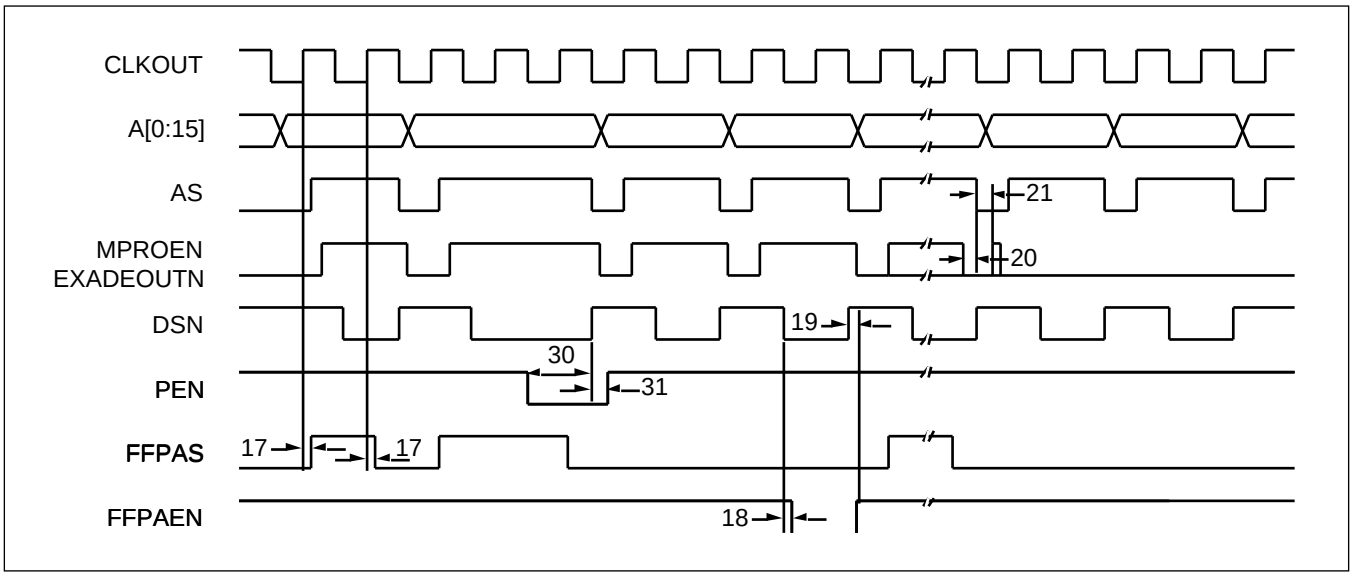


Figure 16: First Failing Physical Address Register Control

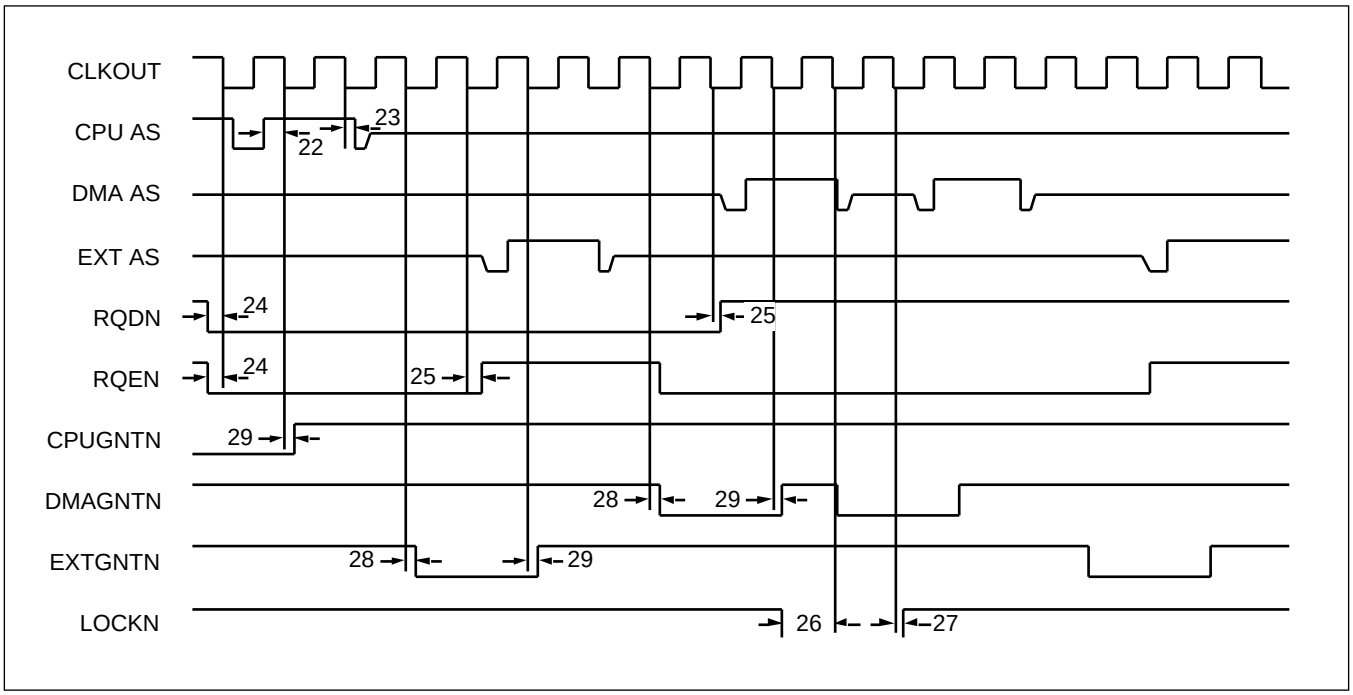


Figure 17: Bus Arbitration

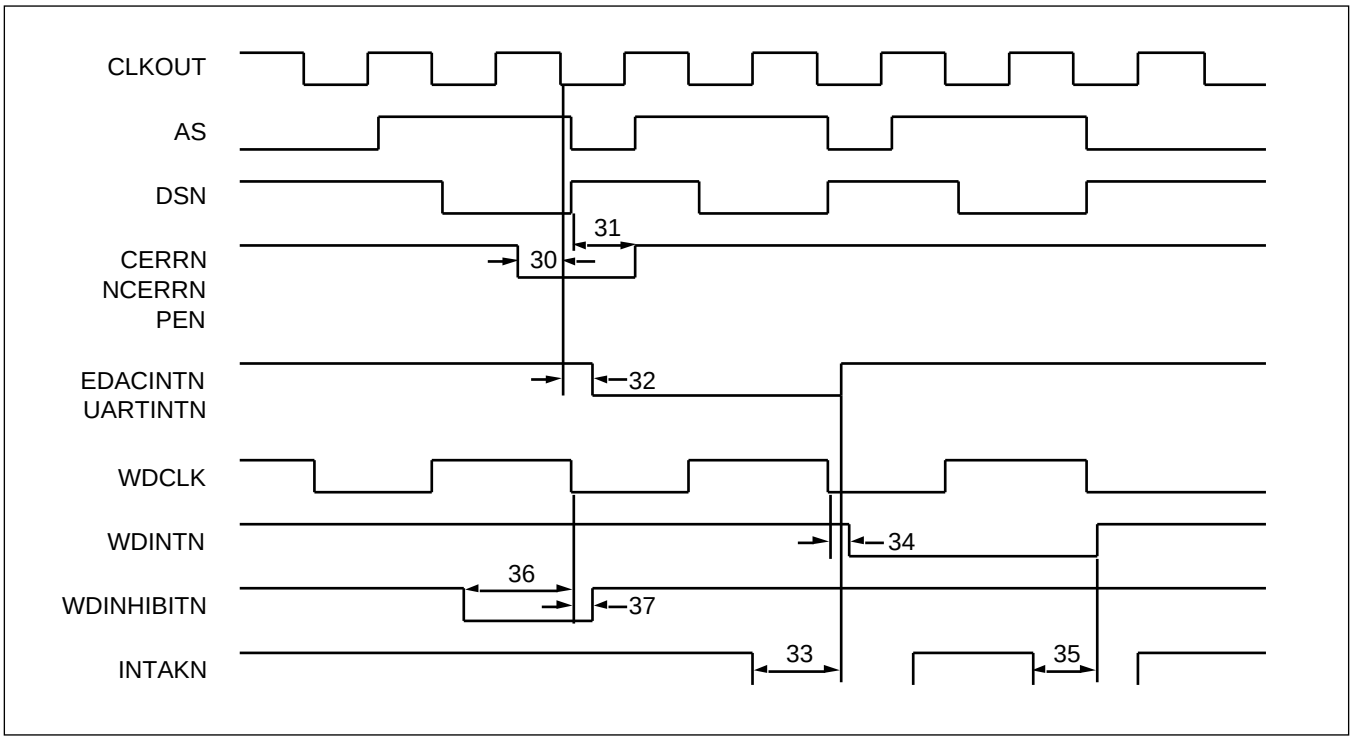


Figure 18: Interrupt Timings

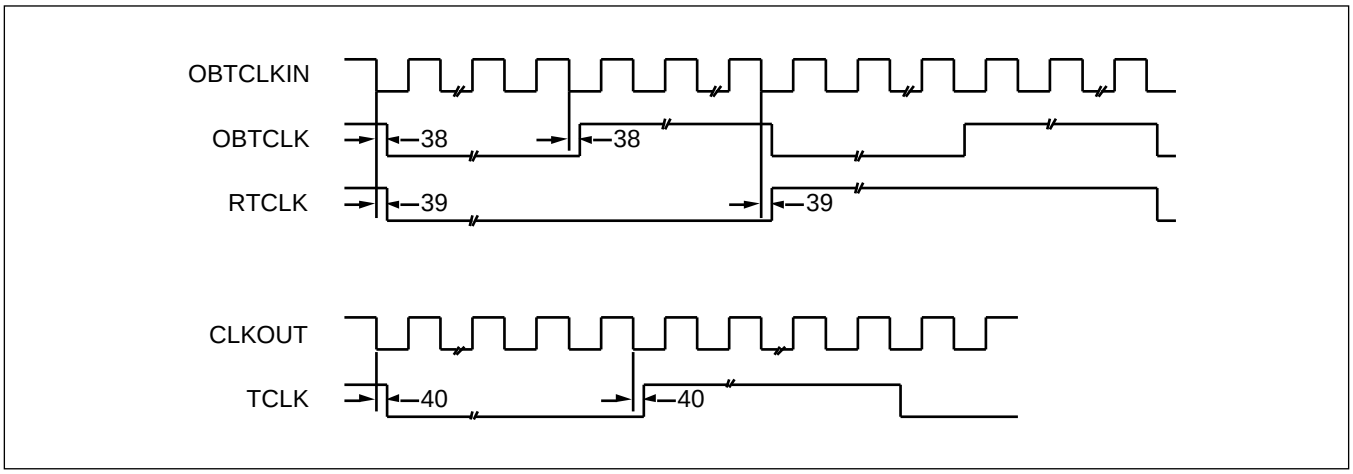


Figure 19: Clock Generation Logic

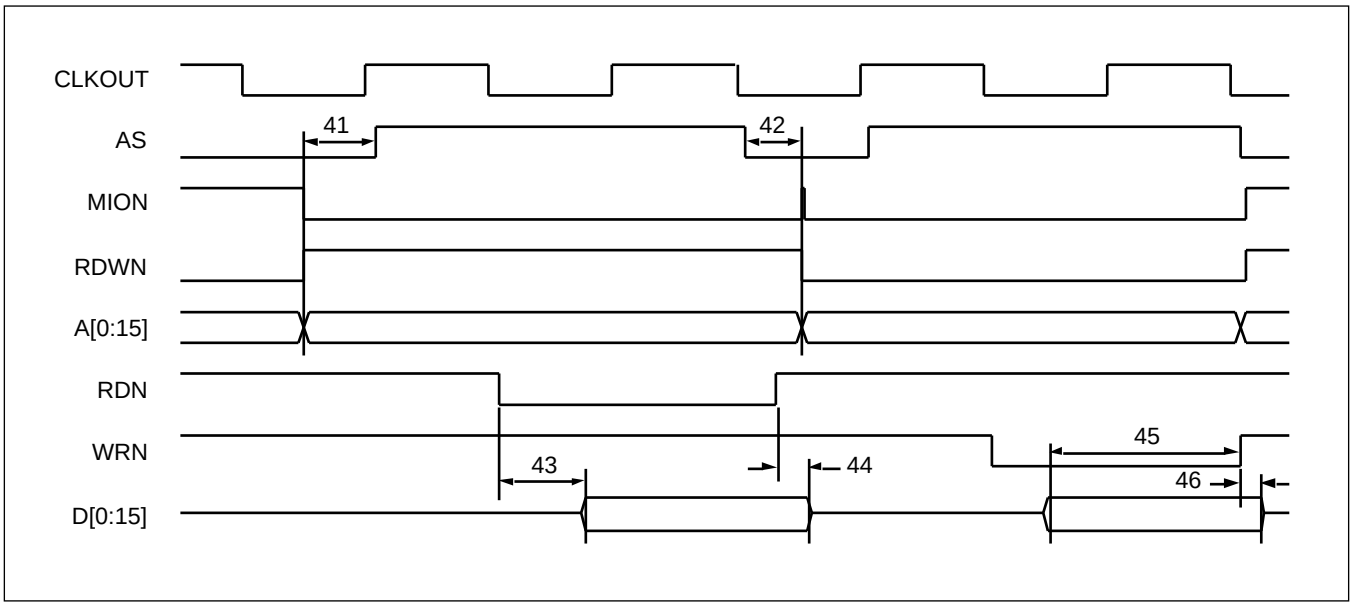


Figure 20: Reading and Writing Registers

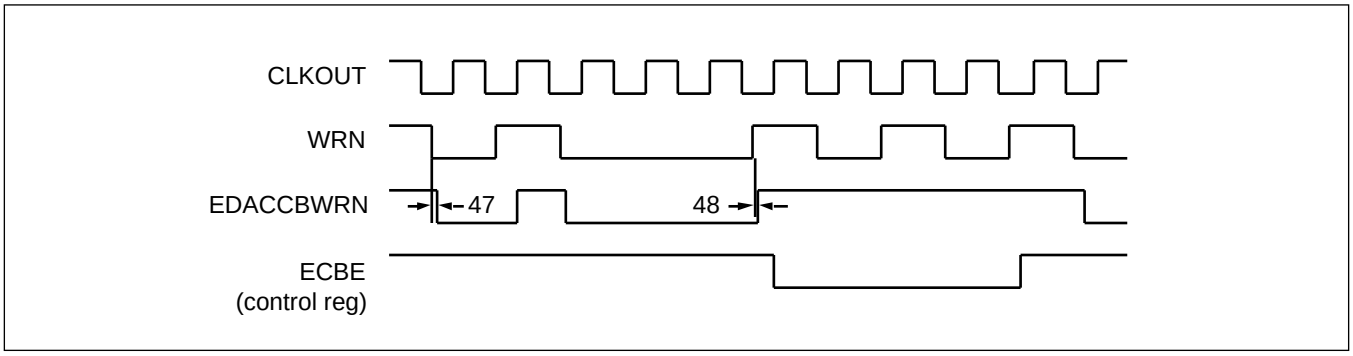


Figure 21: Check Bit Write Strobe Timings

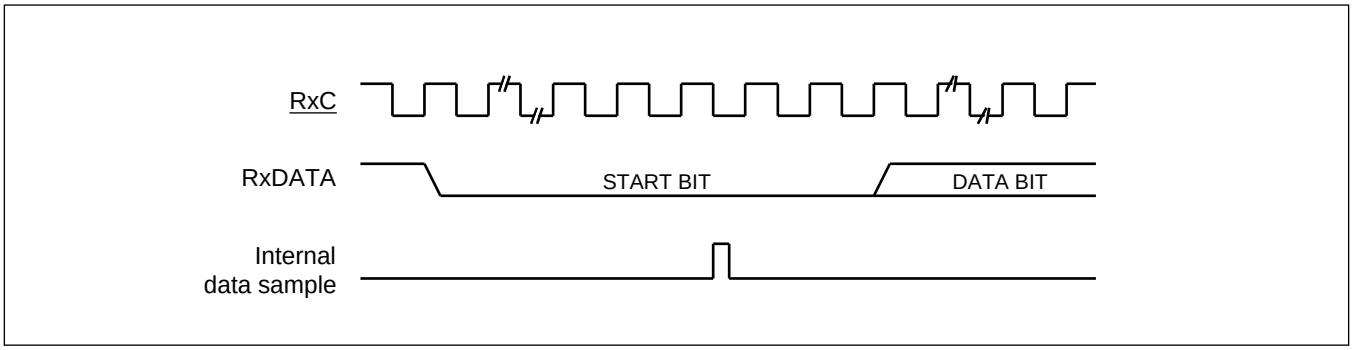


Figure 22: Receive Clock and Data

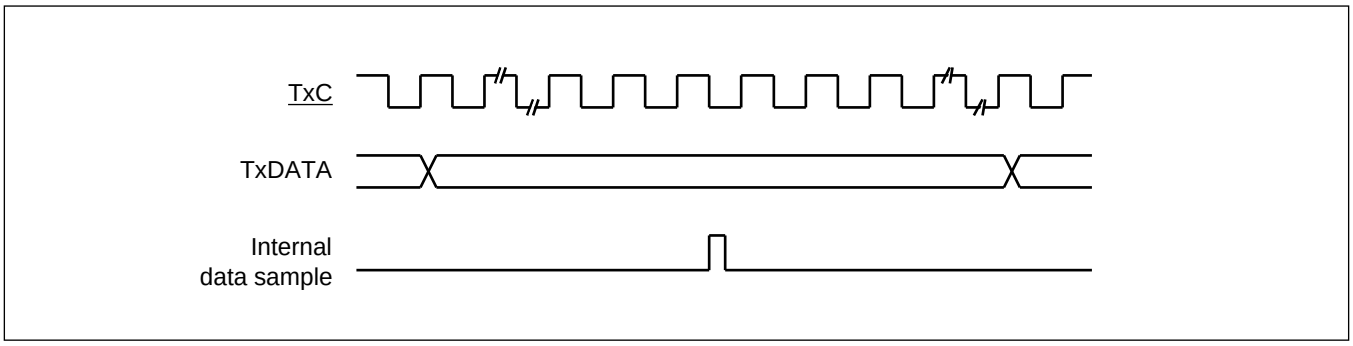


Figure 23: Transmitter Clock and Data

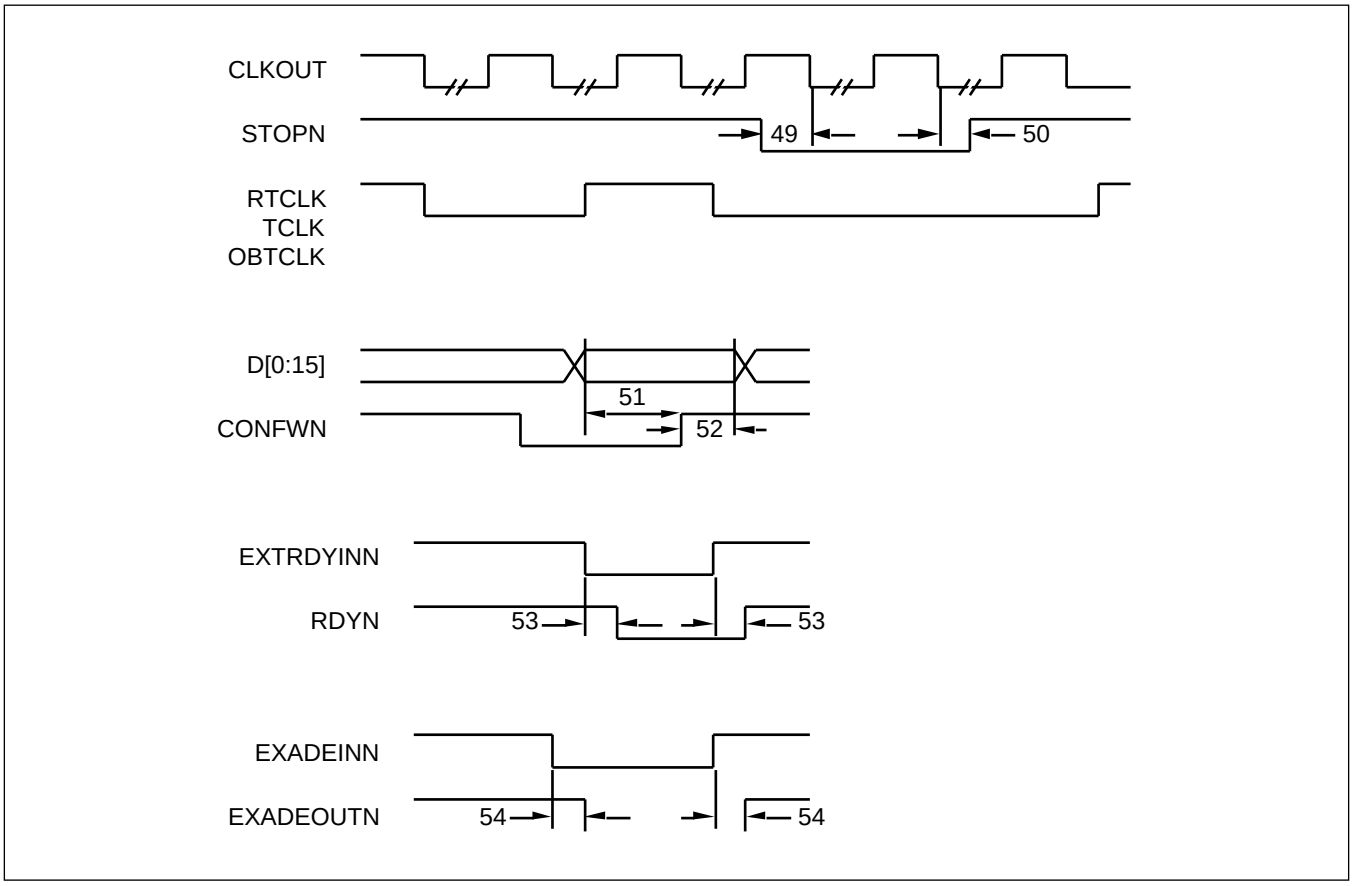


Figure 24: Miscellaneous Timings

No.	Parameter	Min.	Max.	Units
1	RESETN setup to CLKOUT falling			ns
2	RESETN hold after CLKOUT falling			ns
3	ROMWRN setup to CLKOUT falling			ns
4	ROMWRN hold after CLKOUT falling			ns
5	CLKOUT falling to SYSRESETN valid			ns
6	CSAREAN/HITMISSN setup to DSN falling			ns
7	CSAREAN/HITMISSN hold after DSN rising			ns
8	CLKOUT falling to RDYN falling			ns
9	Address setup to AS rising			ns
10	Address hold after AS falling			ns
11	MION setup to AS rising			ns
12	MION hold after AS falling			ns
13	AS rising to IOSELN valid			ns
14	AS falling to IOSELN valid			ns
15	IOSELN falling to RDYN falling			ns
16	AS falling to EXADEOUTN falling			ns
17	CLKOUT rising to FFPAS valid			ns
18	DSN falling to FFPAEN falling			ns
19	DSN rising to FFPAEN rising			ns
20	MPROEN/EXADEOUTN setup to AS falling			ns
21	MPROEN/EXADEOUT hold after AS falling			ns
22	AS setup to CLKOUT falling			ns
23	AS hold after CLKOUT falling			ns
24	RQEN/RQDN setup to CLKOUT falling			ns
25	RQEN/RQDN hold after CLKOUT falling			ns
26	LOCKN setup to CLKOUT falling			ns
27	LOCKN hold after CLKOUT falling			ns
28	CLKOUT falling to CPUGNTN/DMAGNTN/EXTGNTN falling			ns
29	CLKOUT falling to CPUGNTN/DMAGNTN/EXTGNTN rising			ns
30	CERRN/NCERRN/PEN setup to DSN rising			ns
31	CERRN/NCERRN/PEN hold after DSN rising			ns
32	CLKOUT falling to EDACINTN/UARTINTN falling			ns
33	INTAKN falling to EDACINTN/UARTINTN rising			ns
34	WDCLK falling to WDINTN falling			ns
35	INTAKN falling to WDINTN rising			ns
36	WDINHIBITN setup to WDCLK falling			ns
37	WDINHIBITN hold after WDCLK falling			ns
38	OBTCLK valid after OBTCLKIN falling			ns
39	RTCLK valid after OBTCLKIN falling			ns
40	TCLK valid after CLKOUT falling			ns
41	Address, MION and RDWN setup to AS rising			ns
42	Address, MION and RDWN hold after AS falling			ns
43	Data valid after RDN falling			ns
44	Data valid after RDN rising			ns
45	Data setup to WRN rising			ns
46	Data hold after WRN rising			ns
47	EDACCBWRN falling after WRN falling			ns
48	EDACCBWRN rising after WRN rising			ns
49	STOPN setup to CLKOUT falling			ns
50	STOPN hold after CLKOUT falling.			ns
51	Data setup to CONFWN rising			ns
52	Data hold after CONFWN rising			ns
53	EXTRDYINN valid to RDYN valid			ns
54	EXADEINN valid to EXADEOUTN valid			ns
55	AS rising to EXADEOUTN valid			ns

† This timing includes MA31751 Setup Cycles and Built In Test Cycles.
Mil-Std-883, Method 5005, Subgroups 9, 10, 11.
Note: TL = Low CLK period (ns), TH = High CLK period (ns).
Test Conditions: Vdd = 5.0V ±10%, Temperature = -55ºC to 125ºC, Vil = 0.0V, Vih = Vdd.
Output loads: All test load 1 unless otherwise specified.
Output Threshold: 50% Vdd (Load 1), Vss+1V, Vdd-1V (load2).

Figure 25: Timing Parameters

CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 26: Absolute Maximum Ratings

Parameter	Min	Max	Units
Clock Frequency (CLKOUT)	0	16	MHz
Recommended Clock Duty Cycle	45	55	%

Vdd=5V±10% over full operating temperature range.
Mil-Std-883, method 5005, subgroups 7, 8A, 8B.

Figure 27: Operating AC Electrical Characteristics

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad(Si)		Units
			Min	Max	
V_{DD}	Supply Voltage	-	4.5	5.5	V
V_{IH}	Input High Voltage	-	80%V_{DD}	-	V
V_{IL}	Input Low Voltage	-	-	20%V_{DD}	V
V_{CKH}	CLKOUT Input High Voltage	-	V_{DD}-0.5	-	V
V_{CKL}	CLKOUT Input Low Voltage	-	-	V_{SS}+0.5	V
V_{OH}	Output High Voltage	I_{OH} = 3mA	V_{DD}-0.5	-	V
V_{OL}	Output Low Voltage	I_{OL} = 5mA	-	V_{SS}+0.4	V
I_{IH}	Input High Current (Note 1)	-	-	10	µA
I_{IL}	Input Low Current (Note 1)	-	-	-10	µA
I_{OZH}	I/O Tristate High Current (Note 1)	-	-	50	µA
I_{OZL}	I/O Tristate Low Current (Note 1)	-	-	-50	µA
I_{DDYN}	Dynamic Supply Current @16MHz	-	-	110	mA
I_{DDS}	Static Supply Current	-	-	10	mA

V_{DD}=5V±10%, over full operating temperature range.
Mil-Std-883, method 5005, subgroups 1, 2, 3.
Note 1: Guaranteed but not tested at low temperature (-55°C).

Figure 28: Operating DC Electrical Characteristics

Subgroup	Definition
1	Static characteristics specified in Figure 28 at +25°C
2	Static characteristics specified in Figure 28 at +125°C
3	Static characteristics specified in Figure 28 at -55°C
7	Functional characteristics specified in Figure 27 at +25°C
8A	Functional characteristics specified in Figure 27 at +125°C
8B	Functional characteristics specified in Figure 27 at -55°C
9	Switching characteristics specified in Figure 25 at +25°C
10	Switching characteristics specified in Figure 25 at +125°C
11	Switching characteristics specified in Figure 25 at -55°C

Figure 29: Definition of MIL-STD-883, Method 5005 Subgroups

PIN ASSIGNMENTS AND OUTLINES

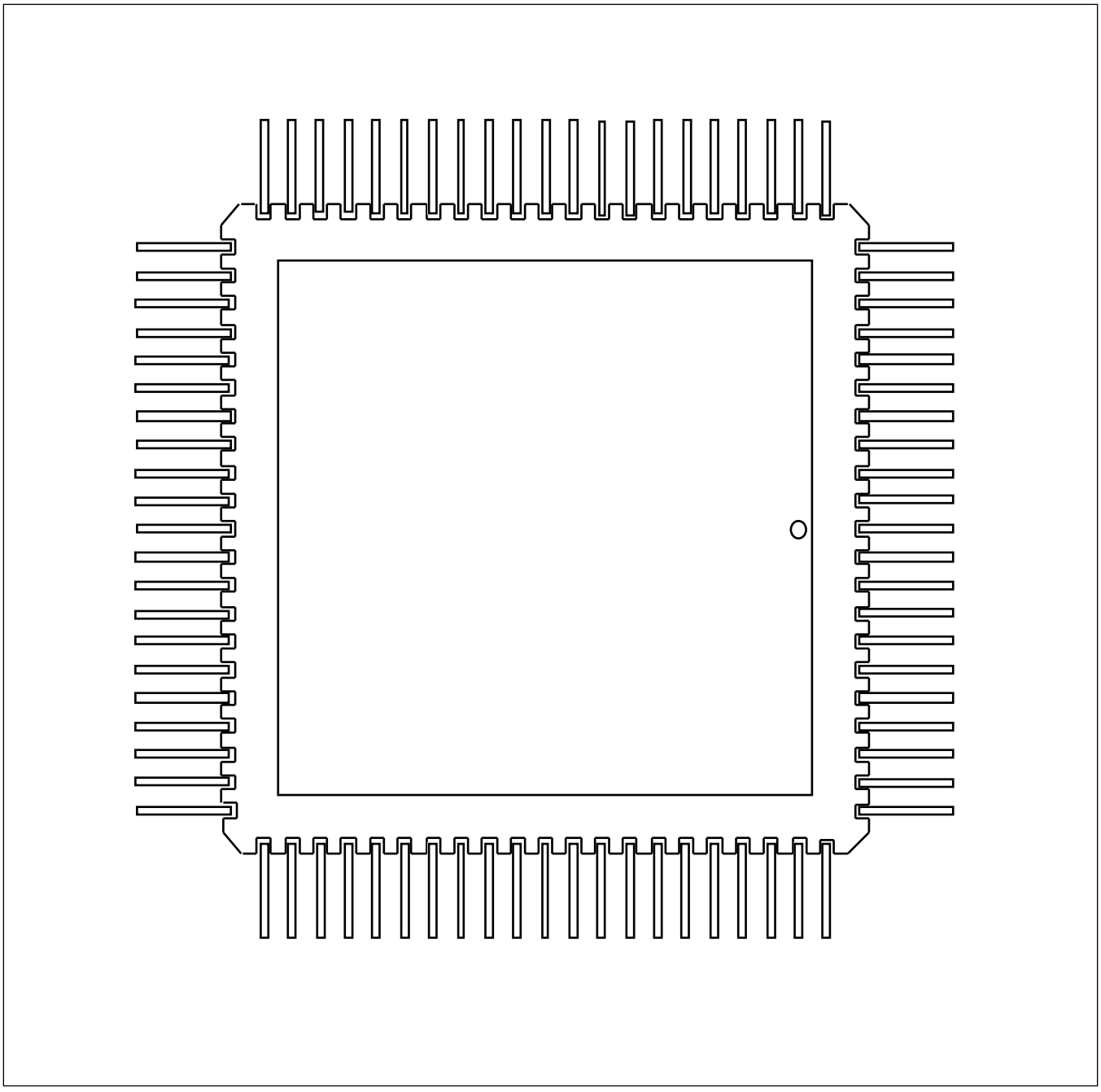


Figure 30: 84-Lead Flatpack - Package Style F

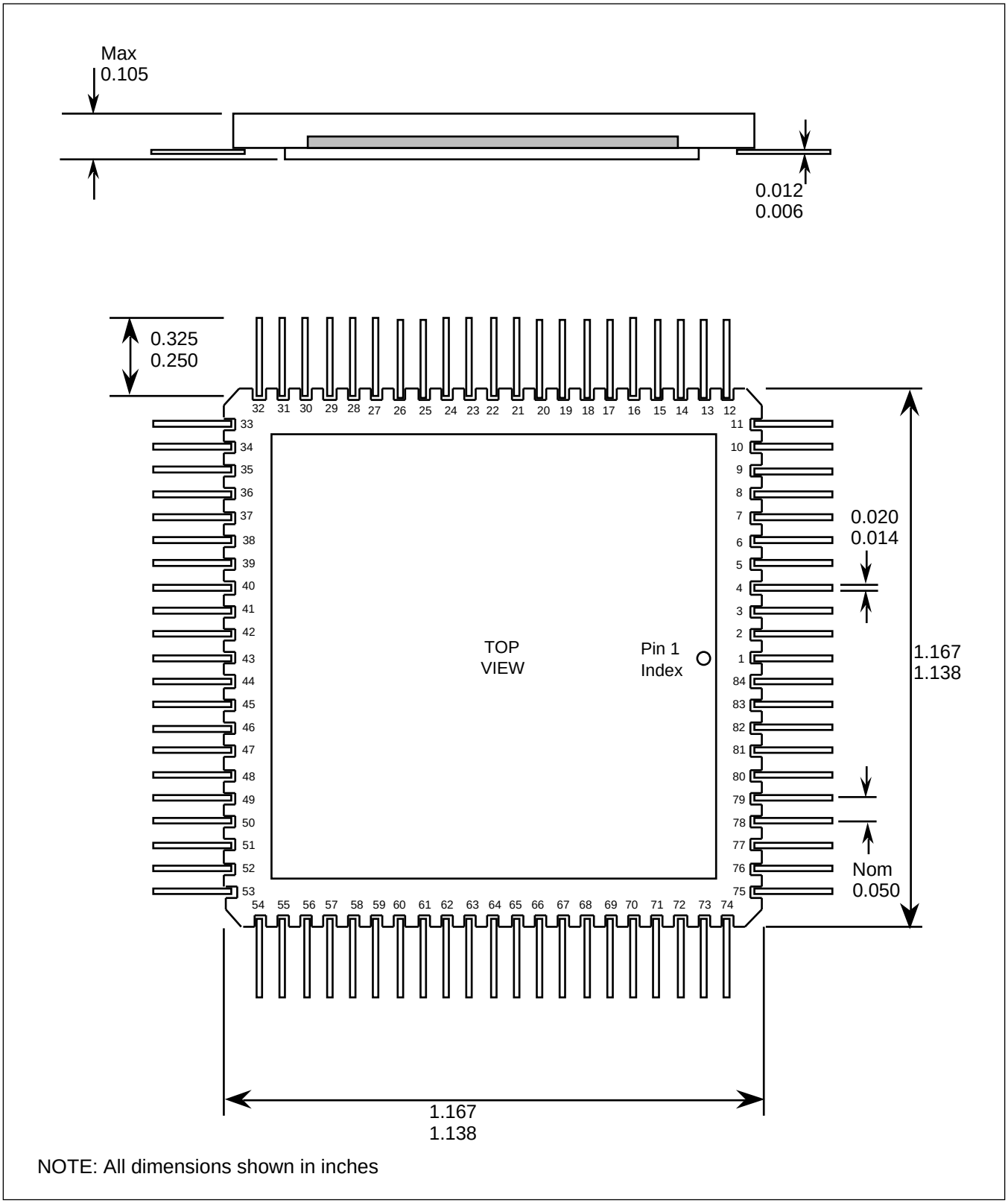
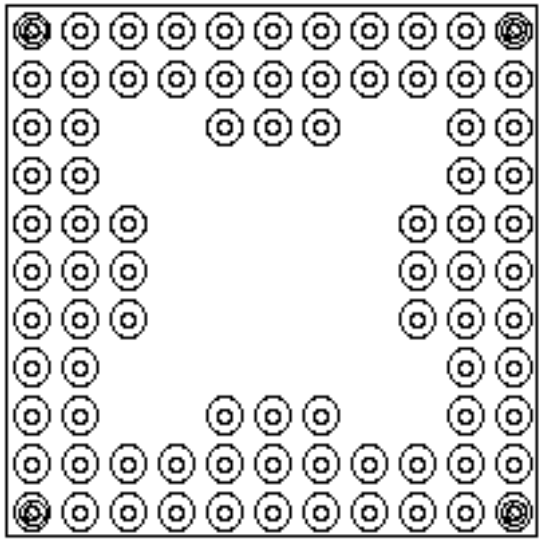
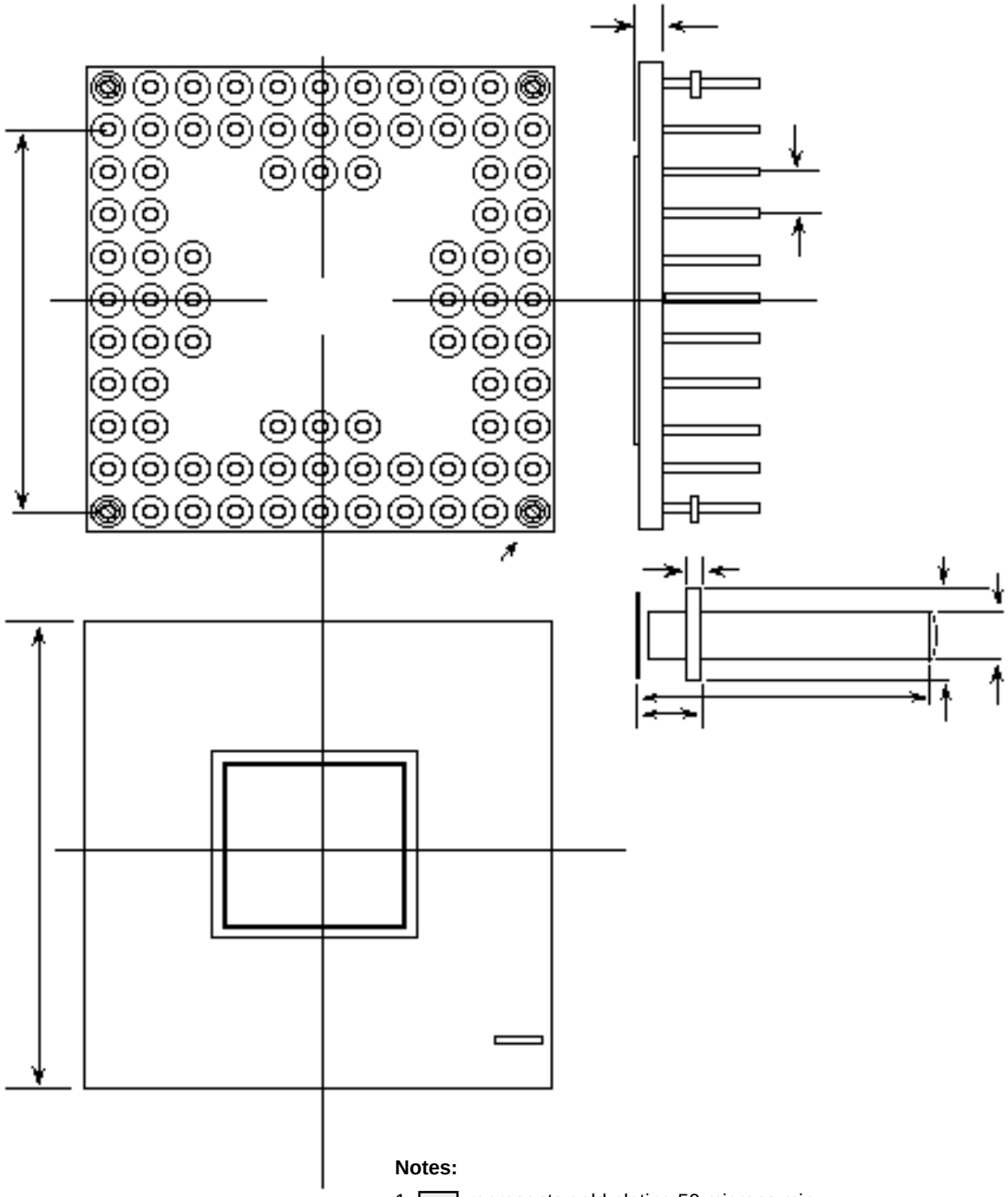


Figure 31: 84-Lead Flatpack - Package Style F



A1		B11		F9		K2	
A2		C1		F10		K3	
A3		C2		F11		K4	
A4		C5		G1		K5	
A5		C6		G2		K6	
A6		C7		G3		K7	
A7		C10		G9		K8	
A8		C11		G10		K9	
A9		D1		G11		K10	
A10		D2		H1		K11	
A11		D10		H2		L1	
B1		D11		H10		L2	
B2		E1		H11		L3	
B3		E2		J1		L4	
B4		E3		J2		L5	
B5		E9		J5		L6	
B6		E10		J6		L7	
B7		E11		J7		L8	
B8		F1		J10		L9	
B9		F2		J11		L10	
B10		F3		K1		L11	

Figure 32: 84-Pin Grid Array - Package Style A



Notes:

1. ▭ represents gold plating 50 microns min. over 100 microns nominal nickel.
2. All dimensions are in inches.
3. Default tolerances ±1% not less than 0.005
4. Ceramic is 92% Alumina.

Figure 33: 84-Pin Grid Array - Package Style A

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 test method 1019 Ionizing Radiation (total dose).

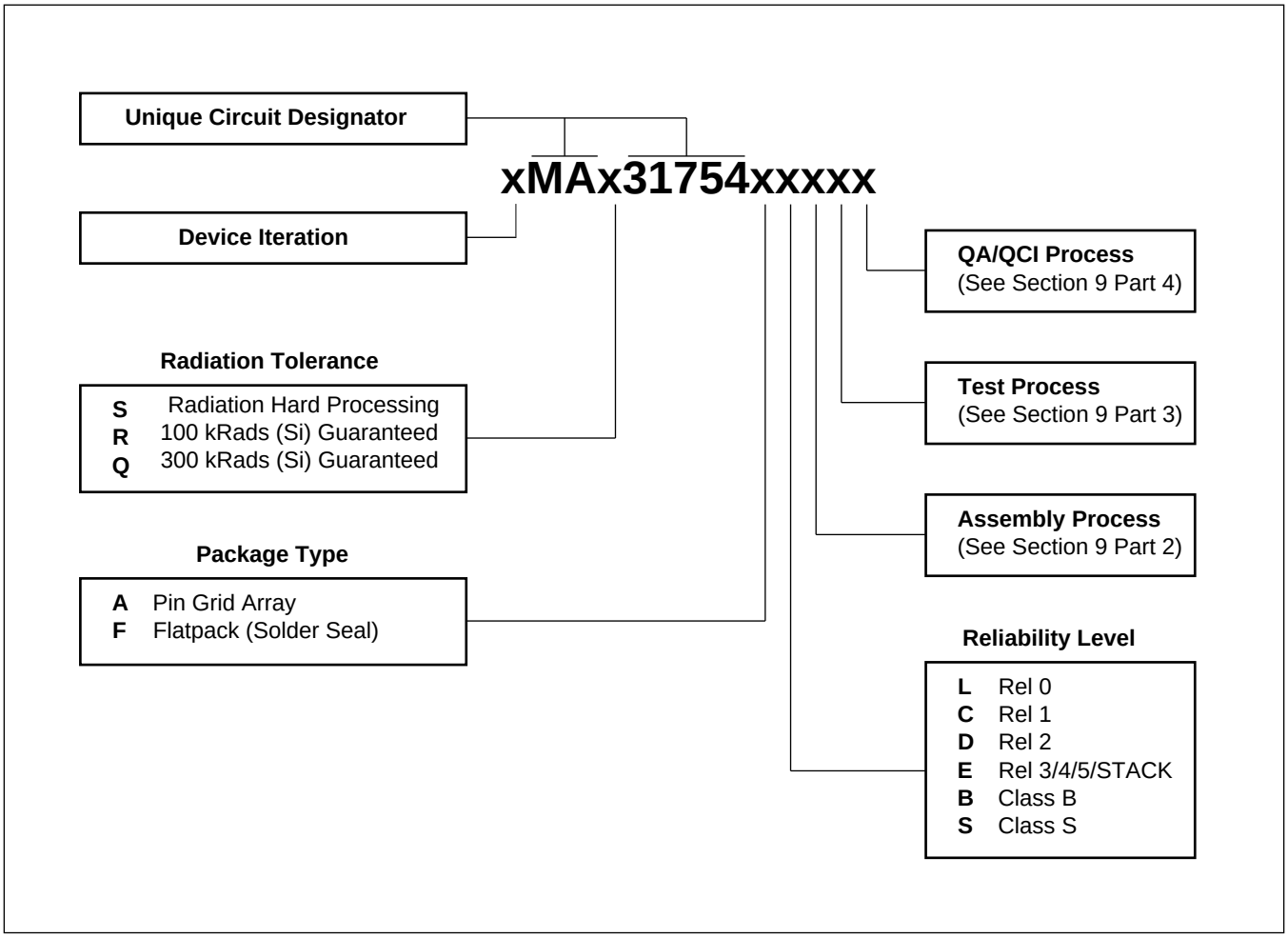
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 34: Radiation Hardness Parameters

ORDERING INFORMATION



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 Publication No. DS3826-3.6 March 1995

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