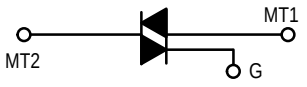
Triacs
Silicon Bidirectional Thyristors

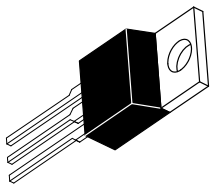
. . . designed primarily for full-wave ac control applications, such as solid-state relays, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Three Modes (MAC320 Series) or Four Modes (MAC320A Series)

MAC320 Series
MAC320A Series

TRIACs
20 AMPERES RMS
200 thru 800 VOLTS





CASE 221A-04
(TO-220AB)
STYLE 4

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage(1) (T_J = –40 to +125°C, 1/2 Sine Wave 50 to 60 Hz, Gate Open) MAC320-4, MAC320A4 MAC320-6, MAC320A6 MAC320-8, MAC320A8 MAC320-10, MAC320A10	V_{DRM}	 200 400 600 800	Volts
Peak Gate Voltage	V_{GM}	10	Volts
On-State Current RMS (T_C = +75°C) (Full Cycle, Sine Wave, 50 to 60 Hz)	$I_{T(RMS)}$	20	Amp
Peak Surge Current (One Full Cycle, 60 Hz, T_C = +75°C) preceded and followed by rated current	I_{TSM}	150	Amp
Peak Gate Power (T_C = +75°C, Pulse Width = 2 μs)	P_{GM}	20	Watts
Average Gate Power (T_C = +75°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
Peak Gate Current	I_{GM}	2	Amp
Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.8	°C/W

1. V_{DRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (V_D Rated V_{DRM}, Gate Open) T_J = 25°C	I_{DRM}	—	—	10	μA
T_J = +125°C		—	—	2	mA
Peak On-State Voltage (Either Direction) (I_{TM} = 28 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%)	V_{TM}	—	1.4	1.7	Volts
Gate Trigger Current (Continuous dc) (Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms)	I_{GT}				mA
MT2 (+), G(+); MT2 (+), G(–); MT2 (–), G(–)		—	—	50	
MT2 (–), G(+) "A" SUFFIX ONLY		—	—	75	
Gate Trigger Voltage (Continuous dc) (Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms)	V_{GT}				Volts
MT2 (+), G(+); MT2 (+), G(–); MT2 (–), G(–)		—	0.9	2	
MT2 (–), G(+) "A" SUFFIX ONLY		—	1.4	2.5	
(Main Terminal Voltage = Rated V_{DRM}, R_L = 10 kΩ, T_J =+110°C)					
MT2 (+), G(+); MT2 (–), G(–); MT2 (+), G(–);		0.2	—	—	
MT2 (–), G(+) "A" SUFFIX ONLY		0.2	—	—	
Holding Current (Either Direction) (Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 200 mA)	I_H	—	6	40	mA
Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 28 A, I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs)	t_{gt}	—	1.5	—	μs
Critical Rate of Rise of Commutation Voltage (V_D = Rated V_{DRM}, I_{TM} = 28 A, Commutating di/dt = 10 A/ms, Gate Unenergized, T_C = +75°C)	dv/dt(C)	—	5	—	V/μs

FIGURE 1 — RMS CURRENT DERATING

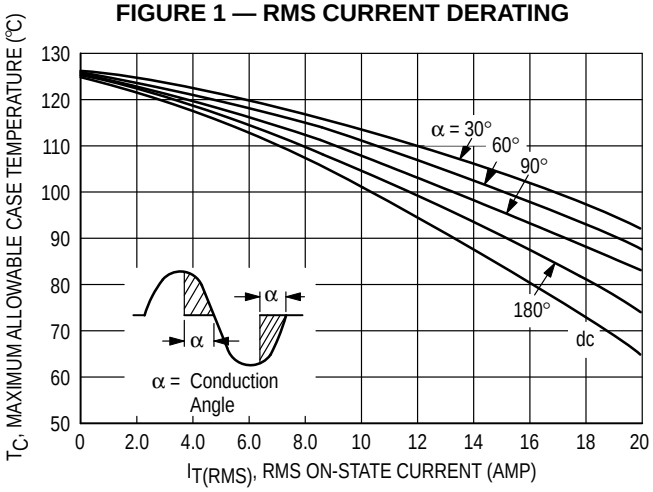


FIGURE 2 — ON-STATE POWER DISSIPATION

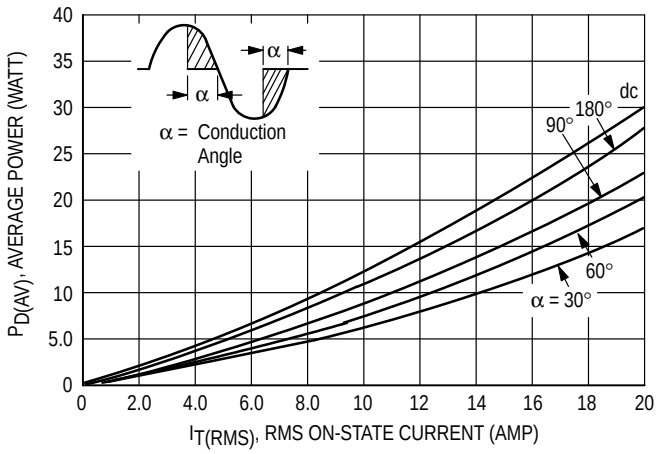


FIGURE 3 — TYPICAL GATE TRIGGER VOLTAGE

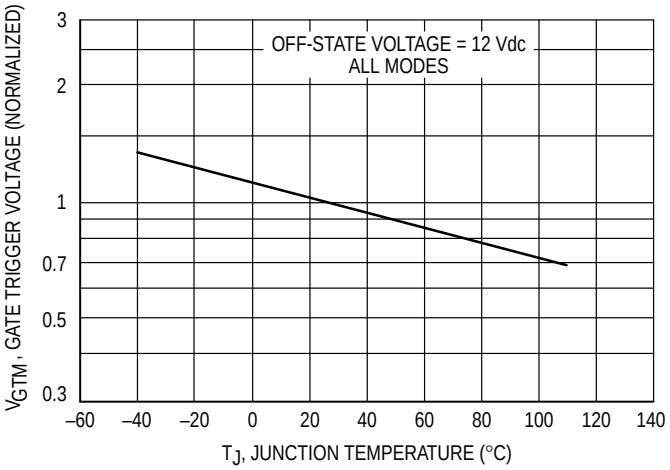


FIGURE 4 — TYPICAL GATE TRIGGER CURRENT

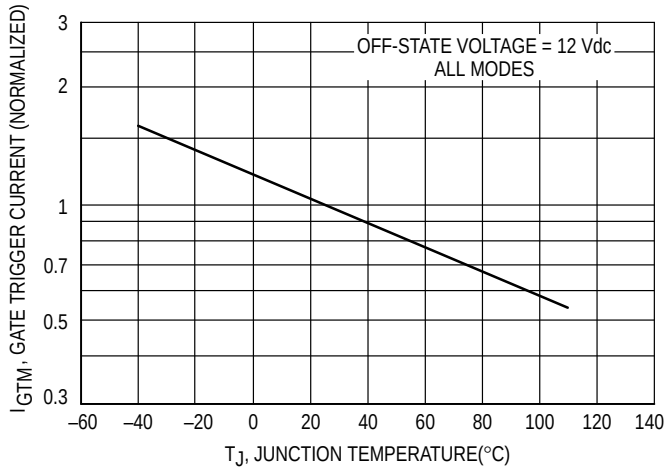


FIGURE 5 — MAXIMUM ON-STATE CHARACTERISTICS

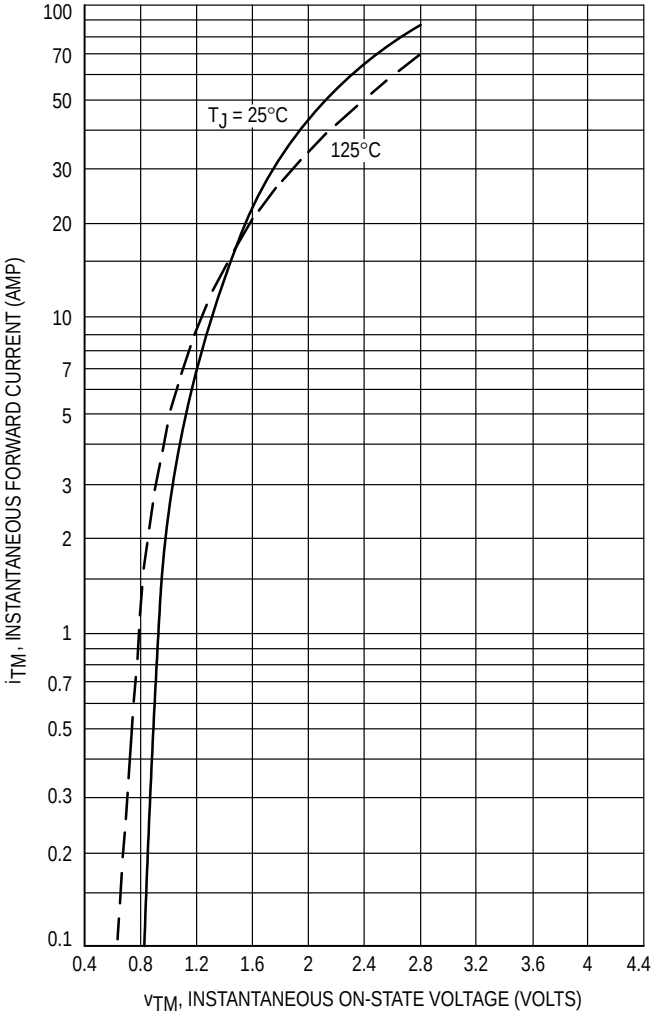


FIGURE 6 — TYPICAL HOLDING CURRENT

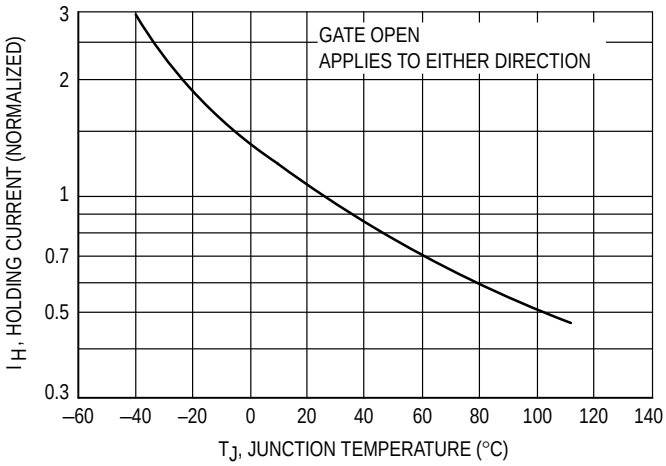


FIGURE 7 — MAXIMUM ON-REPETITIVE SURGE CURRENT

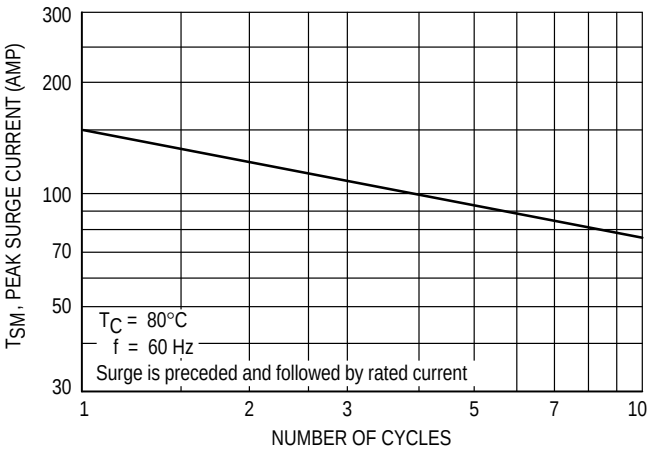
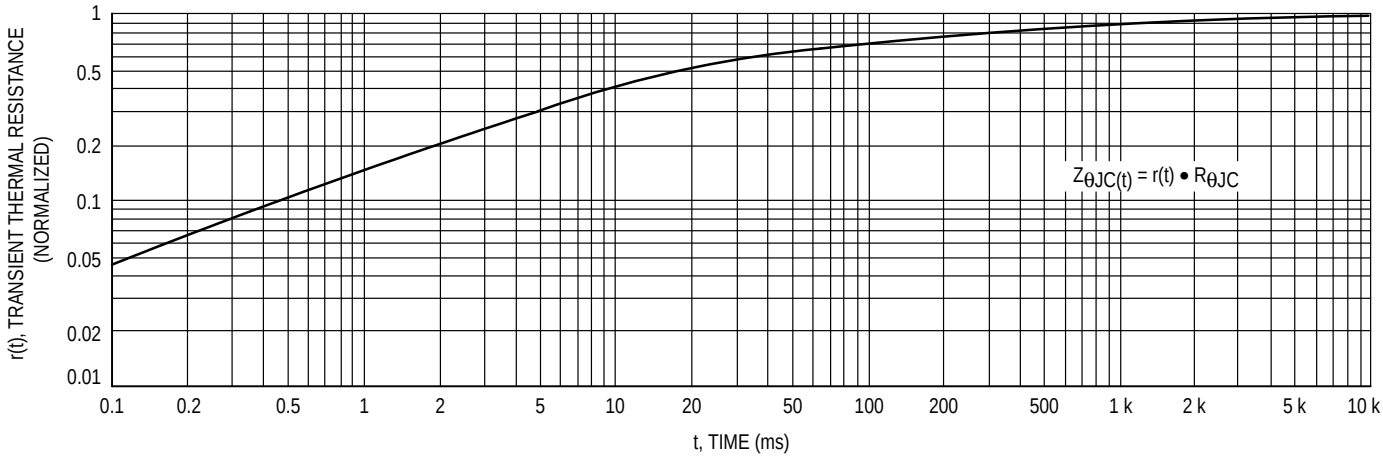
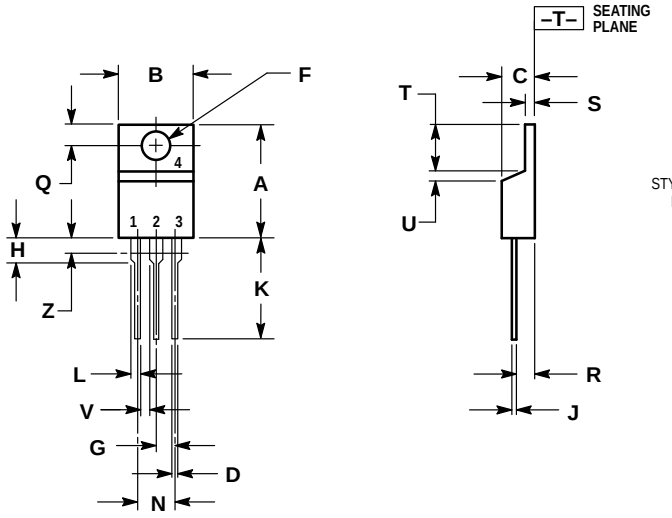


FIGURE 8 — THERMAL RESPONSE



PACKAGE DIMENSIONS



STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.022	0.36	0.55
K	0.500	0.562	12.70	14.27
L	0.045	0.055	1.15	1.39
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A-04
(TO–220AB)

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