MA9187

RADIATION HARD 65536 x 1 BIT STATIC RAM

The MA9187 64k Static RAM is configured as 65536 x 1 bits and manufactured using GPS's CMOS-SOS high performance, radiation hard, 1.5µm technology.

The device has separate input and output terminals controlled by Chip Select and Write Enable. The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when Chip Select is in the high state.

See Application Note "Overview of the GPS Radiation Hard 1.5µm CMOS/SOS SRAM Range".

$\overline{CS}$	$\overline{WE}$	Mode	V_{DD} Current	Output Pin
H	X	Deselected	I_{SB2}	High Z
L	H	Read	I_{SB1}	D_{OUT}
L	L	Write	I_{SB1}	High Z

Figure 1: Truth Table

FEATURES

- 1.5µm CMOS-SOS Technology
- Latch-up Free
- Fast Access Time 45ns Typical
- Total Dose 10^6 Rad(Si)
- Transient Upset >10^{11} Rad(Si)/sec
- SEU 4.3 x 10^{-11} Errors/bitday
- Single 5V Supply
- All Inputs and Outputs Fully TTL or CMOS Compatible
- Fully Static Operation
- Three State Output
- Low Standby Current 100µA Typical
- -55°C to +125°C Operation

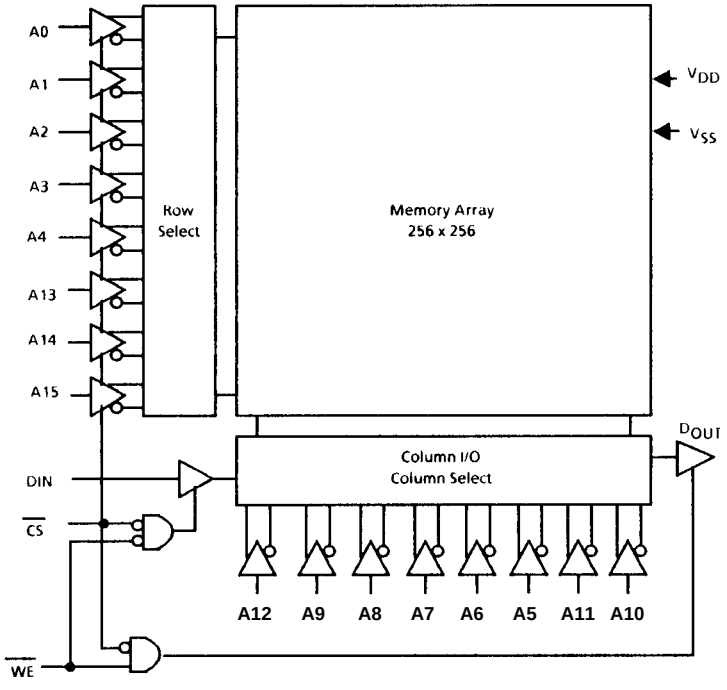


Figure 2: Block Diagram

CHARACTERISTICS AND RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	-0.5	7	V
V_I	Input Voltage	-0.3	V_{DD}+0.3	V
T_A	Operating Temperature	-55	125	°C
T_S	Storage Temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functlonal operation of the device at these condltions, or at any other condition above those indicated in the operations section of this specification, is not Implied Exposure to absolute maxlmum rating conditions for extended perlods may affect device reliability.

Figure 3: Absolute Maximum Ratings

Notes for Tables 4 and 5:
Characteristics apply to pre radiation at T_A = -55°C to +125°C with V_{DD} = 5V ±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10% (characteristics at higher levels available on request). Group A Subgroups 1, 2, 3.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-		4.5	5.0	5.5	V
V_{IH}	Logical '1' Input Voltage	-	TTL CMOS	V_{DD}/2 0.8 V_{DD}	- -	V_{DD} V_{DD}	V V
V_{IL}	Logical '0' Input Voltage	-	TTL CMOS	V_{SS} V_{SS}	- -	0.8 0.2 V_{DD}	V V
V_{OH1}	Logical '1' Output Voltage	I_{OH1} = -4mA		2.4	-	-	V
V_{OH2}	Logical '1' Output Voltage	I_{OH2} = -3mA		V_{DD} -0.5	-	-	V
V_{OL}	Logical '0' Output Voltage	I_{OL} = 8mA		-	-	0.4	V
I_{LI}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS} All inputs		-	-	±10	µA
I_{LO}	Output Leakage Current	Chip disabled, V_{OUT} = V_{DD} or V_{SS}		-	-	±10	µA
I_{SB1}	Selected Static Current (CMOS)	All inputs = V_{DD} -0.2V except $\overline{CS}$ = V_{SS} +0.2V	90ns 60ns 45ns	- - -	0.1 0.1 -	10 10 TBD	mA mA
I_{DD}	Dynamic Operating Current (CMOS)	f_{RC} = 1MHz, all inputs switching, V_{IH} = V_{DD} -0.2V	90ns 60ns 45ns	- - -	3 3 -	13 13 TBD	mA mA
I_{SB2}	Standby Supply Current	$\overline{CS}$ = V_{DD} -0.2V	90ns 60ns 45ns	- - -	0.1 0.1 -	10 10 TBD	mA mA

Figure 4: Electrical Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS}$ = V_{DR}		2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS}$ = V_{DR}, V_{DR} = 2.0V	90ns 60ns 45ns	- - -	0.05 0.05 -	4 4 TBD	mA mA

Figure 5: Data Retention Characteristics

AC CHARACTERISTICS

Conditions of Test for Tables 5 and 6:
1. Input pulse = V_{SS} to 3V (TTL) and V_{SS} to 4V (CMOS).
2. Times measurement reference level = 1.5V.
3. Input Rise and Fall times ≤5ns.
4. Output load 1TTL gate and CL = 60pF.
5. Transition is measured at ±500mV from steady state.
6. This parameter is sampled and not 100% tested.

Notes for Tables 6 and 7:
Characteristics apply to pre-radiation at T_A = -55°C to +125°C with V_{DD} = 5V±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10%. GROUP A SUBGROUPS 9, 10, 11.

Symbol	Parameter	MAX9187X45		MAX9187X60		MAX9187X90		Units
		Min	Max	Min	Max	Min	Max	
T_{AVAVR}	Read Cycle Time	45	-	60	-	90	-	ns
T_{AVQV}	Address Access Time	-	45	-	60	-	90	ns
T_{ELQV}	Chip select Access time	-	45	-	60	-	90	ns
T_{ELQX} (5,6)	Chip Selection to Output in Low Z	15	-	15	-	15	-	ns
T_{EHQZ} (5,6)	Chip Deselection to Output in High Z	0	20	0	20	0	20	ns
T_{AXQX}	Output Hold from Address change	15	-	20	-	30	-	ns

Figure 6: Read Cycle AC Electrical Characteristics

Symbol	Parameter	MAX9187X45		MAX9187X60		MAX9187X90		Units
		Min	Max	Min	Max	Min	Max	
T_{AVAVW}	Write~Cycle Tlme	40	-	50	-	60	-	ns
T_{ELWH}	Chip Selection to End of Write	35	-	40	-	50	-	ns
T_{AVWH}	Address Valid to End of Write	35	-	40	-	50	-	ns
T_{AVWL}	Address Set Up Time	0	-	0	-	0	-	ns
T_{WLWH}	Write Pulse Width	28	-	30	-	35	-	ns
T_{WHAV}	Write Recovery Time	0	-	0	-	0	-	ns
T_{WLQZ} (5,6)	Wnte to Output in High Z	0	20	0	20	0	20	ns
T_{DVWH}	Data to Write Time Overlap	18	-	20	-	25	-	ns
T_{WHDX}	Data Hold from Write	0	-	0	-	0	-	ns
T_{WHQX} (5,6)	Output Active from End to Write	0	20	0	20	0	20	ns

Figure 7: Write Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

Note: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Figure 8: Capacitance

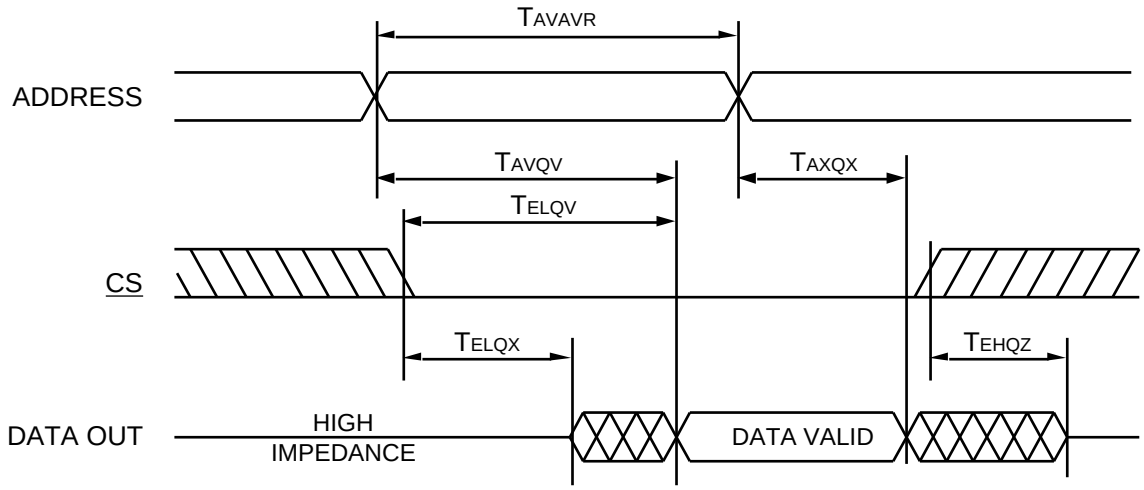
Symbol	Parameter	Conditions
F_T	Basic Functionality	V_{DD} = 4.5V - 5.5V, FREQ = 1MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} \leq 1.5V$, $V_{OH} \geq 1.5V$ TEMP = -55°C to +125°C, GPS PATTERN SET GROUP A SUBGROUPS 7, 8A, 8B

Figure 9: Functionality

Subgroup	Definition
1	Static characteristics specified in Tables 4 and 5 at +25°C
2	Static characteristics specified in Tables 4 and 5 at +125°C
3	Static characteristics specified in Tables 4 and 5 at -55°C
7	Functional characteristics specified in Table 9 at +25°C
8A	Functional characteristics specified in Table 9 at +125°C
8B	Functional characteristics specified in Table 9 at -55°C
9	Switching characteristics specified in Tables 6 and 7 at +25°C
10	Switching characteristics specified in Tables 6 and 7 at +125°C
11	Switching characteristics specified in Tables 6 and 7 at -55°C

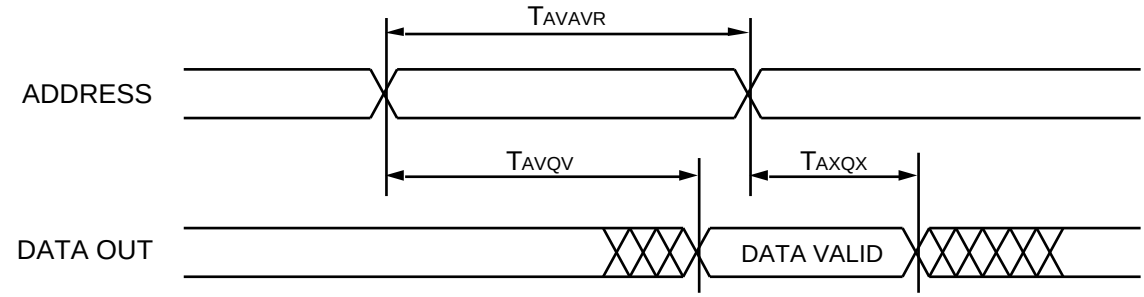
Figure 10: Definition of Subgroups

TIMING DIAGRAMS



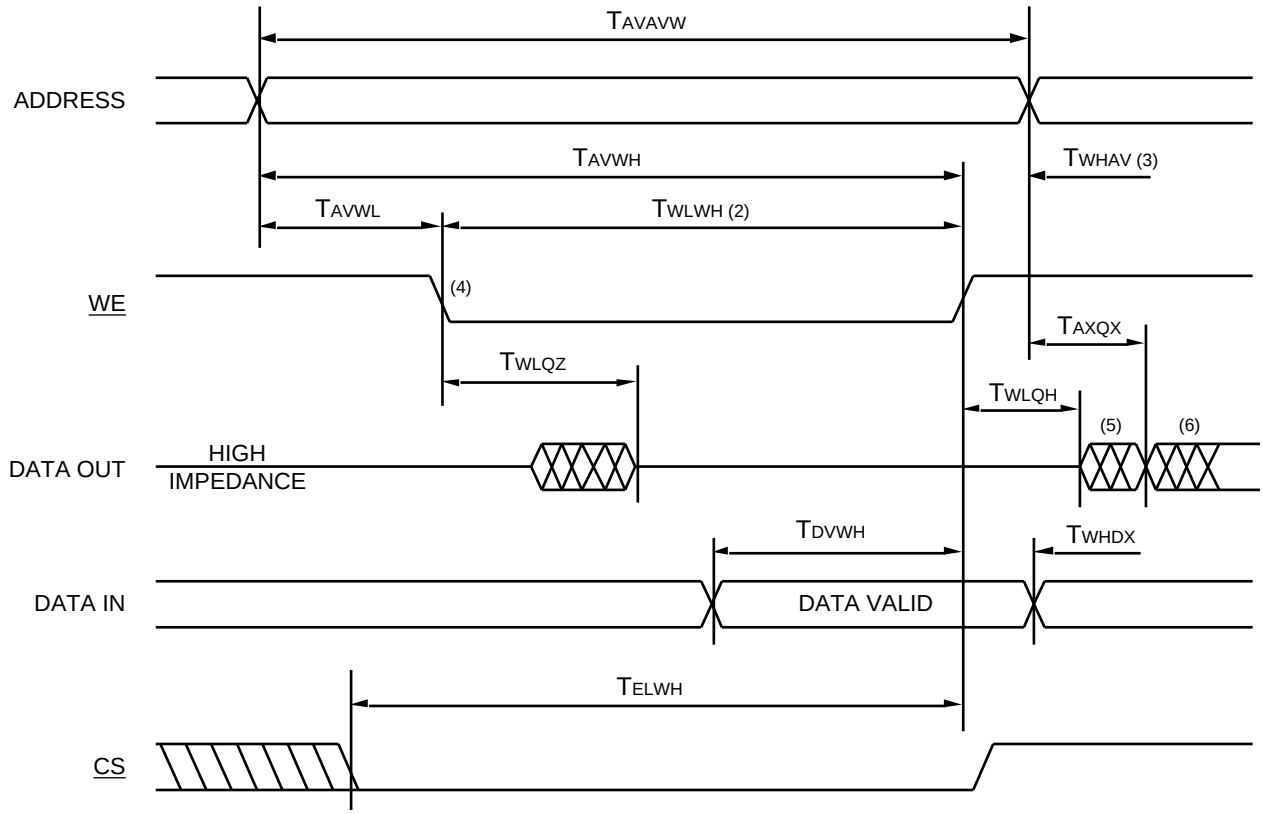
1. WE is high for Read Cycle.
2. Address Vaild prior to or coincident with CS transition low.

Figure 11: Read Cycle 1



1. WE is high for Read Cycle.
2. Device is continually selected. CS low.

Figure 12: Read Cycle 2

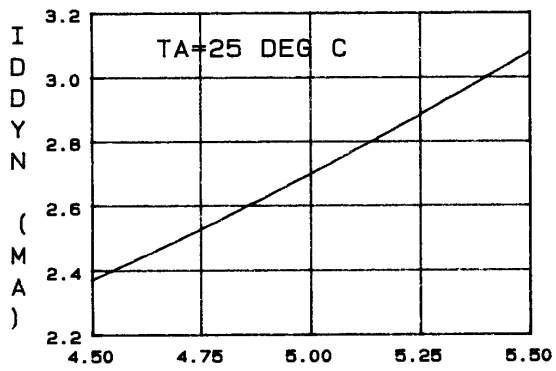


1. WE must be high during all address transitions.
2. A write occurs during the overlap (T_{WLWH}) of a low CS and a low WE.
3. T_{WHAV} is measured from either CS or WE going high, whichever is the earlier, to the end of the write cycle.
4. If the CS low transition occurs simultaneously with, or after, the WE low transition, the output remains in the high impedance state.
5. DATA OUT is the write data of the current cycle, if selected.
6. DATA OUT is the read data of the next address, if selected.

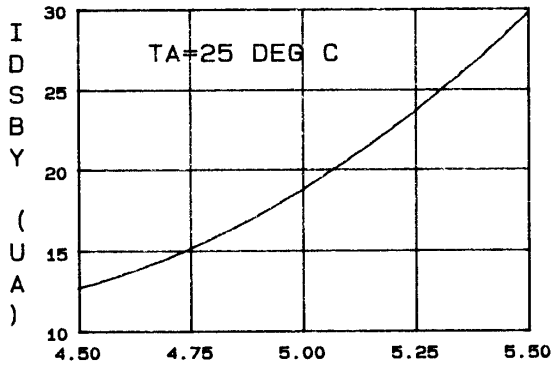
Figure 13: Write Cycle

TYPICAL PERFORMANCE CHARACTERISTICS MAx9187x60

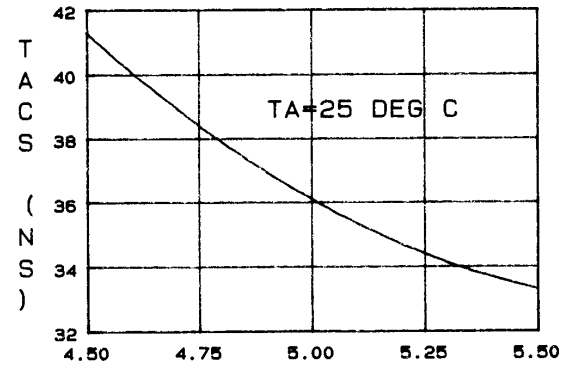
DYNAMIC CURRENT VS SUPPLY VOLTAGE



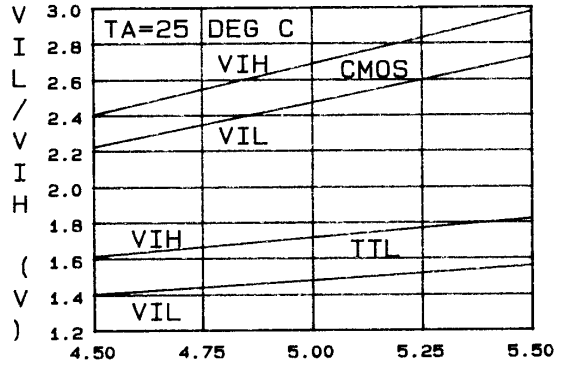
STANDBY CURRENT VS SUPPLY VOLTAGE



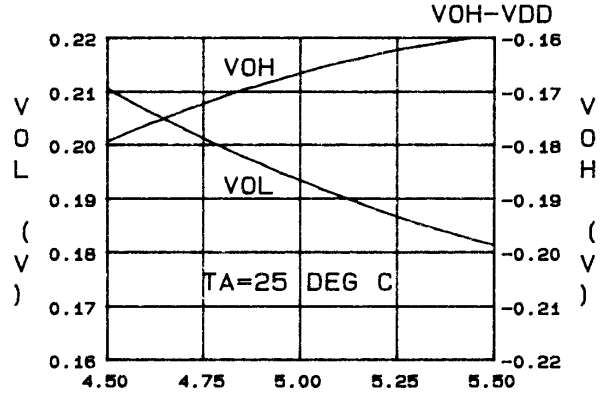
CS ACCESS TIME VS SUPPLY VOLTAGE



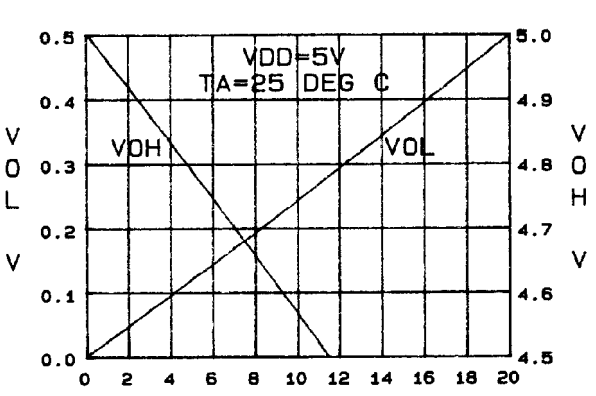
INPUT LEVELS VS SUPPLY VOLTAGE



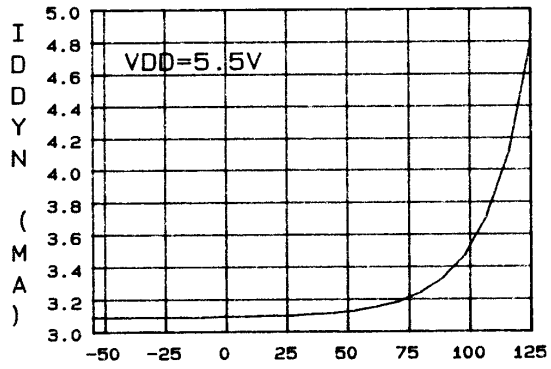
OUTPUT LEVELS VS SUPPLY VOLTAGE



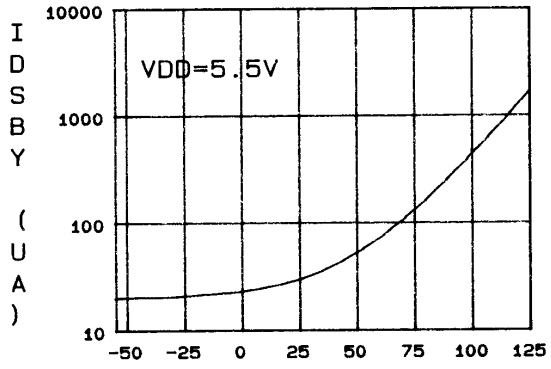
OUTPUT VOLTAGE VS CURRENT



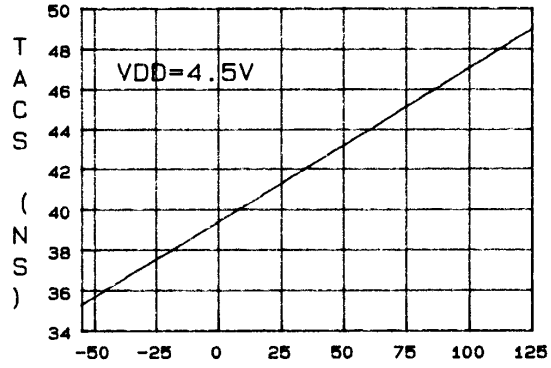
DYNAMIC CURRENT VS TEMPERATURE



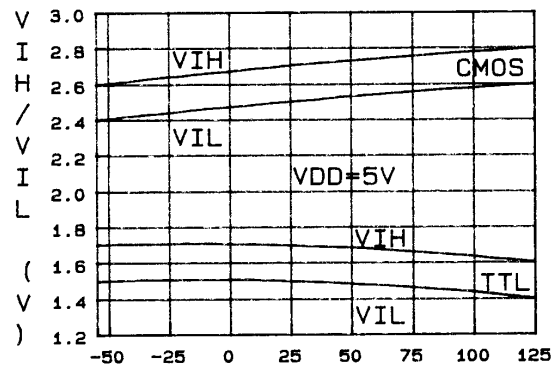
STANDBY CURRENT VS TEMPERATURE



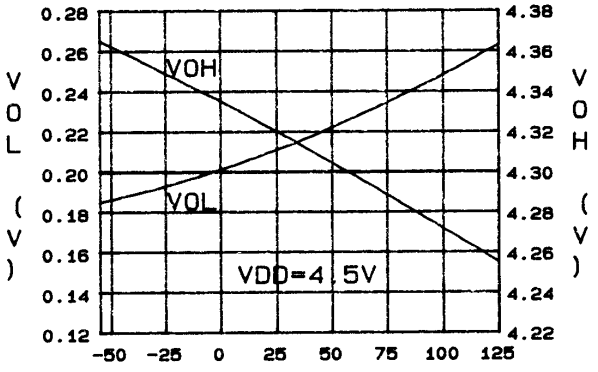
CS ACCESS TIME VS TEMPERATURE



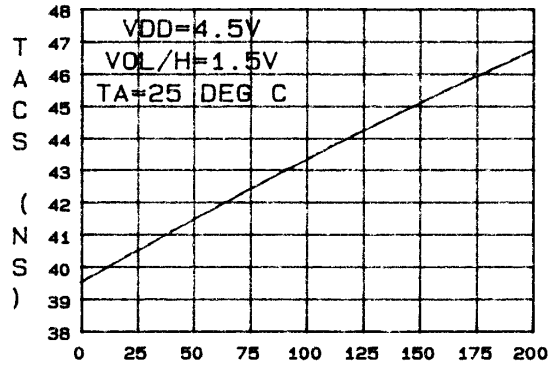
INPUT LEVELS VS TEMPERATURE



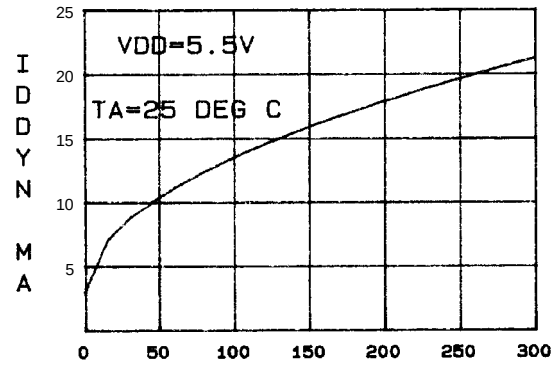
OUTPUT LEVELS VS TEMPERATURE



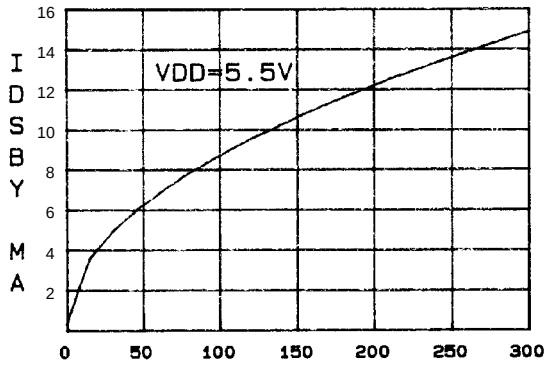
CS ACCESS TIME VS OUTPUT LOAD



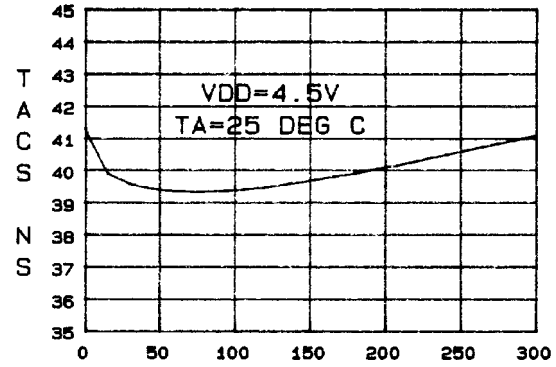
DYNAMIC CURRENT VS RADIATION



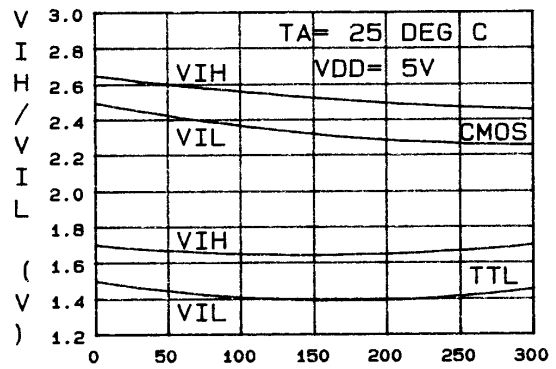
STANDBY CURRENT VS RADIATION



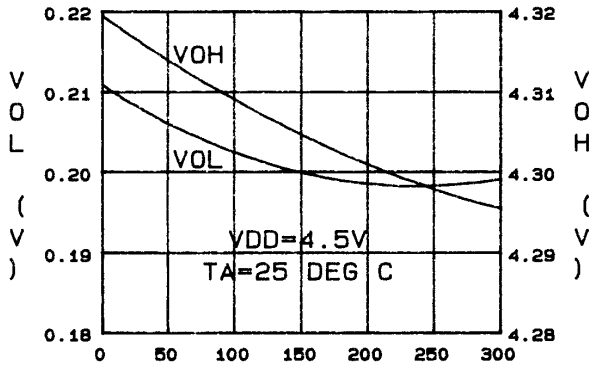
CS ACCESS TIME VS RADIATION



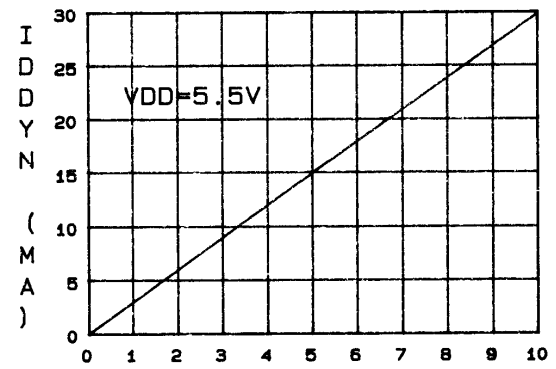
INPUT LEVELS VS RADIATION



OUTPUT LEVELS VS RADIATION



DYNAMIC CURRENT VS FREQUENCY



PIN ASSIGNMENTS

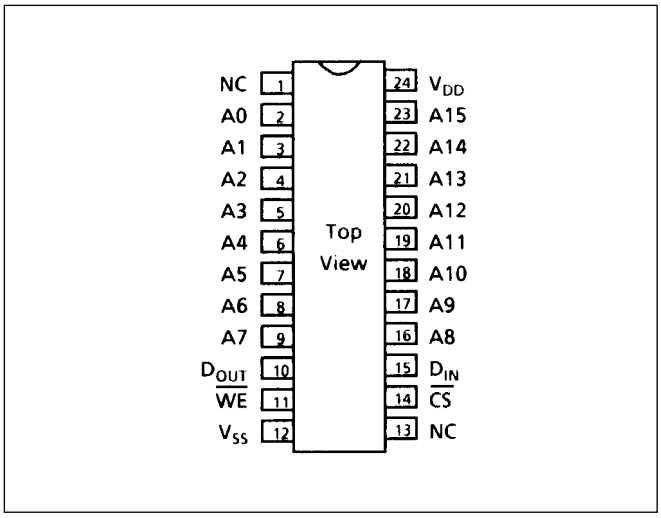


Figure 14: 24 Lead Ceramic DIL (Solder Seal) - Package Style C

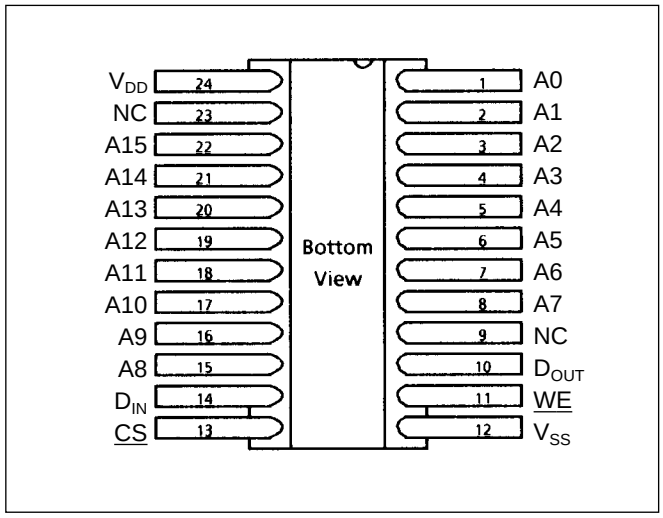


Figure 15: 24 Lead Ceramic Flatpack (Solder Seal) - Package Style B

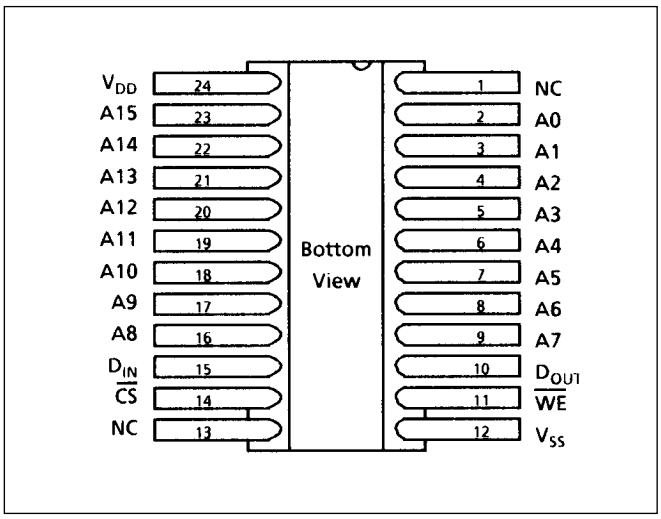


Figure 16: 24 Lead Ceramic Flatpack (Solder Seal) - Package Style F

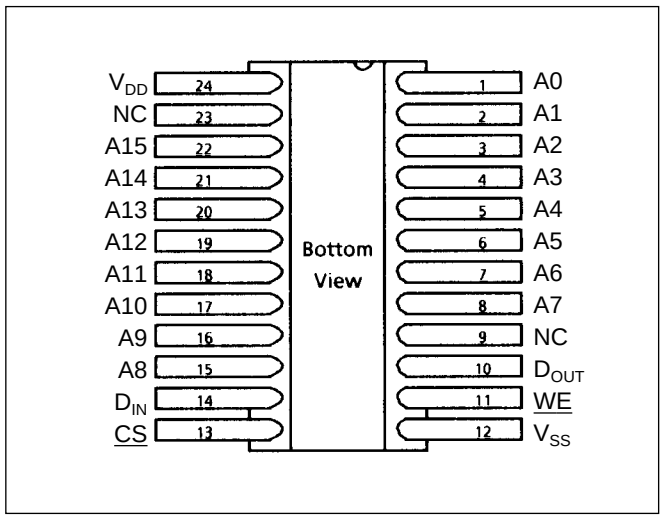


Figure 17: 24 Lead Ceramic Flatpack (Solder Seal) - Package Style Y

OUTLINES Dimensions are shown in mm (in)

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	30.79	-	-	1.212
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

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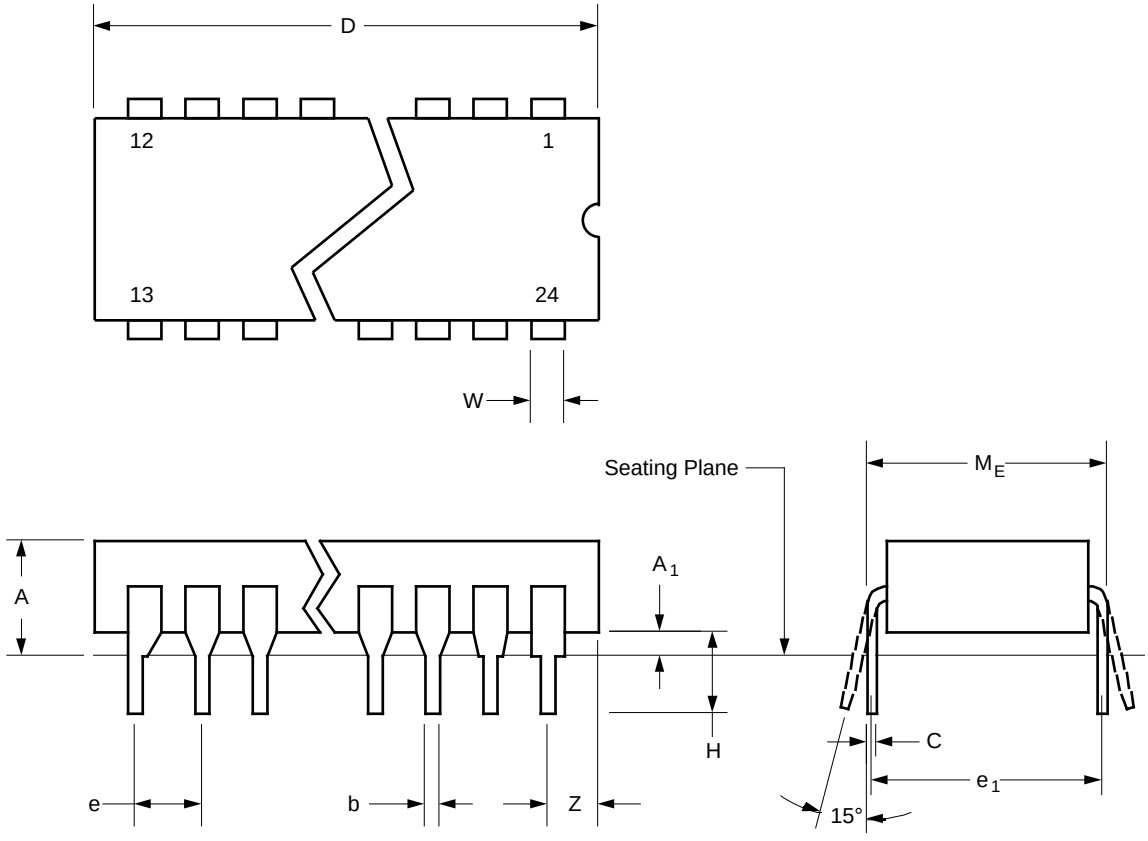
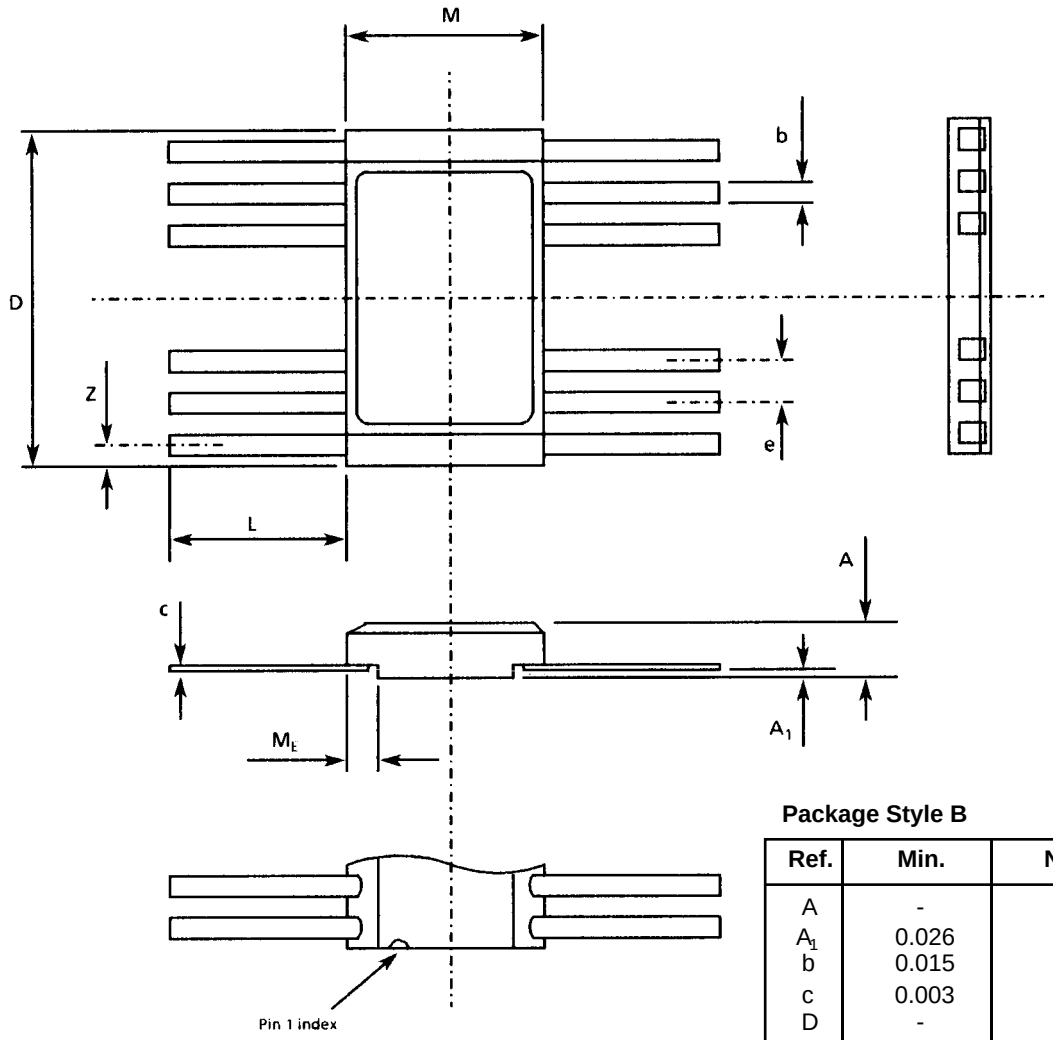


Figure 18: 24 Lead Ceramic DIL (Solder Seal) - Package Style C



Package Style B

Ref.	Min.	Nom.	Max.
A	-	-	0.115
A_1	0.026	-	0.035
b	0.015	-	0.019
c	0.003	-	0.006
D	-	-	0.600
e	-	0.050 Typ.	-
L	0.385	-	0.405
M	0.392	-	0.408
M_E	0.030	-	-
Z	0.005	-	0.045
Dimensions in inches			

XG745

Package Style F

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	3.07	-	-	0.121
A1	0.66	-	-	0.026	-	-
b	0.38	-	0.48	0.015	-	0.019
c	0.08	-	0.152	0.003	-	0.006
D	14.99	-	15.50	0.590	-	0.610
e	-	2.54	-	-	0.050	-
L	6.73	-	7.75	0.265	-	0.305
M	9.96	-	10.36	0.392	-	0.408
Me	7.6	-	-	0.30	-	-
Z	0.13	-	1.14	0.005	-	0.045

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Package Style Y

Ref.	Min.	Nom.	Max.
A	-	-	0.115
A_1	0.026	-	0.035
b	0.015	-	0.019
c	0.003	-	0.006
D	-	-	0.600
e	-	0.050 Typ.	-
L	0.330	-	-
M	0.392	-	0.408
M_E	0.030	-	-
Z	0.005	-	0.045
Dimensions in inches			

XG146

Figure 19: 24 Lead Ceramic Flatpack (Solder Seal) - Package Styles B, F and Y

Function	Pin Number		Via	Static 1	Static 2	Dynamic	Radiation
	Pkg. Opt.	Pkg. Opt.					
A0	1	2	R1	0V	6v	F2	5V
A1	2	3	R1	0V	6v	F3	5V
A2	3	4	R1	0V	6v	F4	5V
A3	4	5	R1	0V	6v	F5	5V
A4	5	6	R1	0V	6v	F6	5V
A5	6	7	R1	0V	6v	F7	5V
A6	7	8	R1	0V	6v	F8	5V
A7	8	9	R1	0V	6v	F9	5V
DOUT	10	10	R2	0V	6v	3V	5V
WEB	11	11	R1	0V	6v	F0	5V
VSS	12	12	Direct	0V	0V	0V	0V
CSB	13	14	R1	0V	6v	F18	5V
DIN	14	15	R1	0V	6v	F1	5V
A8	15	16	R1	0V	6v	F10	5V
A9	16	17	R1	0V	6v	F11	5V
A10	17	18	R1	0V	6v	F12	5V
A11	18	19	R1	0V	6v	F13	5V
A12	19	20	R1	0V	6v	F14	5V
A13	20	21	R1	0V	6v	F15	5V
A14	21	22	R1	0V	6v	F16	5V
A15	22	23	R1	0V	6v	F17	5V
VDD	24	24	Direct	6v	6v	6v	5V

1. Static 1, Static 2 and Dynamic: R1=1k2, R2=330Ω
2. Radiation: R1 =10k, R2=10k
3. F0=100kHz, F1=F0/2, F2=F0/4, F3=F0/8 etc.

Figure 20: Burnin and Radiation Configuration

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$4.3x10^{-11}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 21: Radiation Hardness Parameters

SINGLE EVENT UPSET CHARACTERISTICS

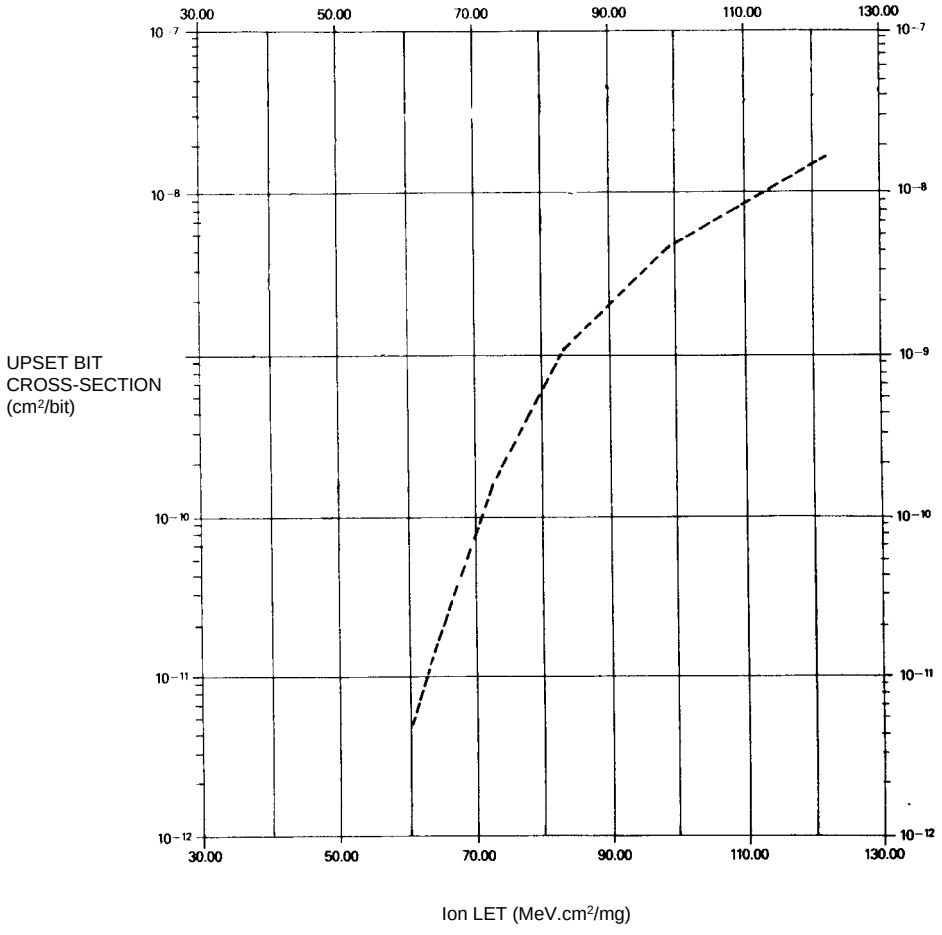
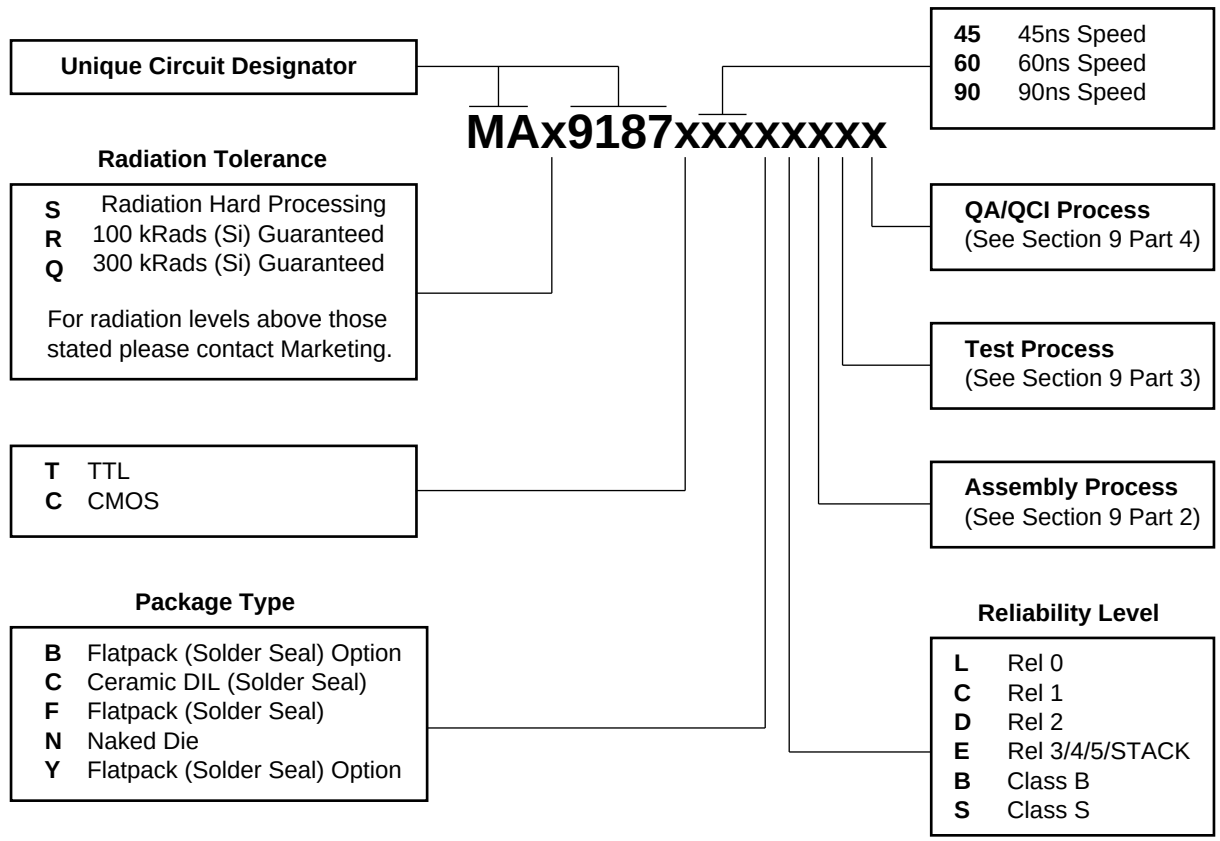


Figure 22: Typical Per-Bit Upset Cross-Section v Ion LET

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

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 Publication No. DS3480-3.2 April 1995

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