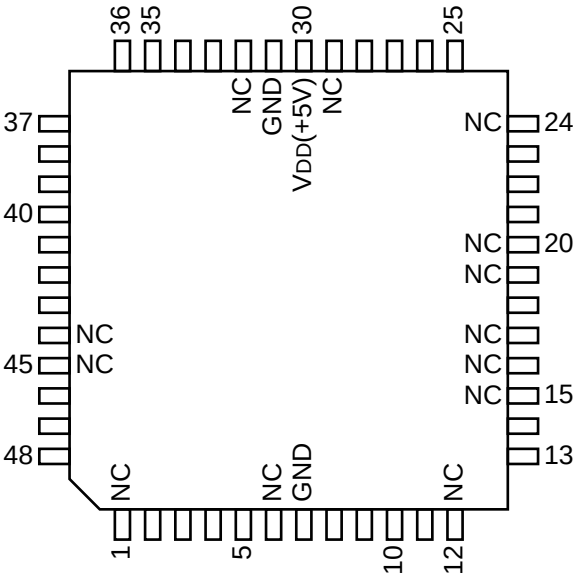
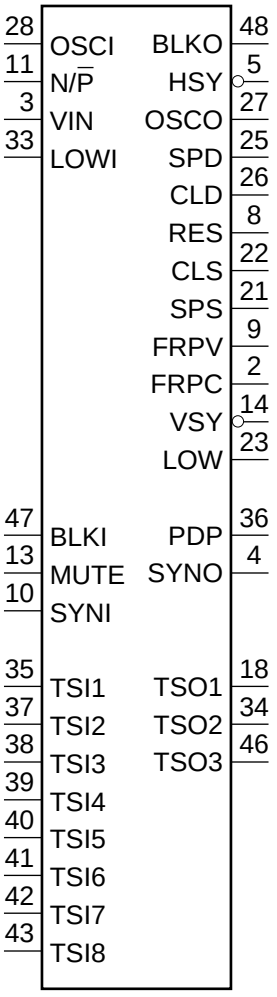
C-MOS TFT-LCD MODULE TIMING CONTROL

—TOP VIEW—





(VDD =+5V)

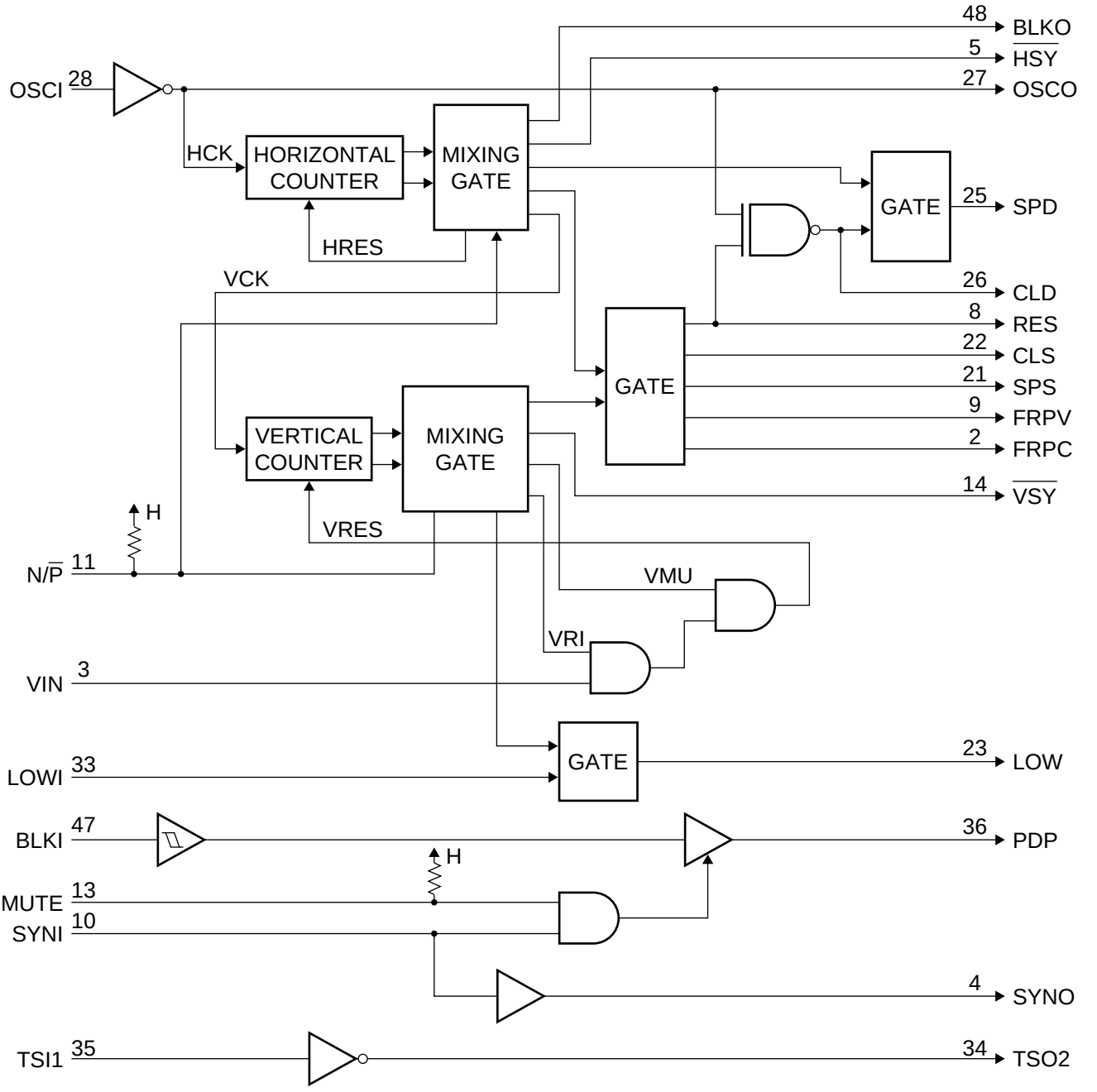
PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	NC	13	I	MUTE	25	O	SPD	37	I	TSI 2
2	O	FRPC	14	O	$\overline{VSY}$	26	O	CLD	38	I	TSI 3
3	I	VIN	15	—	NC	27	O	OSCO	39	I	TSI 4
4	O	SYNO	16	—	NC	28	I	OSCI	40	I	TSI 5
5	O	$\overline{HSY}$	17	—	NC	29	—	NC	41	I	TSI 6
6	—	NC	18	O	TSO1	30	—	VDD	42	I	TSI 7
7	—	GND	19	—	NC	31	—	GND	43	I	TSI 8
8	O	RES	20	—	NC	32	—	NC	44	—	NC
9	O	FRPV	21	O	SPS	33	I	LOWI	45	—	NC
10	I	SYNI	22	O	CLS	34	O	TSO2	46	O	TSO3
11	I	N/$\overline{P}$	23	O	LOW	35	I	TSI1	47	I	BLKI
12	—	NC	24	—	NC	36	O	PDP	48	O	BLKO

INPUT

BLKI ; PLL PHASE COMPARISON
LOWI ; INITIAL RESET
MUTE ; SYNC ADJUST
N/$\overline{P}$; NTSC/PAL SELECT
OSCI ; CLOCK OSCILLATOR
SYNI ; COMPOSITE SYNC
TSI1-TSY8 ; TEST
VIN ; VERTICAL SYNC

OUTPUT

BLKO ; PLL PHASE COMPARISON
CLD ; SOURCE DRIVER CLOCK
CLS ; GATE DRIVER CLOCK
FRPC ; COMMON-ELECTRODE DRIVE SIGNAL POLARITY INVERSION
FRPV ; VIDEO SIGNAL POLARITY INVERSION
$\overline{HSY}$; HORIZONTAL SYNC
LOW ; GATE DRIVER CONTROL
OSCO ; CLOCK OSCILLATOR
PDP ; PLL PHASE COMPARISON CIRCUIT
RES ; SOURCE DRIVER CONTROL
SPD ; SOURCE DRIVER START
SPS ; GATE DRIVER START
SYNO ; COMPOSITE SYNC (VERTICA SYNC SEP.)
TSO1-TSO3 ; TEST
$\overline{VSY}$; VERTICAL SYNC


OSCI
28
HCK
HORIZONTAL COUNTER
MIXING GATE
HRES
VCK
VERTICAL COUNTER
MIXING GATE
VRES
H
N/P
11
VMU
VRI
VIN
3
GATE
LOWI
33
23
LOW
BLKI
47
36
PDP
H
MUTE
13
SYNI
10
4
SYNO
TSI1
35
34
TSO2
48
BLKO
5
HSY
27
OSCO
GATE
25
SPD
26
CLD
GATE
8
RES
22
CLS
21
SPS
9
FRPV
2
FRPC
14
VSY