

SPEC No.	E L 0 8 4 1 5 1 A
I S S U E: Jan. 16 1997	

To ; _____

REFERENCE

S P E C I F I C A T I O N S

Product Type 1/4-type Color CCD Area Sensor with 270k Pixels for NTSC

Model No. L Z 2 4 1 3 A

※This specifications contains 21 pages including the cover and appendix.

If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE: _____

BY: _____

PRESENTED

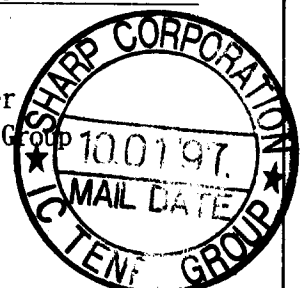
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 - Office electronics
 - Instrumentation and measuring equipment
 - Machine tools
 - Audiovisual equipment
 - Home appliances
 - Communication equipment other than for trunk lines
 - (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
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 - Mainframe computers
 - Traffic control systems
 - Gas leak detectors and automatic cutoff devices
 - Rescue and security equipment
 - Other safety devices and safety equipment, etc.
 - (3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
 - Aerospace equipment
 - Communications equipment for trunk lines
 - Control equipment for the nuclear power industry
 - Medical equipment related to life support, etc.
 - (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.
- Please direct all queries regarding the products covered herein to a sales representative of the company.

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1. GENERAL DESCRIPTION

LZ2413A is a 1/4-type(4.5mm) solid-state image sensor consists of PN photo-diodes and CCDs(charge-coupled devices). Having approximately 270,000 pixels(horizontal 542 x vertical 492), the sensor provides a high resolution stable color image.

Features

- 1) Number of image pixels : Horizontal 512 x vertical 492
Pixel pitch : Horizontal 7.2 μm x vertical 5.6 μm
Number of optical black pixels : Horizontal; front 2 and rear 28
- 2) Complementary color filter composed of Mg, G, Cy, and Ye
- 3) Low fixed pattern noise and lag
- 4) No burn-in and no image distortion
- 5) Blooming suppression structure
- 6) Built-in output amplifier
- 7) 14-pin half-pitch DIP
(Row space: 10.16mm)
- 8) Variable electronic shutter(1/60 to 1/10000 sec.)
- 9) N-type silicon substrate, N-MOS process
- 10) Not designed or rated as radiation hardened
- 11) Compatible with NTSC standard

Applications

- 1) Cameras(Camcorders, industrial monitor cameras, etc.)
- 2) Pattern recognition

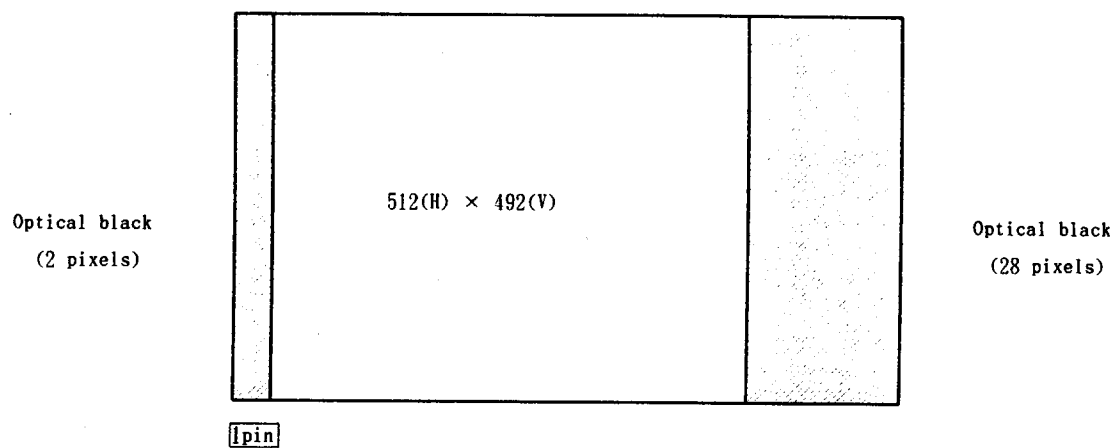
Others

Combined with the timing IC(LZ95D37/M) and SSG IC(LZ93N19) or combined with the timing generator IC(LZ95G55)* and subcarrier IC(LZ95B25), and V driver IC(LR36683N), sample/hold IC(IR3P66), this product operates under the performance satisfying these specifications.

* Set the SLCT(CCD select input) pin of LZ95G55 to Type B.

※ The circuit diagram and others included in this specification are intended for use to explain typical application examples. Therefore, we take no responsibility for any problem as may occur due to the use of the included circuit and for any problem with industrial proprietary rights or other rights.

2. ARRANGEMENT OF PIXELS AND COLOR FILTERS



(1, 492)

(512, 492)

Mg	G	Mg	G	Mg
Cy	Ye	Cy	Ye	Cy
G	Mg	G	Mg	G
Cy	Ye	Cy	Ye	Cy
Mg	G	Mg	G	Mg
Cy	Ye	Cy	Ye	Cy

G	Mg	G	Mg	G
Ye	Cy	Ye	Cy	Ye
Mg	G	Mg	G	Mg
Ye	Cy	Ye	Cy	Ye
G	Mg	G	Mg	G
Ye	Cy	Ye	Cy	Ye

ODD
field

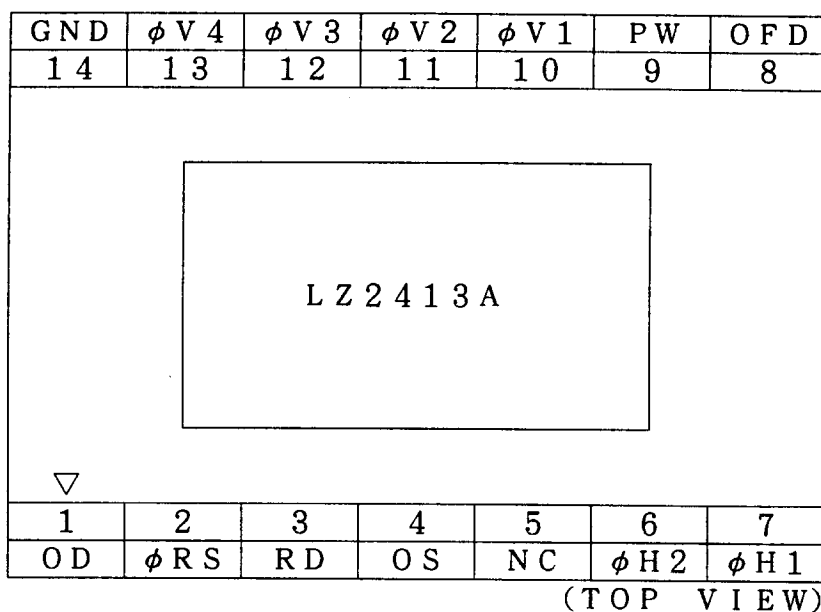
G	Mg	G	Mg	G
Cy	Ye	Cy	Ye	Cy
Mg	G	Mg	G	Mg
Cy	Ye	Cy	Ye	Cy
G	Mg	G	Mg	G
Cy	Ye	Cy	Ye	Cy

EVEN
field

Mg	G	Mg	G	Mg
Ye	Cy	Ye	Cy	Ye
G	Mg	G	Mg	G
Ye	Cy	Ye	Cy	Ye
Mg	G	Mg	G	Mg
Ye	Cy	Ye	Cy	Ye

(1, 1)

(512, 1)

3. PIN IDENTIFICATION

Symbol	Pin name
RD	Reset transistor drain
OD	Output transistor drain
OS	Video output
ϕRS	Reset transistor clock
$\phi V 1, \phi V 2, \phi V 3, \phi V 4$	Vertical shift register clock
$\phi H 1, \phi H 2$	Horizontal shift register clock
OFD	Overflow drain
PW	P well
GND	Ground
NC	Non connection

4. ABSOLUTE MAXIMUM RATINGS(T_a = 25°C)

Parameter	Symbol	Ratings	Unit
Output transistor drain voltage	V _{OD}	0 ~ +18	V
Reset transistor drain voltage	V _{RD}	0 ~ +18	V
Overflow drain voltage	V _{OFD}	0 ~ +45	V
Reset gate clock voltage	V ϕRS	-0.3 ~ +12	V
Vertical shift register clock voltage	V ϕV	-10.5 ~ +17.5	V
Horizontal shift register clock voltage	V ϕH	-0.3 ~ +12	V
Voltage difference between Pwell and vertical clock	V _{PW-VϕV}	-28 ~ 0	V
Voltage difference between vertical clock	V ϕV -V ϕV	0 ~ +15 (note)	V
Storage temperature	T _{stg}	-40 ~ +80	°C
Operating ambient temperature	T _{opr}	-20 ~ +70	°C

(note) When clock width is below 10 μ s, and clock duty factor is below 0.1%, voltage difference between vertical clock is guaranteed to 27V.

5. RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Minimum	Typical	Maximum	Unit
Operating ambient temperature		T _{opr}		25.0		°C
Output transistor drain voltage		V _{OD}	14.5	15.0	16.0	V
Reset transistor drain voltage		V _{RD}		V _{OD}		V
Overflow drain voltage	When DC is applied (note1)	V _{OFD}	5.0		15.0	V
	When pulse is applied p-p level (note2)	V ϕ _{OFD}	21.5			V
Ground		G _{ND}		0.0		V
P well voltage		V _{PW}	-9.0		V ϕ _{VL}	V
Vertical shift register clock LOW level		V ϕ _{V1L} , V ϕ _{V3L} V ϕ _{V2L} , V ϕ _{V4L}	-8.5	-8.0	-7.5	V
Vertical shift register clock INTERMEDIATE level		V ϕ _{V1I} , V ϕ _{V3I} V ϕ _{V2I} , V ϕ _{V4I}		0.0		V
Vertical shift register clock HIGH level		V ϕ _{V1H} , V ϕ _{V3H}	14.5	15.0	15.5	V
Horizontal shift register clock LOW level		V ϕ _{H1L} , V ϕ _{H2L}	-0.05	0.0	0.05	V
Horizontal shift register clock HIGH level		V ϕ _{H1H} , V ϕ _{H2H}	3.3	3.6	5.5	V
Reset gate clock LOW level		V ϕ _{RSL}	0.0		V _{RD} -12.3	V
Reset gate clock HIGH level		V ϕ _{RSH}	V _{RD} -7.8		10.0	V
Vertical shift register clock frequency		f ϕ _{V1} , f ϕ _{V2} f ϕ _{V3} , f ϕ _{V4}		15.73		k Hz
Horizontal shift register clock frequency		f ϕ _{H1} , f ϕ _{H2}		9.53		MHz
Reset gate clock frequency		f ϕ _{RS}		9.53		MHz

* Connect NC to GND directly or through a capacitor larger than 0.047 μ F.

(note1) When DC voltage is applied, shutter speed is 1/60 second.

(note2) When pulse is applied, shutter speed is less than 1/60 second.

(note3) V_{PW} is set below V ϕ _{VL} that is low level of vertical shift register clock, or use the same power supply that is connected to VL of V driver IC.

◆ To apply power, first connect GND and then turn on OFD. After turning on OFD, turn on PW first and then turn on other powers and pulses.

Do not connect the device to or disconnect it from the plug socket while power is being applied.

6. CHARACTERISTICS (Drive method : Field accumulation)

Ambient temperature : +25°C, but +60°C for parameter No. 4 and 5.

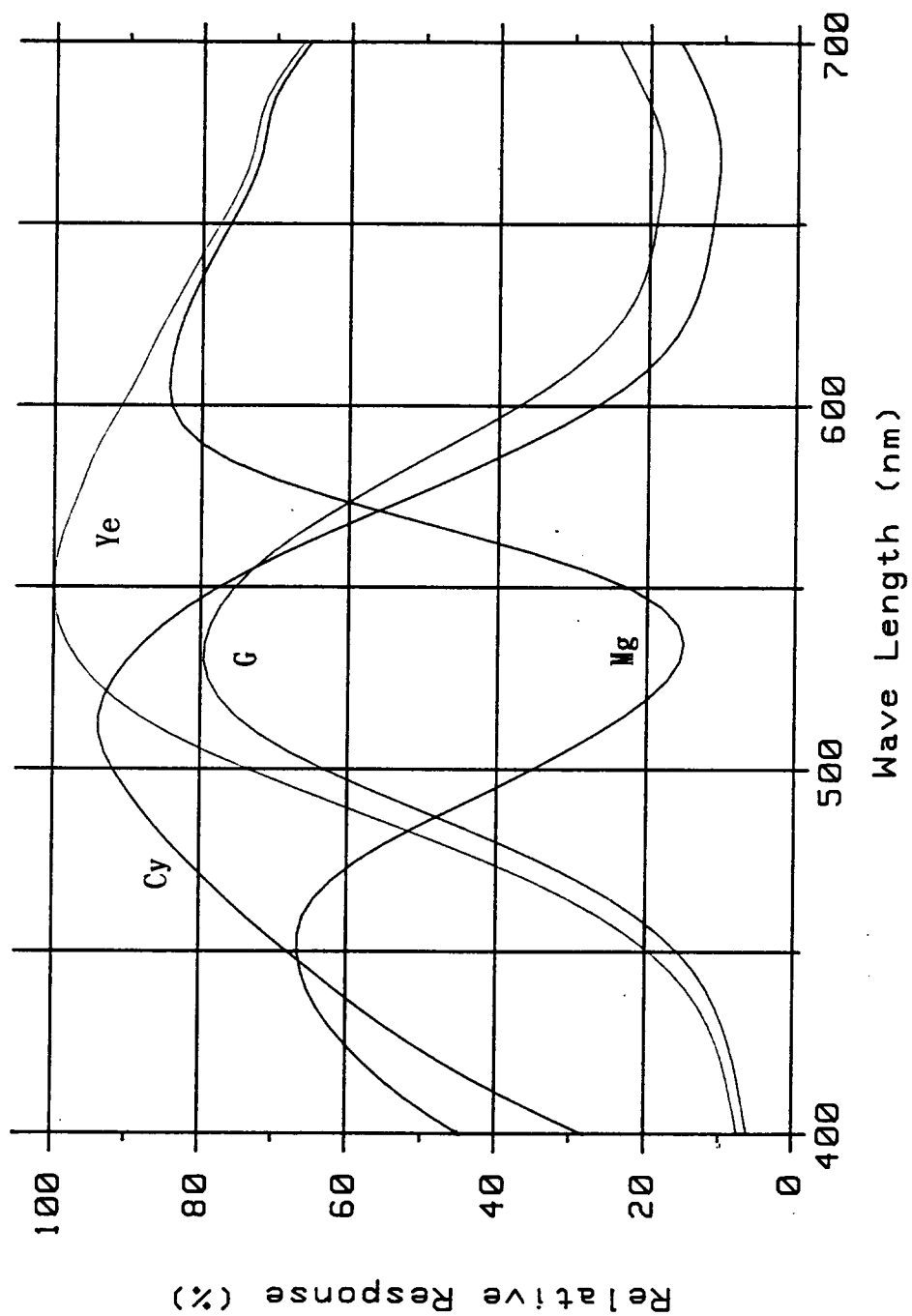
Operating conditions : the typical values specified in recommended conditions.

Color Temperature of light source : 3200K / IR cut-off filter(CM-500,1mm) is used.

No.	Parameter	Symbol	Note	Minimum	Typical	Maximum	Unit
1	Standard output voltage	Vo	(a)		150		mV
2	Photo response non-uniformity	PRNU	(b)			15	%
3	Saturation output voltage	Vsat	(c)	700			mV
4	Dark output voltage	Vdark	(d)		0.5	3.0	mV
5	Dark signal non-uniformity	DSNU	(e)		0.5	2.0	mV
6	Sensitivity	R	(f)	340	450		mV
7	Smear ratio	SMR	(g)		-90	-80	dB
8	Image lag	AI	(h)			1.0	%
9	Blooming suppression ratio	ABL	(i)	1000			
10	Current dissipation	IOD			4.0	8.0	mA
11	Output impedance	Ro			350		Ω
12	Vector breakup		(j)			7.0	°, %
13	Line crawling		(k)			3.0	%
14	Luminance flicker		(l)			2.0	%

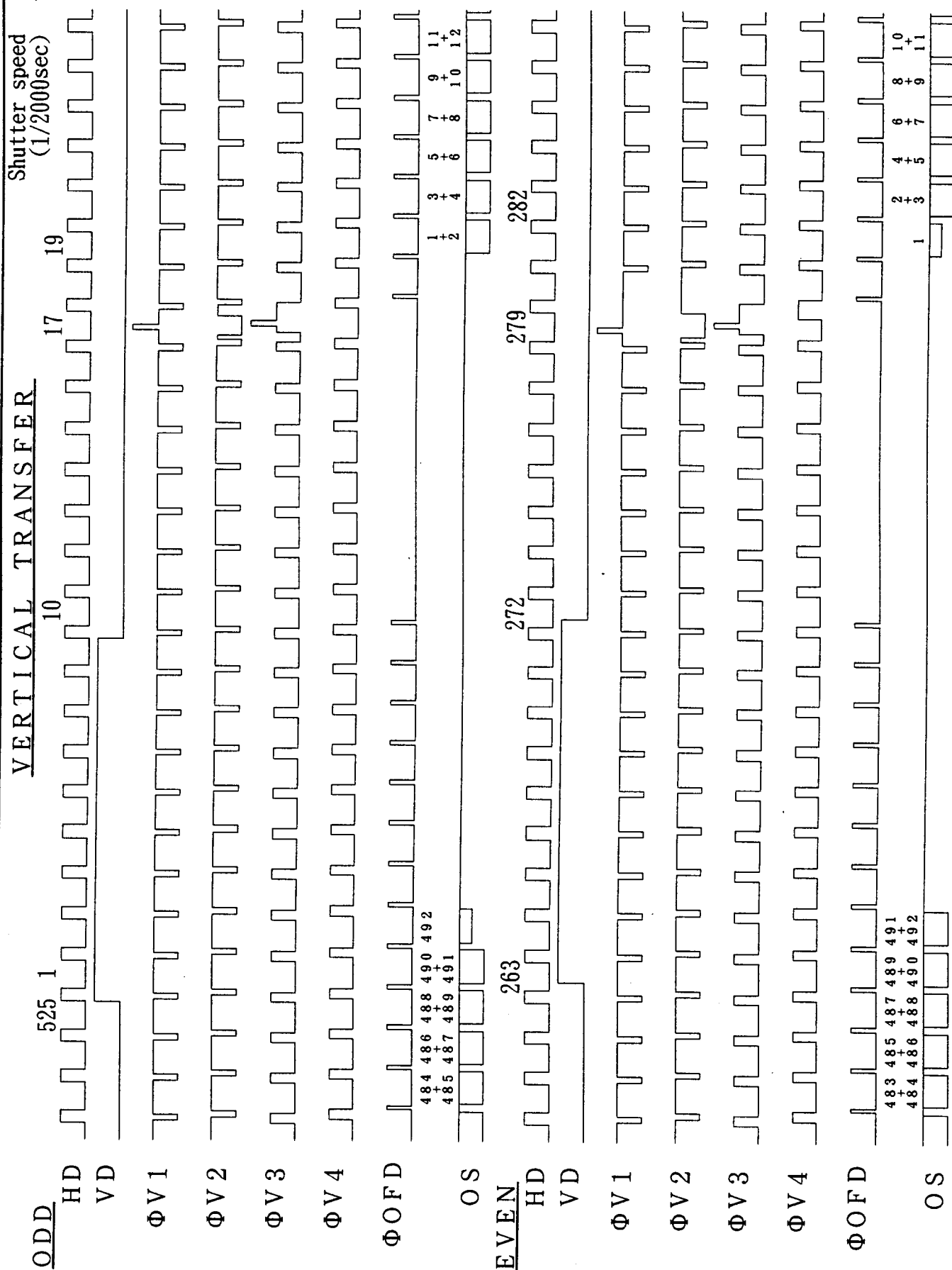
【Note】

- VOFD is adjusted to the minimum voltage with that ABL satisfy the specification or within ±3% of the value displayed on the device.
- (a) The average output voltage under the uniform illumination. The standard exposure condition is defined when Vo is 150 mV.
- (b) The image area is divided into 10 × 10 segments under the standard exposure condition. The voltage of a segment is the average output voltage of all pixels within the segment. PRNU is defined by $(V_{\max} - V_{\min}) / V_o$, where V_{\max} and V_{\min} are the maximum and minimum values of each segment's voltage respectively.
- (c) The image area is divided into 10 × 10 segments. The segment's voltage is the average output voltages of all pixels within the segment. Vsat is the minimum segment's voltage under 10 times exposure of the standard exposure condition.
- (d) The average output voltage under the non-exposure condition.
- (e) The image area is divided into 10 × 10 segments under the non-exposure condition. DSNU is defined by $(V_{d\max} - V_{d\min})$, where $V_{d\max}$ and $V_{d\min}$ are the maximum and minimum values of each segment's voltage respectively.
- (f) The average output voltage when a 1000 lux light source with a 90% reflector is imaged by a lens of F4, f50 mm.
- (g) The sensor is exposed only in the central area of V/10 square with a lens at F4, where V is the vertical image size. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum of the output voltage in the V/10 square.
- (h) The sensor is exposed at the exposure level corresponding to the standard condition. AI is defined by the ratio between the output voltage measured at the 1st field during the non-exposure period and the standard output voltage.
- (i) The sensor is exposed only in the central area of V/10 square, where V is the vertical image size. ABL is the ratio between the exposure at the standard condition and the exposure at a point where a blooming is observed.
- (j) Observe with a vector scope when the color bar chart is imaged under the standard exposure condition.
- (k) The difference of the average output voltage between the (Mg+Cy), (G+Ye) line and the (Mg+Cy), (G+Ye) line under the standard exposure condition.
- (l) The difference of the average output voltage between odd field and even field under the standard exposure condition.

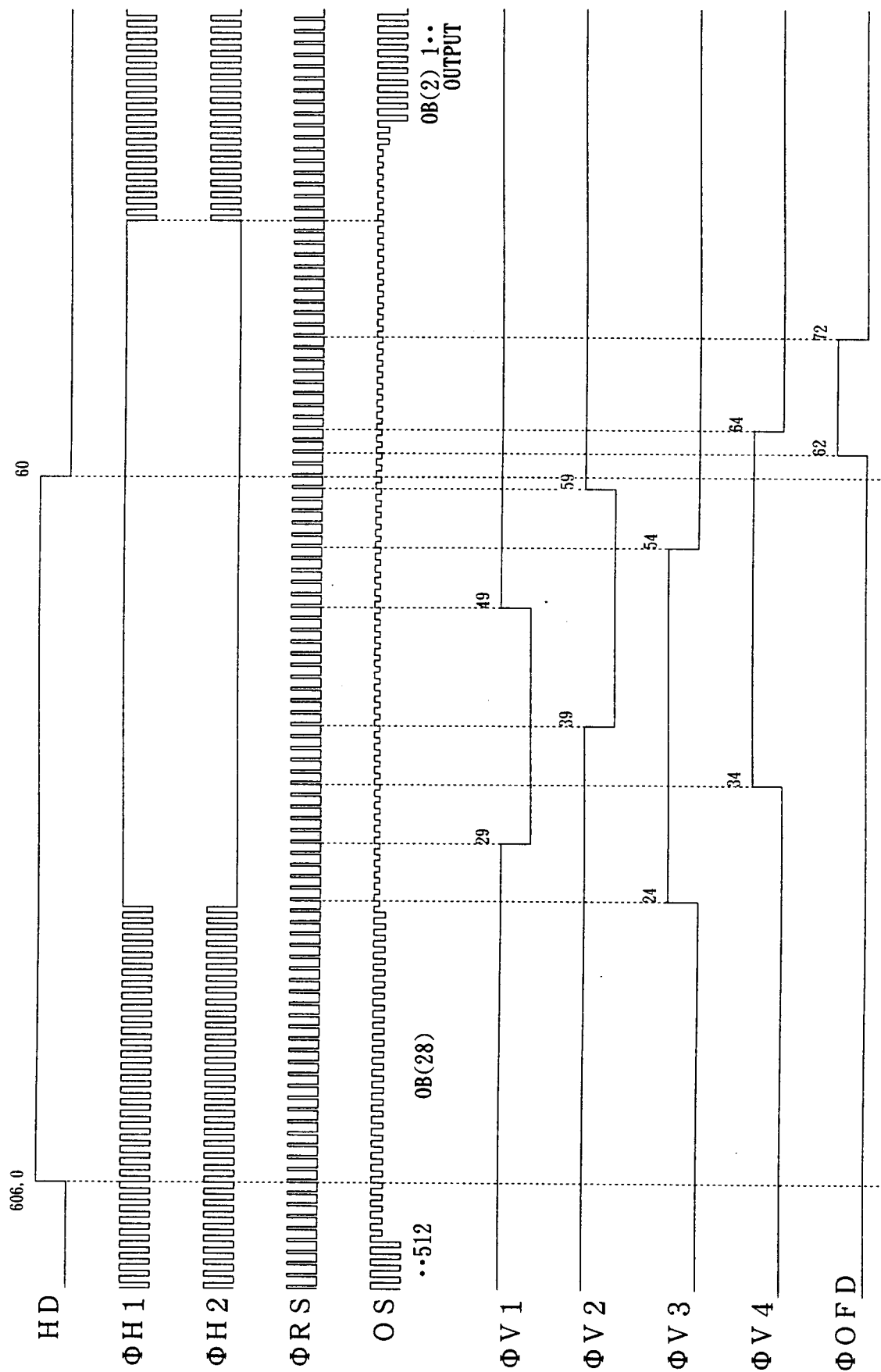


Spectral Response Example

7. TIMING DIAGRAM EXAMPLE

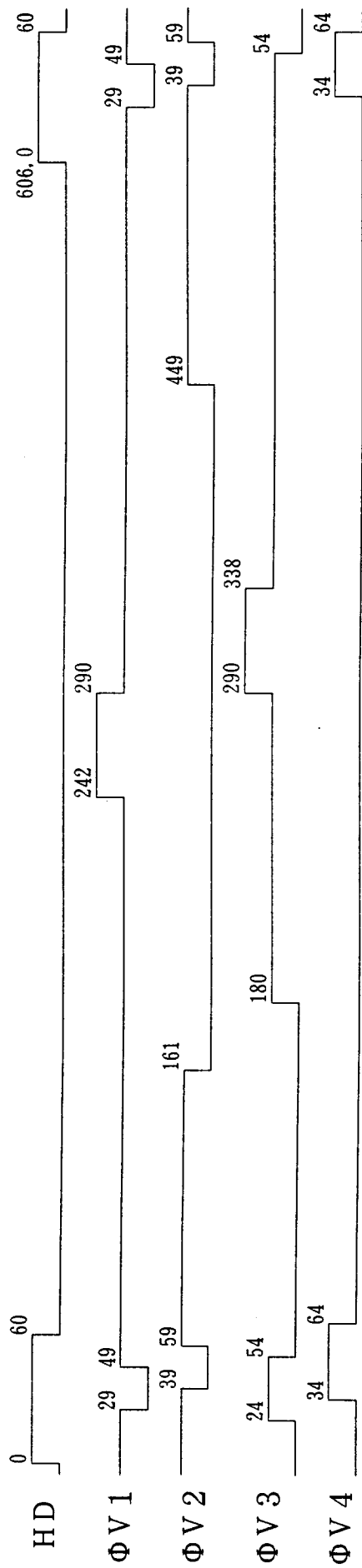


HORIZONTAL TRANSFER

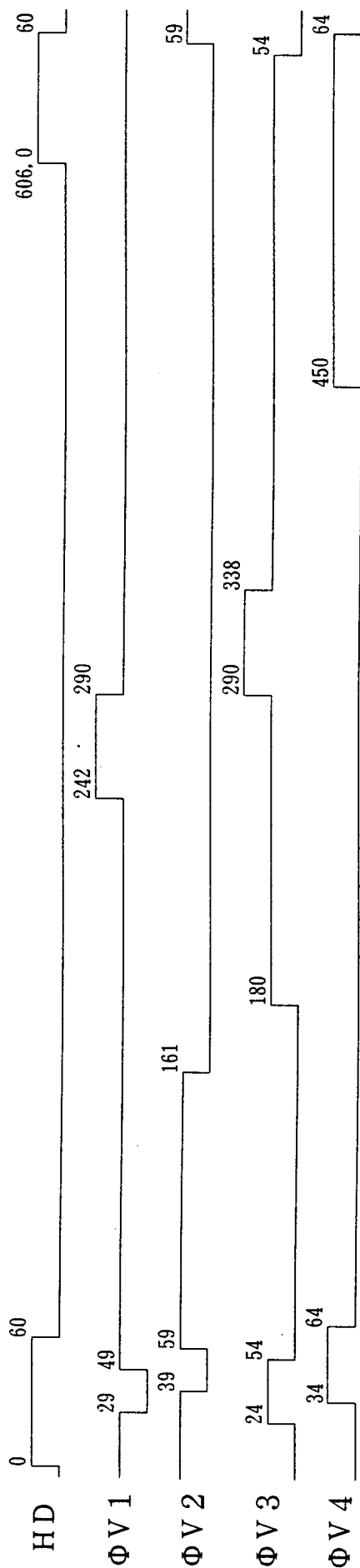


READOUT TIMING

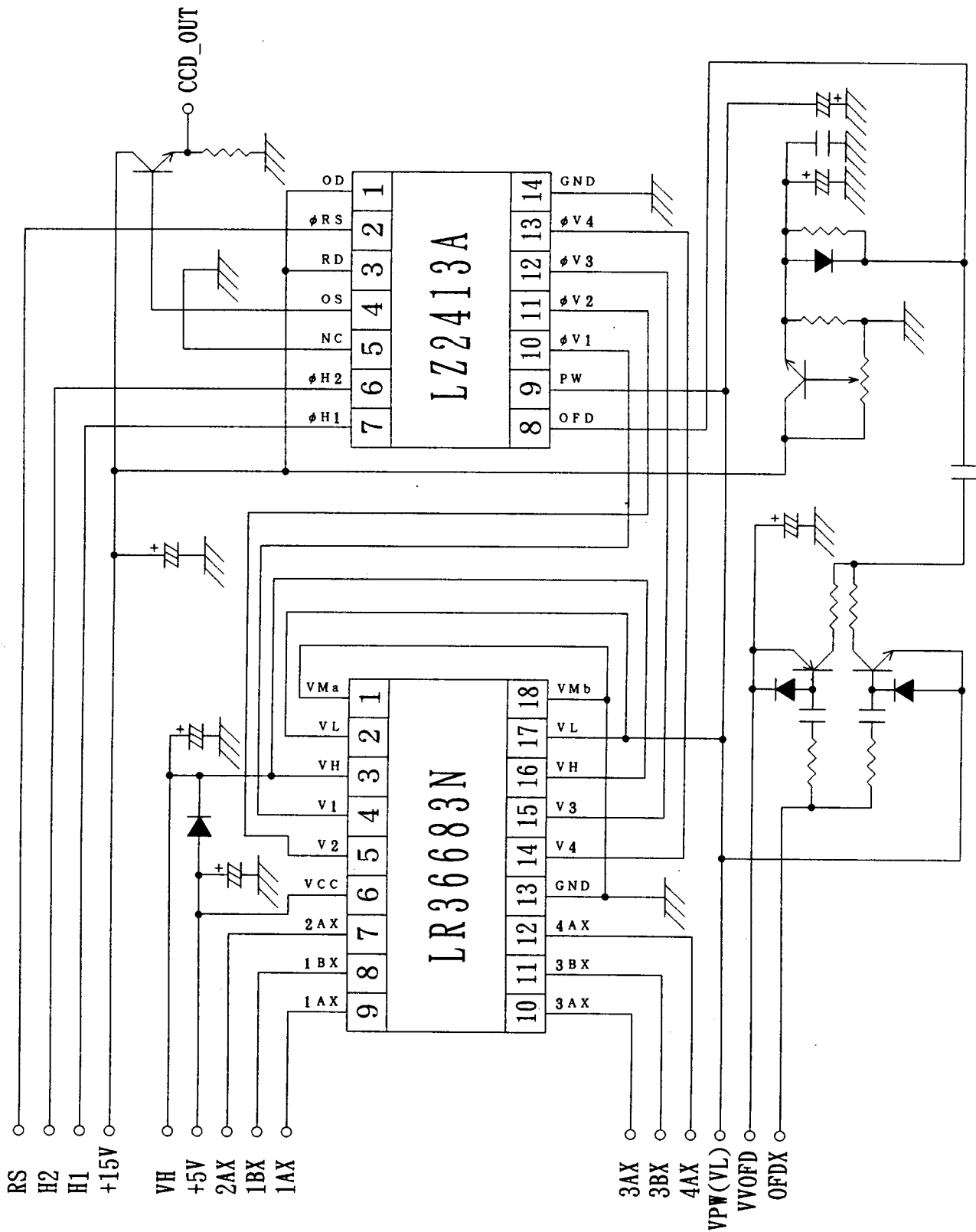
ODD



EVEN



8. STANDARD OPERATING CIRCUIT EXAMPLE



9. SPECIFICATION FOR BLEMISH

1) Definition of blemish

	Level of blemish (mV)	Permitted number of blemish		Comment
White blemish (Exposed)	$23 \leq B$	0		<ul style="list-style-type: none">• See fig. 9-1(a)、fig. 9-2.• $V_{out} = V_{std}$• $M + N = 10$ Up to 4 blemishes are allowed in AREA I
	$13 \leq B < 23$	M		
	$B < 13$	no count		
Black blemish (Exposed)	$23 \leq B$	0		
	$13 \leq B < 23$	N		
	$B < 13$	no count		
White blemish (Non_exposed)		AREA I	AREA II	<ul style="list-style-type: none">• See fig. 9-1(b)、fig. 9-2.• Sum of the blemishes in AREA I and II are allowed up to 6.
	$8 < B$	0		
	$6 < B \leq 8$	2	4	
	$4 < B \leq 6$	4	5	
	$B \leq 4$	no count		
White blemish (Shutter mode)	$4.5 \leq B$	0		<ul style="list-style-type: none">• See fig. 9-1(a)、fig. 9-2.• $V_{out} = V_{std}/10$
	$B < 4.5$	no count		
Black blemish (Shutter mode)	$4.5 \leq B$	0		<ul style="list-style-type: none">• The electronic shutter speed is set at 1/10000 s
	$B < 4.5$	no count		

《note》

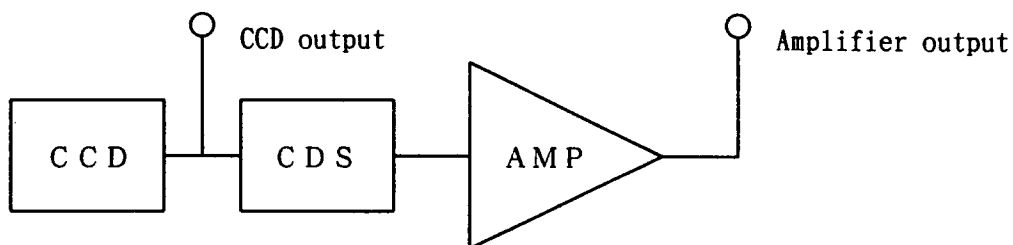
- B : Blemish level defined in fig. 9-1.
- V_{out} : Average output voltage
- V_{std} : 150 mV. The standard output voltage defined in the specification of the characteristics.

2) Definition of stain.

The measuring area is divided into segments which include 20×20 pixels, respectively. The difference between the average output voltage of neighboring segments is permitted below 1.5 mV, under the condition that the average output voltage of all imaging pixels is 75 mV ($= V_{std}/2$).

【MEASURING CONDITION】

- T a : 60 °C
- Measuring block diagram



The output voltage is measured at the CCD output.
The gain of the amplifier is adjusted to the unity between the CCD output and the amplifier output.

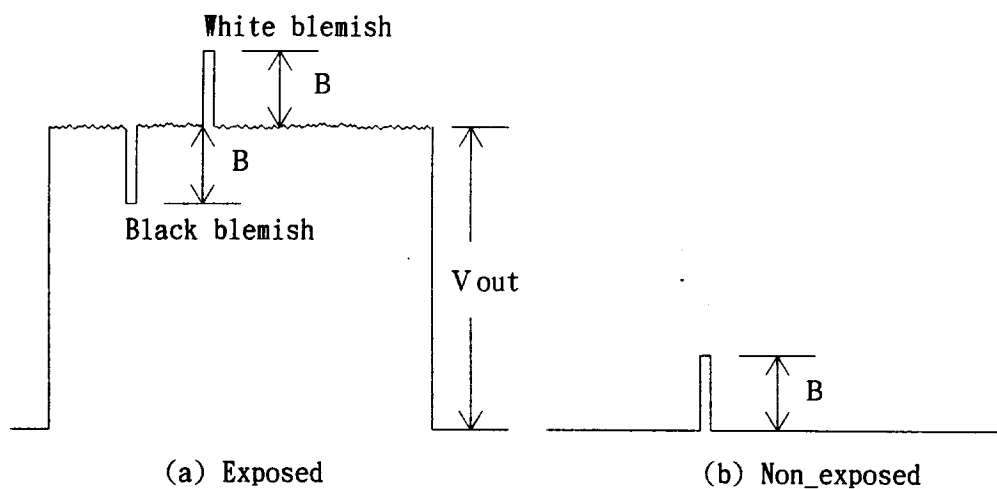


fig. 9-1 Definition of blemish level

(The wave form is the luminance signal measured at the Amplifier output.)

【MEASURING AREA】

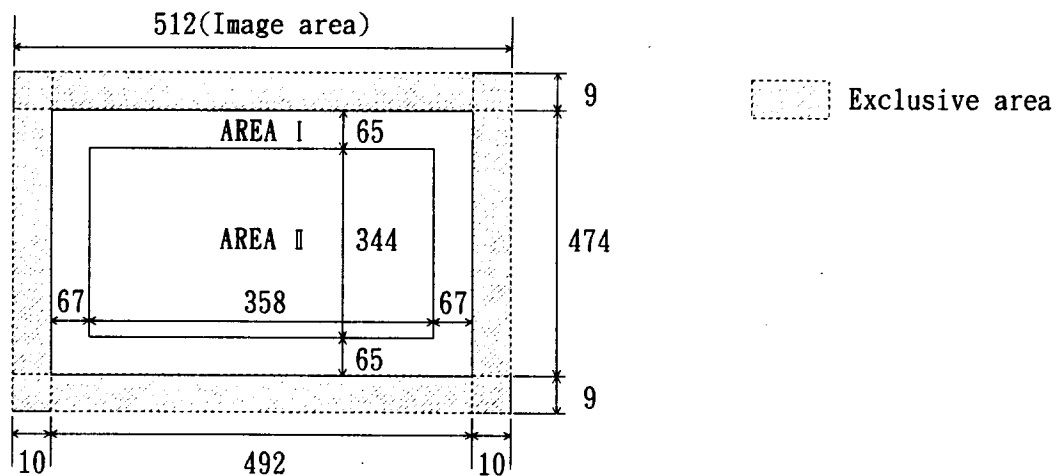


fig. 9-2 Definition of the measuring area

10. CAUTIONS FOR USE

1. Package breakage

In order to prevent the package from being broken, observe the following instructions:

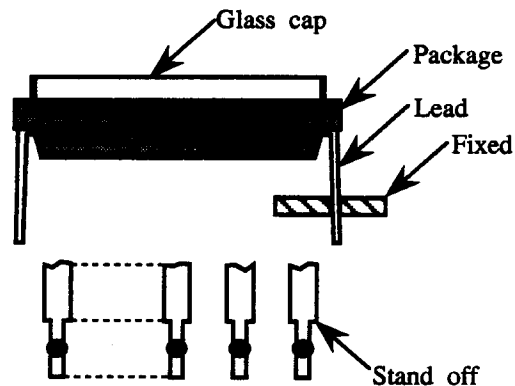
- 1) The CCD is a precise optical component and the package material is plastic. Therefore.

- Take care not to drop the device when mounting, handling, or transporting.
- Avoid giving a shock to the package. Especially when leads are fixed to the shock and the circuit board, small shock could break the package more easily than when the package isn't fixed.

- 2) When applying force for mounting the device or any other purposes, fix the leads between a joint and a stand_off, so that no stress will be given to the jointed part of the lead.

In addition, when applying force, do it at a point below the stand_off part.

- The leads of the package are fixed with package body (plastic), so stress added to a lead could cause a crack in the package body (plastic) in the jointed part of the lead.
- 3) When mounting the package on the housing, be sure that package is not bent.
- If a bent package is forced into place between a hard plate or the like, the package may be broken.



- 4) If any damage or breakage occur on the surface of the glass cap, its characteristics could deteriorate.

Therefore,

- Do not hit the glass cap.
- Do not give a shock large enough to cause distortion.
- Do not scrub or scratch the glass surface.
- Even a soft cloth or applicator, if dry, could cause dust to scratch the glass.

2. Electrostatic damage

As compared with general MOS-LSI, CCD has lower ESD.

Therefore, please take the following anti-static measures when handling the CCD:

- 1) Always discharge static electricity by grounding the human body and the instrument to be used. To ground the human body, provide resistance of about 1 Meg ohm between the human body and the ground to be on the safe side.
- 2) When directly handling the device with fingers, hold the part without leads and do not touch any lead.
- 3) To avoid generating static electricity,
 - a. do not scrub the glass surface with cloth or plastic
 - b. do not attach any tape or labels
 - c. do not clean the glass surface with dust-cleaning tape
- 4) When storing or transporting the device, put it in a container of conductive material.

3. Dust and contamination

Dust or contamination on the glass surface could deteriorate the output characteristic or cause a scar. In order to minimize dust or contamination on the glass surface, take the following precautions:

- 1) Handle CCD in a clean environment such as a cleaned booth.
(The cleanliness level should be, if possible, class 1,000 at least.)
 - 2) Do not touch the glass surface with fingers. If dust or contamination gets on the glass surface, the following cleaning method is recommended:
 - Dust from static electricity should be blown off with an ionized air blower.
For anti-electrostatic measures, however, ground all the leads on the device before blowing off the dust.
 - The contamination on the glass surface should be wiped off with a clean applicator soaked in Isopropyl alcohol. Wipe slowly and gently in one direction only.
- Frequently replace the applicator and do not use the same applicator to clean more than one device.

※ Note: In more cases, dust and contamination are unavoidable, even before the device is first used. It is, therefore, recommend that the above procedures should be taken to wipe out dust and contamination before using the device.

4. Other

- 1) Soldering should be manually performed within 5 seconds at 350°C maximum at soldering iron.
- 2) Avoid using or storing the CCD at high temperature or high humidity as it is a precise optical component. Do not give a mechanical shock to the CCD.
- 3) Do not expose the device to strong light. For the color device, long exposure to strong light will fade the color of the color filters.
- 4) The exit pupil position of lens should be more than 25mm from the top surface of CCD.

L Z 2 4 1 3 A

1.1 PACKAGE OUTLINE AND PACKING SPECIFICATION

1. Package Outline Specification

Refer to drawing No. GDP 0 1 4 B - 0 5 E 1.

(The seal resin stick out from the package shall be passed. And, the seal resins are two kinds of colors, white and transparency.)

2. Markings

Marking contents

(1) Product name : L Z 2 4 1 3 A

(2) Company name : S H A R P

(3) Country of origin : J A P A N

(4) Date code : Y Y W W X X X

Denotes the production ref. code.(1 ~ 2 figures)

Denotes the production day of the week.

1	2	3	4	5	6	7
SUN.	MON.	TUE.	WED.	THU.	FRI.	SAT.

Denotes the production week.

(01,02,03,52,53)

Denotes the production year.

(Lower two digits of the year.)

(5) Over flow drain : E E

Denotes the corresponding code of over flow drain voltage.

Positions of markings are shown in the package outline drawing (No.GDP014B-05E1).

But, markings shown in that drawing are not provided any measurements of their characters and their positions.

3. Packing Specification

3-1. Packing materials

Material Name	Material Spec.	Purpose
Device case	Paper (180devices/case)	Device packing (2trays/case)
Device tray	Conductive plastic (90devices/tray)	Device fixing
Cover tray	Conductive plastic (2trays/case)	Device covering
Buffer	Cardboard (1sheet/case)	Shock absorber of device tray
Air cushion bag	Plastic film	Device tray fixing
Tape	Paper	Sealing air cushion bag

3-2. External appearance of packing

Refer to drawing No. K S E C - 1 8 0 T 3 - O.

4. Precaution

- Before unpacking, confirm the imports of the chapter "Handling Precaution" in this device specifications.
- Unpacking should be done on the stand treated with anti-ESD. At that time, the same anti-ESD treatment should be done to operator's body, too.
- Printer's ink of over flow drain voltage isn't solvent-proof, so it is possible to be defaced by using a solvent.

ISSUE DATE	9 6 . 0 2 . 2 8	M. Kanishi K. Takada J. Seko	(NOTE)
ISSUE NUMBER	5 2 2 8 2 A D C		
S/C NUMBER	L Z 2 4 1 3 A		

L Z 2 4 1 3 A

5. Corresponding code of over flow drain voltage

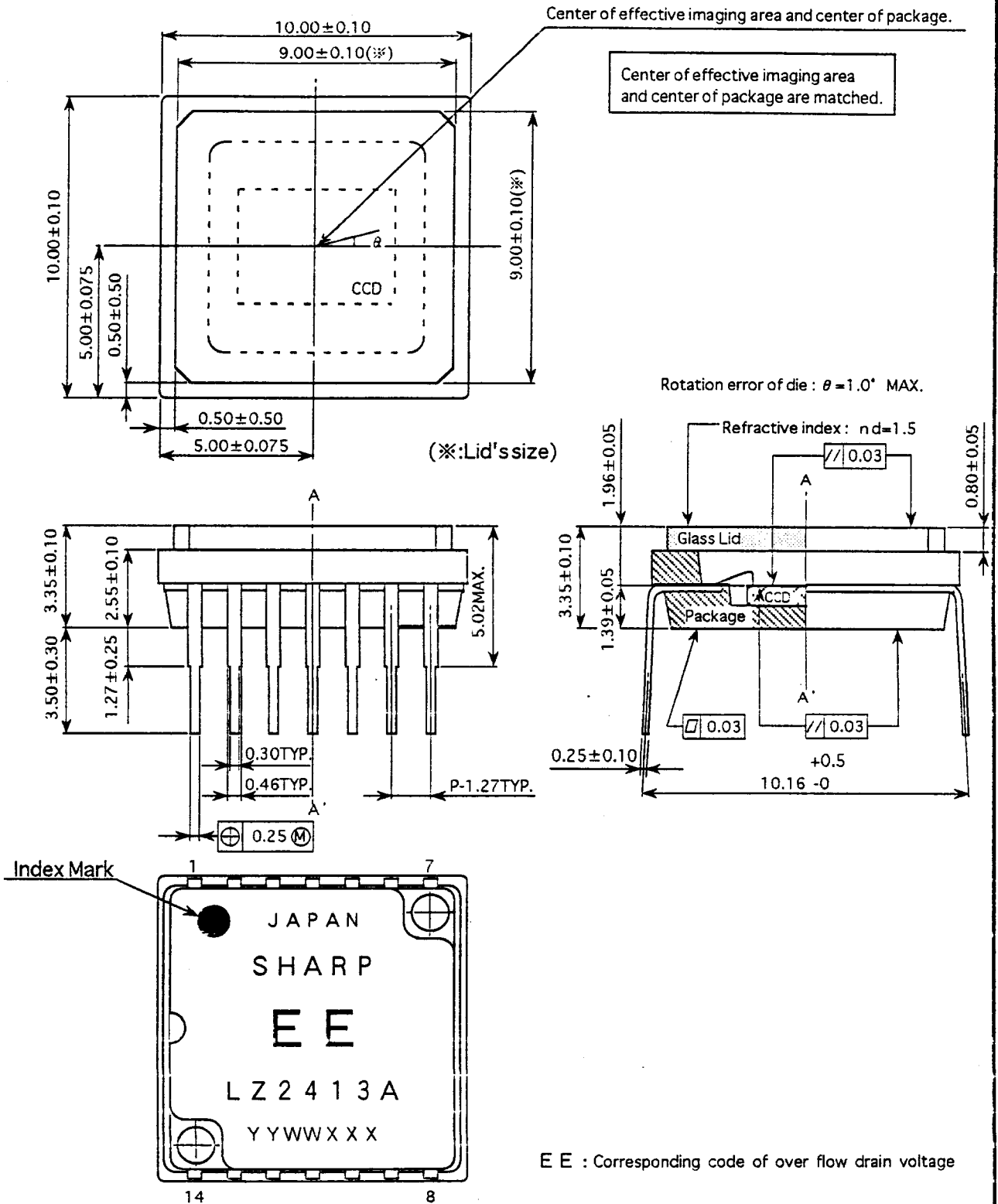
Contents of the corresponding code

Numerical value of over flow drain voltage (V) (Down to one decimal place)		Corresponding code of over flow drain voltage (English alphabet and numeral of two figures)	
Integral value	3.	One figure	3
	4.		4
	5.		5
	6.		6
	7.		7
	8.		8
	9.		9
	10.		A
	11.		B
	12.		C
	13.		D
	14.		E
	15.		F
	16.		G
	17.		H
	18.		J
	19.		K
	20.		L
Decimal value	. 0	Two figures	0
	. 1		1
	. 2		2
	. 3		3
	. 4		4
	. 5		5
	. 6		6
	. 7		7
	. 8		8
	. 9		9

Example of the corresponding code

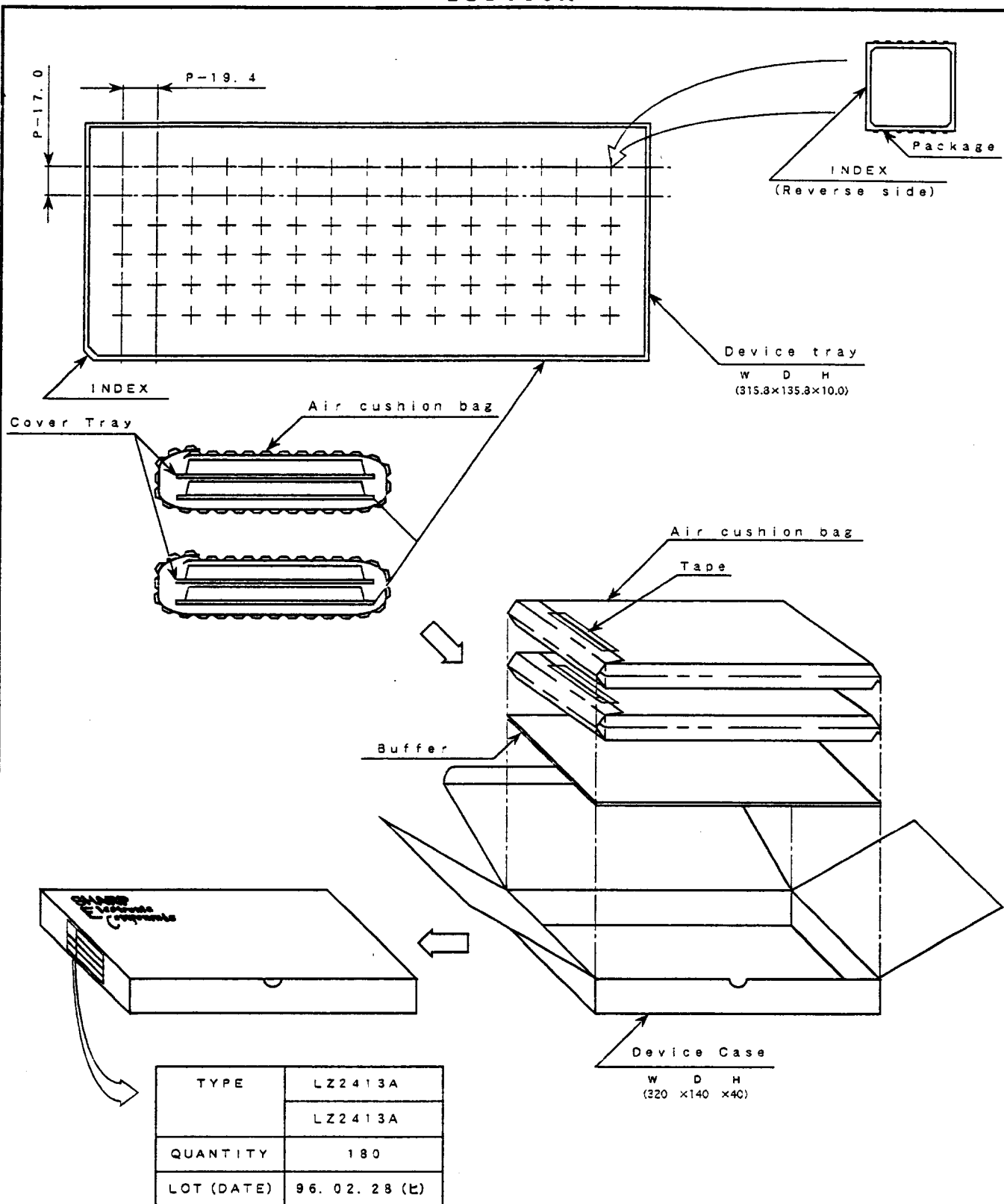
Numerical value of voltage : 9. 5 (V) → Corresponding code of voltage : 9 5
 14. 3 (V) → E 3

LZ2413A



材質 MATERIAL	仕上 FINISH	名 称 NAME	DMPP14BS-01 Package Outline Specification
ASSEMBLY & TEST ENGINEERING DEPARTMENT		コード CODE	
INTEGRATED CIRCUITS (IC) GROUP		図 番 DRAWING No.	G.D.P.014.B-0.5.E.1
SHARP CORPORATION			

LZ2413A



(UNIT : mm)

材質 MATERIAL	仕 上 FINISH	名 称 NAME	External Appearance of Packing									
			コード CODE									
ASSEMBLY & TEST ENGINEERING DEPARTMENT												
INTEGRATED CIRCUITS (IC) GROUP		図 番 DRAWING No.	K, S, E, C - 1, 8, 0, T, 3 - 10									
SHARP CORPORATION												