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ISSUE:	Feb. 26 1997

To: _____

PRELIMINARY SPECIFICATIONS

Product Type 1/3 type solid state B/W imaging device for CCIR system

Model No. LZ2326AJ

※This specifications contains 19 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE: _____

BY: _____

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 - (1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
 - Office electronics
 - Instrumentation and measuring equipment
 - Machine tools
 - Audiovisual equipment
 - Home appliances
 - Communication equipment other than for trunk lines
 - (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
 - Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
 - Mainframe computers
 - Traffic control systems
 - Gas leak detectors and automatic cutoff devices
 - Rescue and security equipment
 - Other safety devices and safety equipment, etc.
 - (3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
 - Aerospace equipment
 - Communications equipment for trunk lines
 - Control equipment for the nuclear power industry
 - Medical equipment related to life support, etc.
 - (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.
- Please direct all queries regarding the products covered herein to a sales representative of the company.

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1. GENERAL

LZ2326AJ is a 1/3 type (6.0mm) solid state imaging device consisting of PN photo-diodes and CCDs(charge-coupled devices) driven by only positive voltages.

Having about 320,000 pixels(horizontal 542 x vertical 582), it allows a stable B/W image to be obtained at high resolution.

1 Features

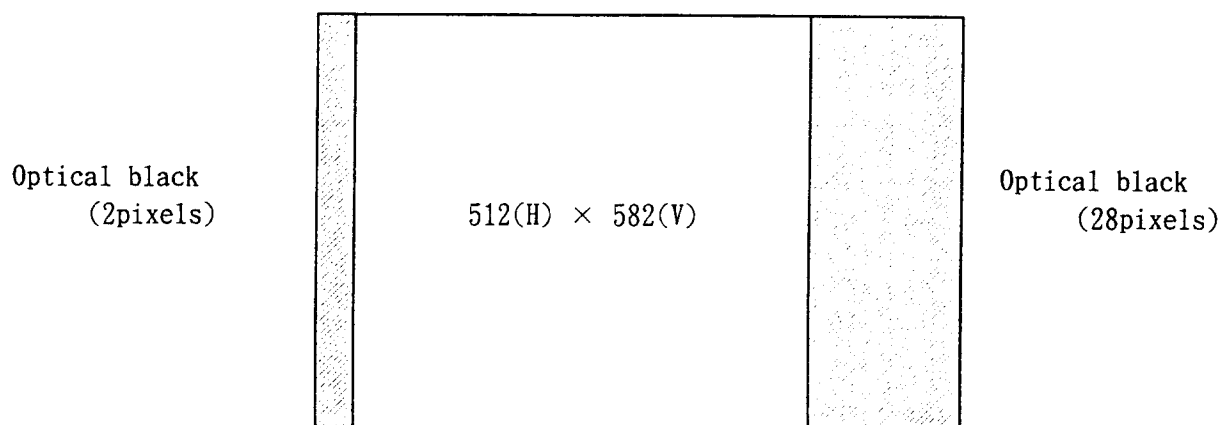
- 1) Number of video picture elements : Horizontal 512 x vertical 582
Pixel pitch : Horizontal 9.6 μm x vertical 6.3 μm
Number of optically black pixel : Horizontal; front 2 and rear 28
- 2) Reduced fixed pattern noise and lag
- 3) No sticking and no image distortion
- 4) Blooming suppression structure
- 5) Built-in output amplifier, pulse mix circuit
- 6) 16-pin shrink DIP
(Row space: 12.70 mm)
- 7) Variable electronic shutter
- 8) N-type silicon substrate
- 9) Not designed or rated as radiation hardened
- 10) Compatible with CCIR standard
- 11) Built-in overflow drain voltage output circuit, and built-in reset gate bias output circuit

2 Applications

- 1) Camcorders
- 2) Monitor cameras(TV doorphone, Video phone, Rear view cameras, etc.)
- 3) Pattern recognition

※ The circuit diagram and others included in this specification are intended for use to explain typical application examples. Therefore, we take no responsibility for any problem as may occur due to the use of the included circuit and for any problem with industrial proprietary rights or other rights.

2. COMPOSITION OF PIXELS



3. PIN ASSIGNMENT AND PIN IDENTIFICATION

T 1	OFD	ϕ TG	ϕ V2	ϕ V1	ϕ V4	ϕ V3	ϕ H1
16	15	14	13	12	11	10	9
L Z 2 3 2 6 A J							
▽							
1	2	3	4	5	6	7	8
ϕ RS	R D	GND	O S	O D	ϕ H2B	ϕ H2	ϕ H1B

(TOP VIEW)

Symbol	Pin name
R D	Reset transistor drain
O D	Output transistor drain
O S	Video output
ϕ R S	Reset transistor gate clock (*1)
ϕ V 1, ϕ V 2, ϕ V 3, ϕ V 4	Vertical shift register gate clock (*3)
ϕ H 1, ϕ H 2, ϕ H1B, ϕ H2B	Horizontal shift register gate clock
ϕ T G	Transfer gate clock (*4)
O F D	Overflow drain (*2)
T 1	Test terminals
G N D	Ground

(*1~4):REFER TO "8. SATNDARD OPERATING CIRCUIT EXAMPLE" (P11)

4. ABSOLUTE MAXIMUM RATING

(T a = 25 °C)

Item	Symbol	Rating	Unit
Output transistor drain voltage	V O D	0 to +15	V
Reset transistor drain voltage	V R D	0 to +15	V
Test terminal, T1	V T 1	0 to +15	V
Reset gate clock voltage	V ϕ R S	internal output(note1)	
Vertical shift register clock voltage	V ϕ V	0 to +7.5	V
Horizontal shift register clock voltage	V ϕ H	0 to +7.5	V
Transfer gate clock voltage	V ϕ T G	-0.3 to +15	V
Overflow drain voltage	V O F D	internal output(note2)	
Storage temperature	T stg	-40 to +85	°C
Operating ambient temperature	T opr	-20 to +70	°C

(note1) Do not connect to DC voltage directly. When ϕ RS is connected to GND, connect VOD to GND. Reset gate clock is applied below 8Vp-p.

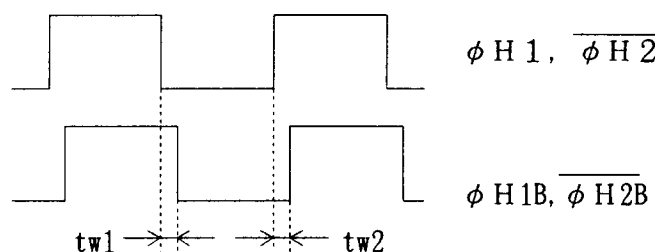
(note2) Do not connect to DC voltage directly. When OFD is connected to GND, connect VOD to GND. Overflow drain clock is applied below 13Vp-p.

5. RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Minimum	Typical	Maximum	Unit
Operating ambient temperature	T _{opr}		25.0		°C
Output transistor drain voltage	V _{OD}	12.0	12.5	13.0	V
Reset transistor drain voltage	V _{RD}		V _{OD}		V
Overflow drain clock p-p level (note1)	V _{φOFD}	12.0	12.5	13.0	V
Test terminals, T1	V _{T1}		V _{OD}		V
Ground voltage	G _{ND}		0.0		V
Transfer gate clock	LOW level	-0.05	0.0	0.05	V
	HIGH level	12.0	12.5	13.0	V
Vertical shift register clock p-p level (note2)	V _{φV1~4}	4.7	5.0	5.5	V
Horizontal shift register clock	LOW level	-0.05	0.0	0.05	V
	HIGH level	4.7	5.0	5.5	V
Reset gate clock p-p level (note3)	V _{φRS}	4.5	5.0	5.5	V
Vertical shift register clock freq.	f _{φV1~4}		15.63		kH z
Horizontal shift register clock freq.	f _{φH1~2} , f _{φH1~2B}		9.66		MH z
Reset gate clock freq.	f _{φRS}		9.66		MH z
Horizontal shift register clock phase	tw1, tw2 (note4)	1.0	5.0	10.0	n s

(note1、2、3) Use the circuit parameter indicated in "8. STANDARD OPERATING CIRCUIT EXAMPLE" (P11), and do not connect to DC voltage directly.

(note4)



※ To apply power, first connect GND and then turn on V_{OD} and then turn on other powers and pulses.

Do not connect the device to or disconnect it from the plug socket while power is being applied.

6. CHARACTERISTICS

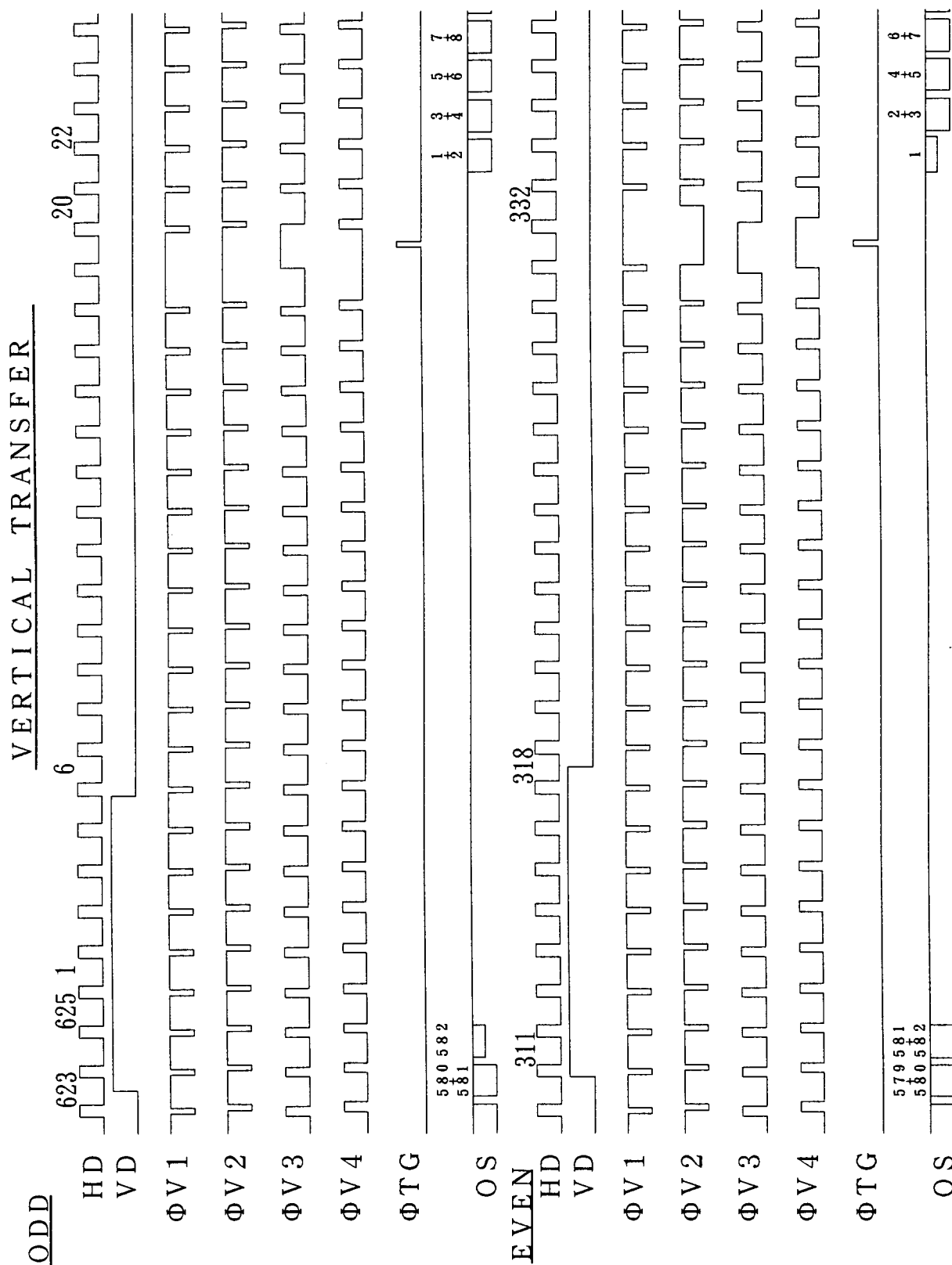
No.	Item	Symbol	Note	Min.	Typ.	Max.	Unit
1	Photo response non-uniformity	PRNU	(a)			15	%
2	Saturation signal	Vsat	(b)	550			m V
3	Dark output voltage	Vdark	(c)		0.5		m V
4	Dark signal non-uniformity	DSNU	(d)		0.5		m V
5	Sensitivity	R	(e)				m V
6	Smear ratio	SMR	(f)		-110.0	-90.0	d B
7	Image lag	AI	(g)			1.0	%
8	Blooming suppression ratio	ABL	(h)	1000			
9	Current dissipation	I _{OD}			4.0	8.0	m A
10	Output impedance	R _O			400		Ω

【 Conditions 】

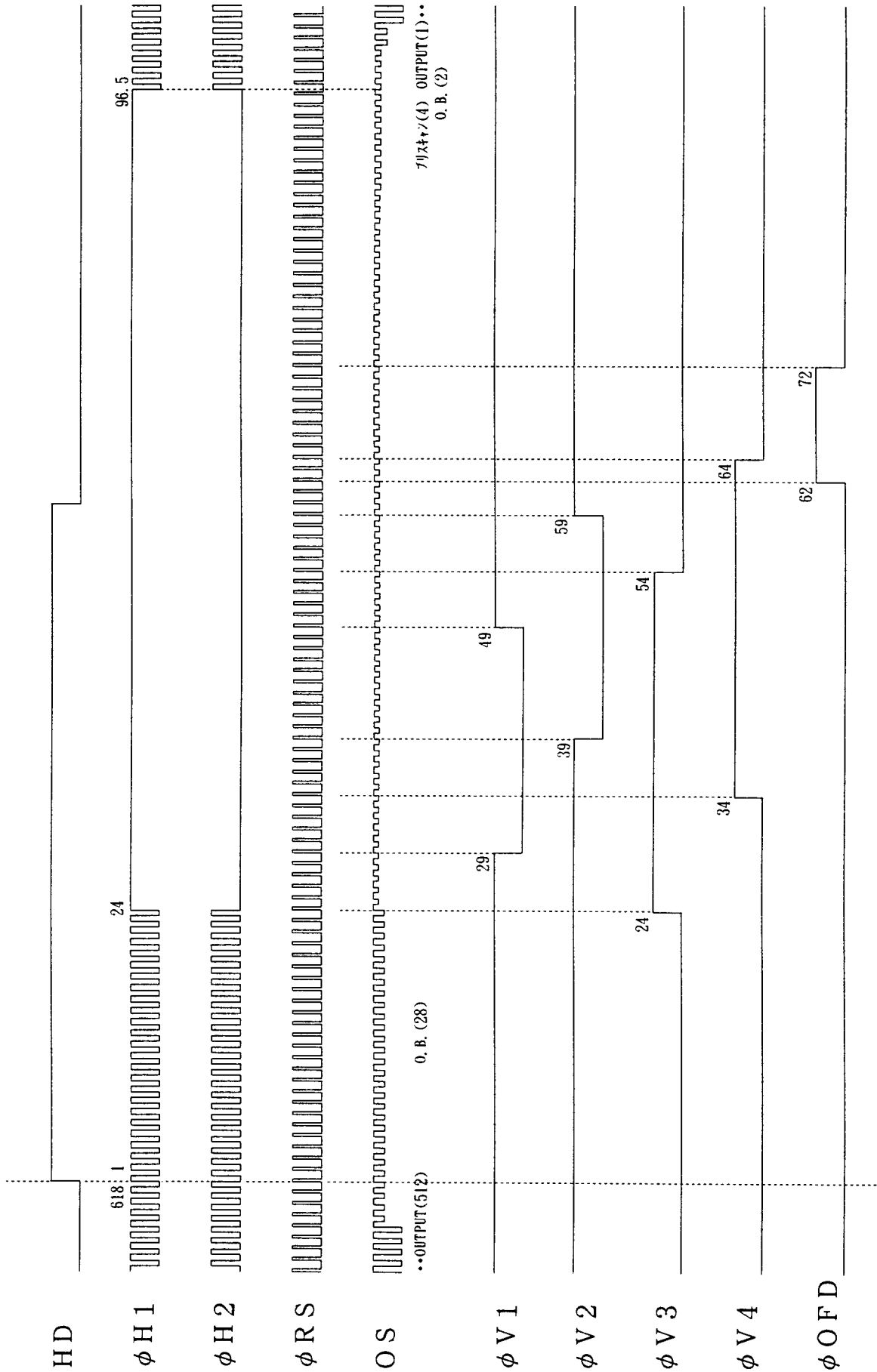
- Drive method : Field accumulation.
- DC and AC conditions : the typical values under the recommended operating conditions.
- Ta : +25°C, but +60°C for Item No. 3 and 4.
- Temperature of light source : 3200 K.
Infrared absorbing filter (CM-500, 1 mm) is used.

【 Notes 】

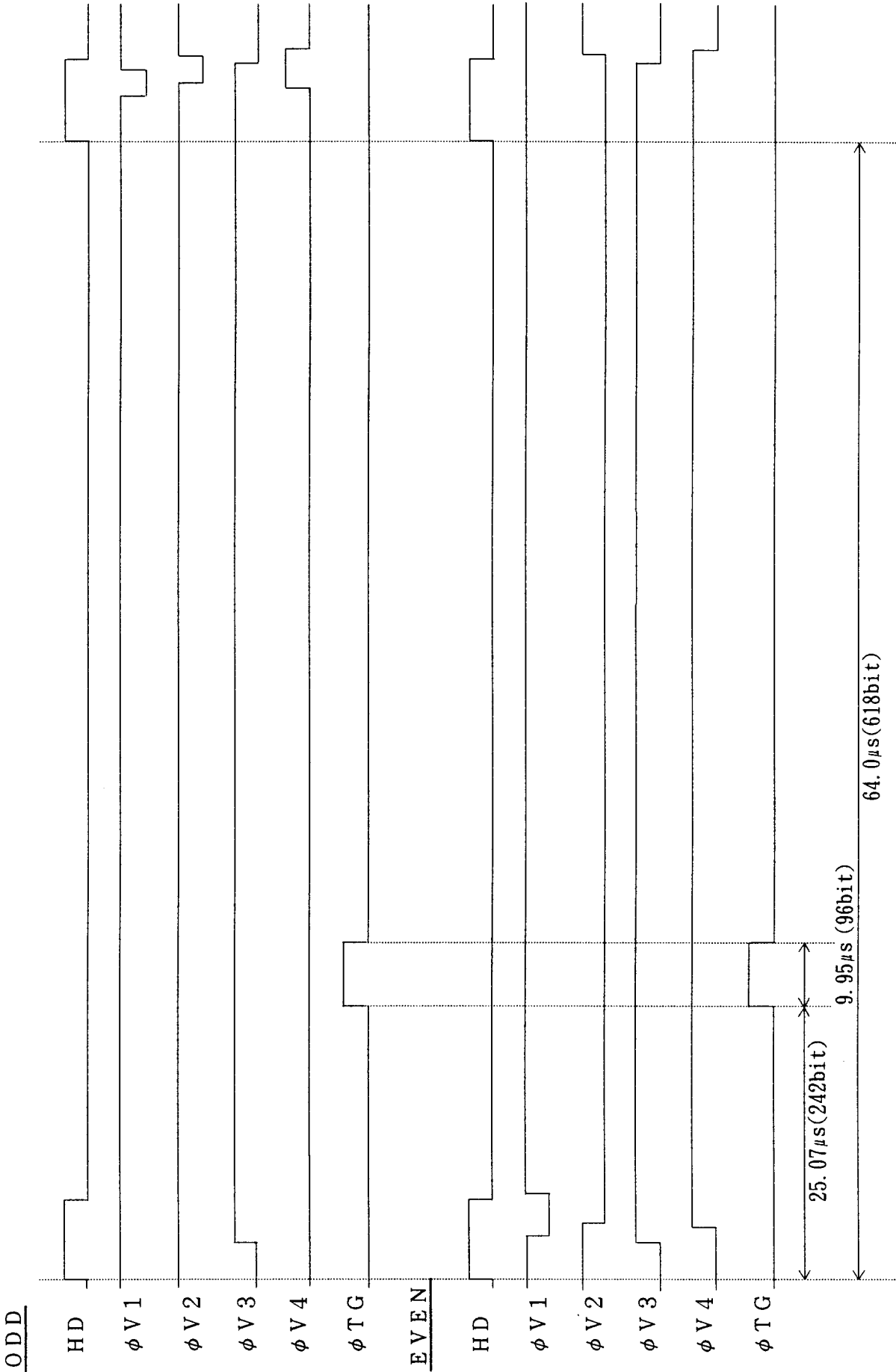
- (a) The image area is divided into 10×10 segments. The voltage of a segment is the average of output voltage from all the pixels within the segment.
PRNU is defined by $(V_{\max} - V_{\min}) / V_o$, where V_{\max} and V_{\min} are the maximum and the minimum values of each segment's voltage respectively, when the average output voltage V_o is 150 mV.
 - (b) The image area is divided into 10×10 segments. The saturation signal is defined as the minimum of each segment's voltage which is the average of output voltage from all the pixels within the segment, when the exposure level is set as 10 times, compared to standard level.
 - (c) The average output voltage under a non-exposure condition.
 - (d) The image area is divided into 10×10 segments.
DSNU is defined by $(V_{d\max} - V_{d\min})$ under the non-exposure condition where $V_{d\max}$ and $V_{d\min}$ are the maximum and the minimum values of each segment's voltage, respectively, that is the average output voltage over all pixels in the segment.
 - (e) The average output voltage when a 1000 lux light source attached with a 90% reflector is imaged by a lens of F4, f50 mm.
 - (f) The sensor is adjusted to position a $V/10$ square at the center of image area where V is the vertical length of the image area. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum of the pixel voltage in the $V/10$ square.
 - (g) The sensor is exposed at the exposure level corresponding to the standard condition preceding non-exposure condition. AI is defined by the ratio between the output voltage measured at the 1st field during the non-exposure period and the standard output voltage.
 - (h) The sensor is adjusted to position a $V/10$ square at the center of image area.
ABL is the ratio between the exposure at the standard condition and the exposure at a point where a blooming is observed.
- ◆ Within the recommended operating condition of VOD, VOFD of the internal output satisfy with ABL larger than 1000 times exposure of the standard exposure condition, and v_{sat} larger than 550mV.

7. TIMING DIAGRAM EXAMPLE

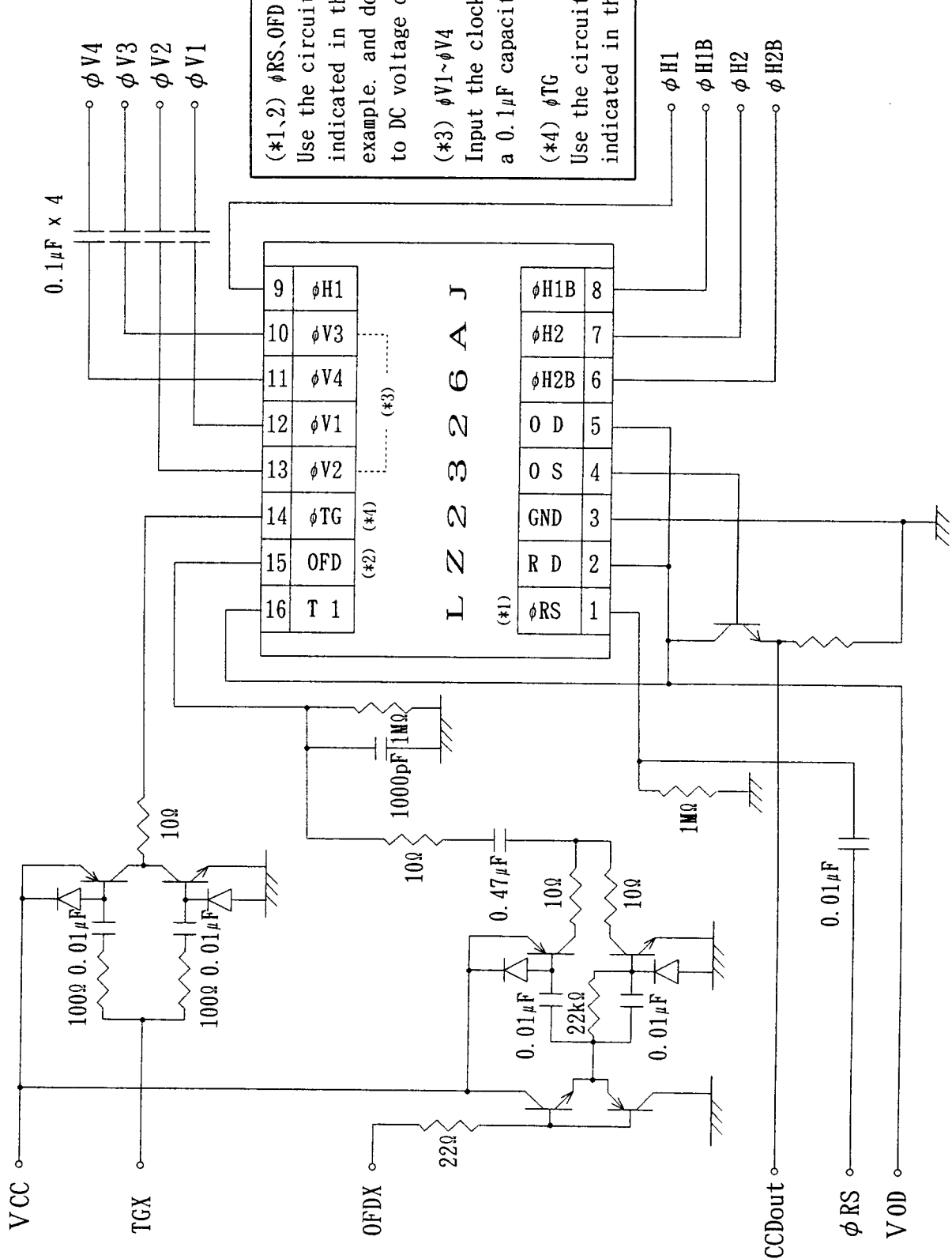
HORIZONTAL TRANSFER



READOUT TIMING



8. STANDARD OPERATING CIRCUIT EXAMPLE



9. SPECIFICATION FOR BLEMISH

1) Definition of blemish

Blemish	Level of blemish (mV)	Permitted number of blemish	COMMENT
White blemish(I) (Exposed)	$12 \leq B$	0	<ul style="list-style-type: none"> • B is defined in fig. 9(a). • $V_{out} = 75\text{mV}$.
	$B < 12$	no count	
Black blemish(I) (Exposed)	$12 \leq B$	0	
	$B < 12$	no count	
White blemish(II) (Non-exposed)	$10 \leq B$	0	<ul style="list-style-type: none"> • B is defined in fig. 9(b). • Non-exposure condition.
	$B < 10$	no count	
White blemish(III) (Shutter mode)	$4.5 \leq B$	0	<ul style="list-style-type: none"> • B is defined in fig. 9(a). • $V_{out} = 15\text{ mV}$.
	$B < 4.5$	no count	
Black blemish(III) (Shutter mode)	$4.5 \leq B$	0	<ul style="list-style-type: none"> • The electronic shutter speed is set at $1/10000\text{ s}$
	$B < 4.5$	no count	

B : Blemish level defined in fig. 9.

V_{out} : Average output voltage

2) Measuring condition

1. Operating temperature : 60°C
2. Measuring area : Measurement excludes the outer 10 pixels;
includes the optical black pixels.

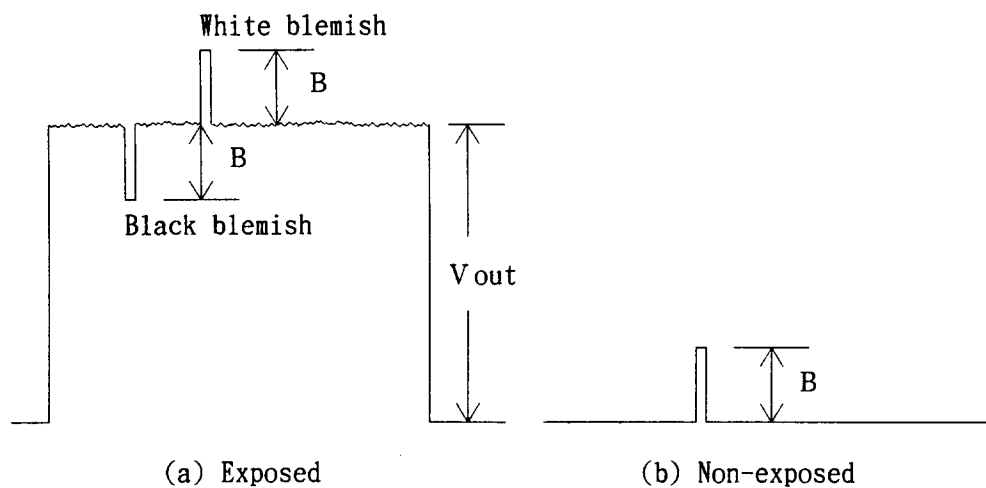


fig. 9 Definition of the blemish level

10. CAUTIONS FOR USE

10.1 Package Breakage

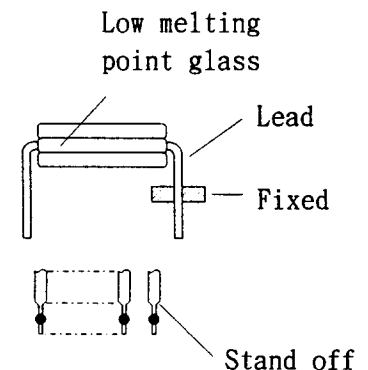
In order to prevent the package from being broken, observe the following instructions:

- 1) The CCD is a precision optical component and the package material is ceramic. Therefore,
 - * Take care not to drop the device when mounting, handling, or transporting.
 - * Avoid giving a shock to the package. Especially when leads are fixed to the socket and the circuit board, small shock could break the package more easily than when the package isn't fixed.
- 2) When applying force for mounting the device or any other purposes, fix the leads between a joint and a stand-off, so that no stress will be given to the jointed part of the lead. In addition, when applying force, do it at a point below the stand-off part.
 - ... The leads of the package are fixed with low melting point glass, so stress added to a lead could cause a crack in the low melting point glass in the jointed part of that lead.
- 3) When mounting the package on the housing, be sure that the package is not bent.
 - ... If a bent package is forced into place between a hard plate or the like, the package may be broken.

Example for mounting

 - * Place the buffers between the package and the housing.
 - * Keep the bottom side of the package free.
- 4) If any damage or breakage occur on the surface of the glass cap, its characteristics could deteriorate. Therefore,
 - * Do not hit the glass cap.
 - * Do not give a shock large enough to cause distortion.
 - * Do not scrub or scratch the glass surface.

Even a soft cloth or applicator, if dry, could cause dust to scratch the glass.



10.2 Electrostatic damage

As compared with general MOS-LSI, CCD has lower ESD.

Therefore, please take the following anti-static measures when handling the CCD:

- 1) Always discharge static electricity by grounding the human body and the instrument to be used.

To ground the human body, provide resistance of about 1 Meg ohm between the human body and the ground to be on the safe side.
- 2) When directly handling the device with fingers, hold the part without leads and do not touch any lead.
- 3) To avoid generating static electricity,
 - a. do not scrub the glass surface with cloth or plastic
 - b. do not attach any tape or labels
 - c. do not clean the glass surface with dust-cleaning tape
- 4) When storing or transporting the device, put it in a container of conductive material.

10.3 Dust and contamination

Dust or contamination on the glass surface could deteriorate the output characteristic or cause a scar. In order to minimize dust or contamination on the glass surface, take the following precautions:

- 1) Handle CCD in a clean environment such as a cleaned booth.
(The cleanliness level should be, if possible, class 1000 at least.)
- 2) Do not touch the glass surface with fingers. If dust or contamination gets on the glass surface, the following cleaning method is recommended:
 - * Dust from static electricity should be blown off with an ionized air blower.
For anti-electrostatic measures, however, ground all the leads on the device before blowing off the dust.
 - * The contamination on the glass surface should be wiped off with a clean applicator soaked in Isopropyl alcohol. Wipe slowly and gently in one direction only.
 - ... Frequently replace the applicator and do not use the same applicator to clean more than one device.

Note: In most cases, dust and contamination are unavoidable, even before the device is first used. It is, therefore, recommended that the above procedures should be taken to wipe out dust and contamination before using the device.

10.4 Cautions

- 1) Soldering should be manually performed within 5 seconds at 350°C maximum at soldering iron.
- 2) Avoid using or storing the CCD at high temperature or high humidity as it is a precision optical component. Do not give a mechanical shock to the CCD.
- 3) Do not connect the device to or disconnect it from the plug socket while power is being applied.
- 4) The exit pupil position of lens should be more than 20mm from top surface of CCD.

1 1 PACKAGE OUTLINE AND PACKING SPECIFICATION

1 . Package Outline Specification

Refer to attached drawing

(The seal resin stick out from the package shall be passed. And, the seal resins are two kinds of colors, white and transparency.)

2 . Markings

Marking contents

- (1) Product name : L Z 2 3 2 6 A J
 (2) Company name : S H A R P
 (3) Country of origin : J A P A N
 (4) Date code : Y Y W W X X X

Denotes the production ref. code.(1 ~ 2 figures)

Denotes the production day of the week.

1	2	3	4	5	6	7
SUN.	MON.	TUE.	WED.	THU.	FRI.	SAT.

Denotes the production week.

(01,02,03, . . . ,52,53)

Denotes the production year.

(Lower two digits of the year.)

Positions of markings are shown in the package outline drawing .

But, markings shown in that drawing are not provided any measurements of their characters and their positions.

3 . Packing Specification

3 - 1 . Packing materials

Material Name	Material Spec.	Purpose
Device case	Cardboard(150devices/case)	Device tray fixing
Device tray	Conductive plastic (50devices/tray)	Device packing(3trays/case)
Cover tray	Conductive plastic(1tray/case)	Device packing
PP band	Polypropylene	Device tray fixing
Buffer	Cardboard(2sheets/case)	Shock absorber of device tray
Plastic film bag	Plastic film	Device tray fixing
Tape	Paper	Sealing plastic film bag and device case
Label	Paper	Indicates part number, quantity and date of manufacture

3 - 2 . External appearance of packing

Refer to attached drawing

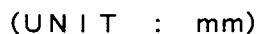
4 . Precaution

- Before unpacking, confirm the imports of the chapter "Handling Precaution" in this device specifications.
- Unpacking should be done on the stand treated with anti-ESD. At that time, the same anti-ESD treatment should be done to operator' s body, too.

ISSUE NUMBER

(NOTE)

7 3 2 5 G A D C



材質 MATERIAL	仕 上 FINISH	名 称 NAME	WDIP16-N-500C												
			Package Outline Specification												
MODULE ASSEMBLY APPLICATION ENGINEERING DEPARTMENT		コード CODE	:	:	:	:	:	:	:	:	:	:	:	:	:
		INTEGRATED CIRCUITS (IC) GROUP		図 番 DRAWING No.	G:D:G:0:1:6:B-1:6:E:6										
SHARP CORPORATION															



材質 MATERIAL	仕上 FINISH	名称 NAME	External Appearance of Packing
		コード CODE	. .
MODULE ASSEMBLY APPLICATION ENGINEERING DEPARTMENT			
INTEGRATED CIRCUITS (IC) GROUP		図番 DRAWING No.	K : S : E : C - 1 5 0 T : 2 - 0
SHARP CORPORATION			