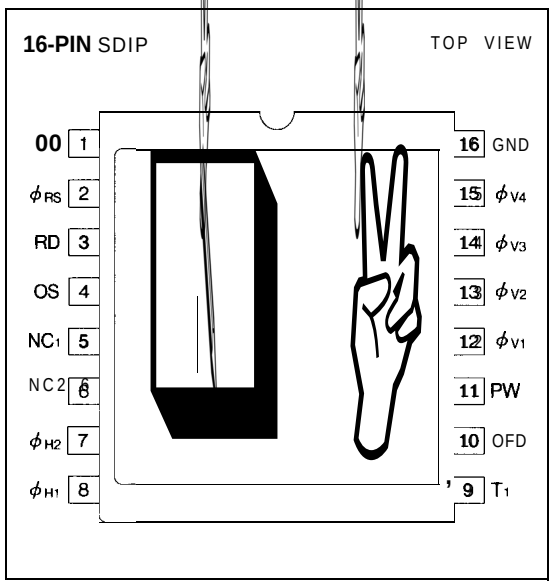
# LZ2323H5

1/3 type Color CCD Area Sensor for PAL

## DESCRIPTION

LZ2323H5 is a 1/3-type (6.0 mm) solid-state image sensor that consists of PN phote-diodes and CCDS (charge-coupled devices). Having approximately 320000 pixels (horizontal 542 X vertical 582), the sensor probides a high resolution stable color image.

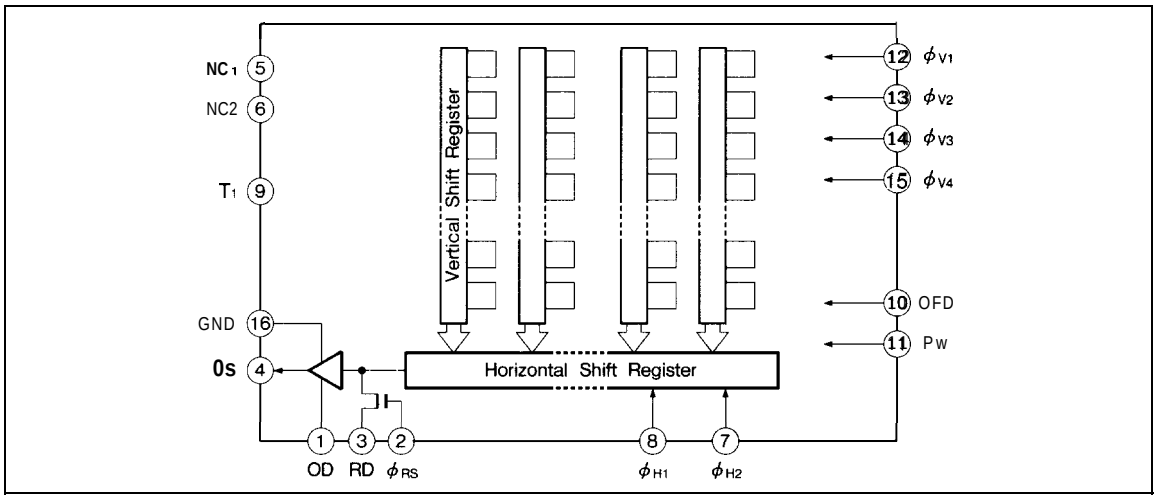
## PIN CONNECTIONS




## FEATURES

- Number of pixels : 512 (H) X 582 (V)
  Pixel pitch : 9.6 μm (H) X 6.3 μm (V)
  Number of optically black pixels
  : Horizontal; front 2 and rear 28
- Complementary color filters of Mg, G, Cy and Ye
- Low fixed pattern noise and lag
- No sticking and no image distortion
- Blooming suppression structure
- Built-in output amplifier
- Variable electronic shutter (1/50 to 1/1 0000 s)
- Compatible with PAL standard
- Package : 16-pin SDIPICERDIP](WDIPO1 6-N-0500C)

## BLOCK DIAGRAM





"In the absence of confirmation by device specification sheets, SHARP takes no responsibility for any defects that recur in equipment using any of WARP's devices, shown in catalogs, data books, etc. Contact SHARP in order to obtain the latest version of the device specification sheets before using any SHARPS device."

## PIN DESCRIPTION

| SYMBOL | PIN NAME | NOTE |
|---|---|---|
| RD | Reset transistor drain | |
| OD | Output transistor drain | |
| 0s | Video output | |
| $\phi_{RS}$ | Reset transistor gate clock | |
| $\phi_{V1}, \phi_{V2}, \phi_{V3}, \phi_{V4}$ | Vertical shift register gate clink | |
| $\phi_{H1}, \phi_{H2}$ | Horizontal shift register gate clock | |
| OFD | Overflow drain | |
| PW | P type well | |
| GND | Ground | |
| $T_I$ | Test terminal | |
| NC I , NC2 | No connection | 1 |

NOTE :

1. Connect each pin to GND directly or through a capacitor larger than 0.047 $\mu$F.

## ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C )

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Output transistor drain voltage | Voo | O to +18 | v |
| Reset transistor drain voltage | $V_{RD}$ | O to +18 | v |
| Overflow drain voltage | Vom | o to +55 | v |
| Test terminal, $T_1$ | $V_{T1}$ | O to +18 | v |
| Reset gate clock voltage | $V_{\phi RS}$ | –0.3 to +18 | v |
| Vertical shift register clock voltage | $V_{\phi V}$ | –9.0 to +18 | v |
| Horizontal shift register clock voltage | $V_{\phi H}$ | –0.3 to +18 | v |
| Voltage difference between PW and vertical clock | $V_{PW}-V_{\phi V}$ | –27 to +0 | v |
| Storage temperature | Tstg | –40 to +80 | ℃ |
| Operating ambient temperature | Topr | –20 to +70 | ℃ |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| Operating ambient temperature | | Topr | | 25.0 | | ‘c | |
| Output transistor drain voltage | | Voo | 14.5 | 15,0 | 16.0 | v | |
| Reset transistor drain voltage | | $V_{RD}$ | | VOD | | v | |
| Overflow drain voltage | When DC is applied | VOm | 5.0 | (adj.) | 19.0 | v | 1 |
| | When pulse is applied p-p level | $V_{\phi OFD}$ | 22.0 | | | v | 2 |
| Ground | | GND | | 0.0 | | v | |
| P-well voltage | | VPW | -9.0 | | $V_{\phi VL}$ | V | |
| Test terminal, $T_1$ | | $V_{T1}$ | | VOD | | v | |
| Vertical shift register clock | LOW level | $V_{\phi V1L}$, $V_{\phi V2L}$ v $\phi V3L$, v $\phi V4L$ | -8.5 | - 8.0 | -7.5 | v | |
| | INTERMEDIATE level | $V_{\phi V1I}$, $V_{\phi V2I}$ $V_{\phi V3I}$, $V_{\phi V4I}$ | | 0.0 | | v | |
| | HIGH level | $V_{\phi V1H}$, $V_{\phi V3H}$ | 16.0 | 16.5 | 17.0 | V | |
| Horizontal shift resister clock | LOW level | $V_{\phi H1L}$, $V_{\phi H2L}$ | - 0.05 | 0.0 | 0.05 | v | |
| | HIGH level | $V_{\phi H1H}$, $V_{\phi H2H}$ | 4.7 | 5.0 | 6.0 | v | |
| Reset gate clock | LOW level | $V_{\phi RSL}$ | 0.0 | | VRD - 13,0 | v | |
| | HIGH level | $V_{\phi RSH}$ | VRD - 8.5 | | 9.5 | v | |
| Vertical shift register clock frequency | | $f_{\phi V1}$, $f_{\phi V2}$ $f_{\phi V3}$, $f_{\phi V4}$ | | 15,63 | | kHz | |
| Horizontal shift register clock frequency | | $f_{\phi H1}$, $f_{\phi H2}$ | | 9.66 | | MHz | |
| Reset aate clock frequency | | $f_{\phi RS}$ | | 9.66 | | MHz | |

**NOTES :**

1. When DC voltage is applied, shutter speed is 1 /50 seconds.
2. When pulse is applied, shutter speed is less than 1 /50 seconds

## ELECTRICAL CHARACTERISTICS (Drive method : Field Accumulation)

(Ta = 25°C, Operating conditions : typical values for the recommended operating conditions, Color temperature of light source : 3200 K / IR cut-off filter (CM-500, 1 mmt))

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|
| Photo response non-uniformity | PRNU | | | 15 | % | 2 |
| Carrier saturation | Vsat | 400 | | | mV | 3 |
| Dark output voltage | Vdark | | 0.3 | 3.0 | mV | 1, 4 |
| Dark signal non-uniformity | DSNU | | 0.6 | 2.0 | mV | 1, 5 |
| Sensitivity | R | 400 | 550 | | mV | 6 |
| Smear ratio | SMR | | 0.009 | 0.016 | % | 7 |
| Image lag | AI | | | 1.0 | % | 8 |
| Blooming suppression ratio | ABL | 100 | | | | 9 |
| Output transistor drain current | $I_{OD}$ | | 4.0 | 8.0 | mA | |
| Output impedance | Ro | | 350 | | Ω | |
| Vector breakuo | | | | 7.0 | °, % | 10 |
| Line crawling | | | | 3.0 | % | 11 |
| Luminance flicker | | | | 2.0 | % | 12 |

. The standard output voltage is defined as 150 mV by the average output voltage under uniform illumination.

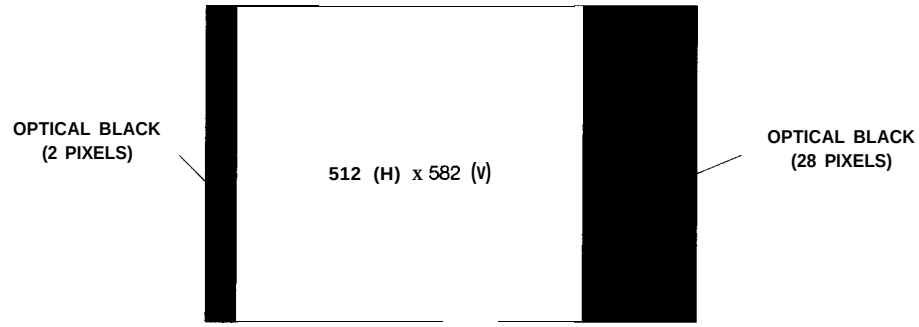
● The standard exposure level is defined when the average output voltage is 150 mV under uniform illumination.

. $V_{OFD}$ should be adjusted to the minimum voltage with that ABL satisfy the specification,

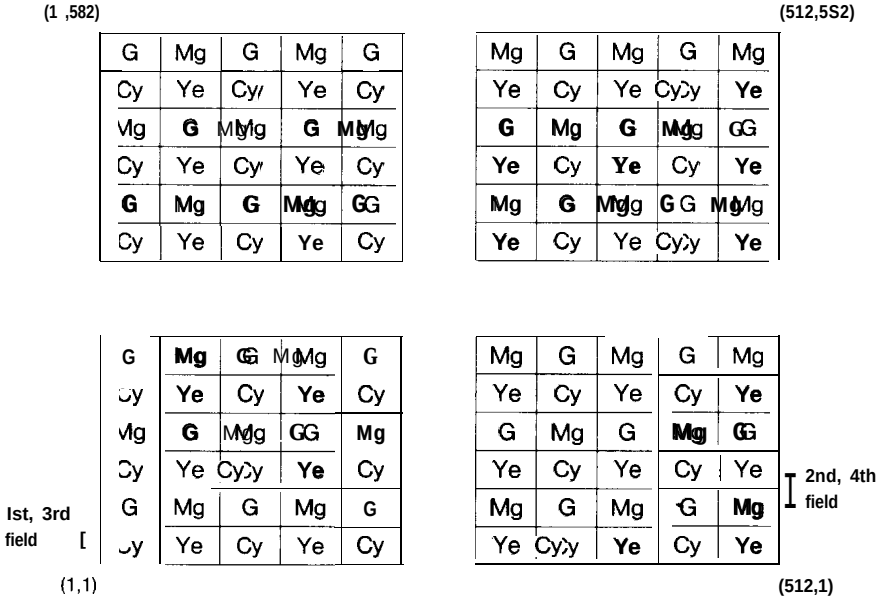
### NOTES :

1. Ta : +60°C
2. The image area is divided into 10x 10 segments. I-he segment's voltage is the average output voltage of all the pixels within the segment. PRNU is defined by (Vmax – Vmin)/Vo, where Vmax and Vmin are the maximum and the minimum values of each segment's voltage respectively, when the average output voltage Vo is 150 mV.
3. The output voltage measured at the carrier peak when the carrier signal reaches maximum.
4. The average output voltage under a non-exposure condition.
5. The image area is divided into 10x 10 segments. OSNU is defined by (Vdmax – Vdmin) under the non-exposure condition where Vdmax and Vdmin are the maximum and the minimum values of each segment's voltage, respectively, that is the average output voltage over all pixels in the segment.
6. The average output voltage when a 1000 lux light source attached with a 90% reflector is imaged by a lens of F4, f50 mm.
7. The sensor is adjusted to position a V/l O square at the center of image area where V is the vertical length of the image area. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum of the pixel voltage in the V/l O square.
6. The sensor is exposed at the exposure level corresponding to the standard condition preceding non-exposure condition. AI is defined by the ratio between the output voltage measured at the 1st field during the non-exposure period and the standard output voltage.
9. The sensor is adjusted to position a V/l O square at the center of image area. ABL is the ratio between the exposure at the standard condition and the exposure at a point where a blooming is observed.
10. Observed with a vector scope when the color bar chart is imaged under the standard exposure condition.
11. The difference between the average output voltage of the (Mg + Ye), (G+ Cy) line and the (Mg + Cy), (G+ Ye) line under the standard exposure condition.
12. The difference between the average output voltage of the odd field and the even field.

## PIXEL STRUCTURE




## COLOR FILTER ARRAY

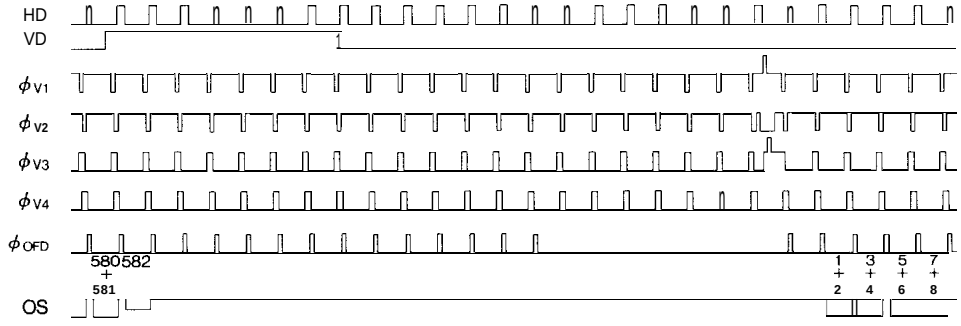


## M NG DIAGRAM EXAMPLE

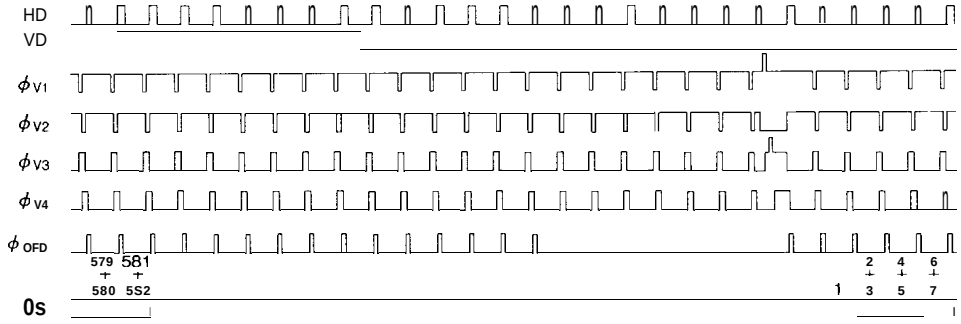
### VERTICAL TRANSFER TIMING

Shutter speed
1 /2000 s

**(1st, 3rd FIELD)**



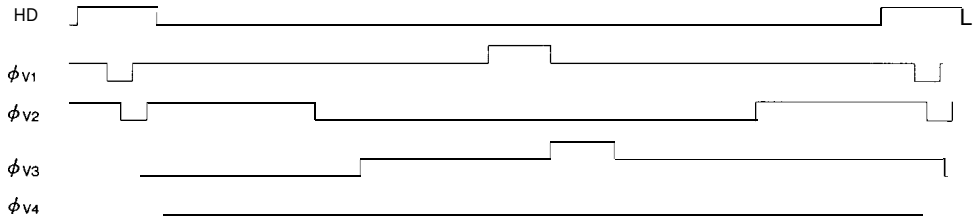

**(2nd, 4th FIELD)**



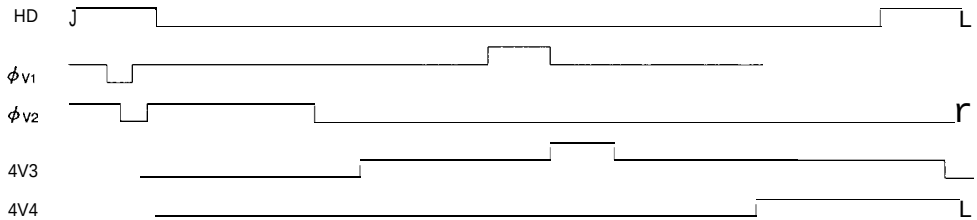

### HORIZONTAL TRANSFER TIMING

READOUT TIMING

**(1st, 3rd FIELD)**




(2nd, **4th FIELD)**



## SYSTEM CONFIGURATION EXAMPLE