SHARP

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To ;

REFERENCE

SPECIFICATIONS

Product Type 1/3 type solid state B/W imaging device for EIA system
(Versatile output for mirror and normal image)

Model No. LZ2316J1

※This specifications contains 20 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED

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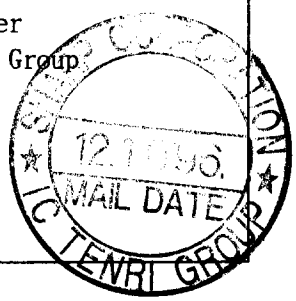
Development Dept. 3
Logic IC Engineering Center
TENRI Integrated Circuits Group
SHARP CORPORATION



● When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
- ·Office electronics
- ·Instrumentation and measuring equipment
- ·Machine tools
- ·Audiovisual equipment
- ·Home appliances
- ·Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
- ·Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- ·Mainframe computers
- ·Traffic control systems
- ·Gas leak detectors and automatic cutoff devices
- ·Rescue and security equipment
- ·Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
- ·Aerospace equipment
- ·Communications equipment for trunk lines
- ·Control equipment for the nuclear power industry
- ·Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

● Please direct all queries regarding the products covered herein to a sales representative of the company.

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1. GENERAL

LZ2316J1 is a 1/3 type (6.0mm) solid state imaging device consisting of PN photo-diodes and CCDs(charge-coupled devices) driven by only positive voltages.
Having about 270,000 pixels(horizontal 542 x vertical 492), it allows a stable B/W normal or mirror image to be obtained at high resolution.

1 Features

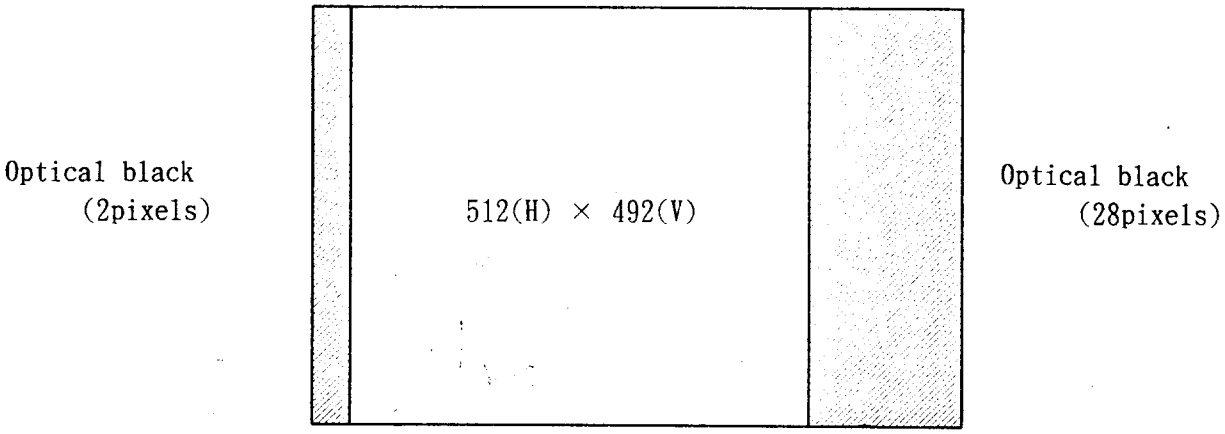
1) Number of video picture elements : Horizontal 512 x vertical 492
   Pixel pitch : Horizontal 9.6 μm x vertical 7.5 μm
   Number of optically black pixel : Horizontal; front 2 and rear 28
2) Reduced fixed pattern noise and lag
3) No sticking and no image distortion
4) Blooming suppression structure
5) Built-in output amplifier
6) 16-pin shrink DIP
   (Row space: 12.70 mm)
7) Variable electronic shutter
8) N-type silicon substrate
9) Not designed or rated as radiation hardened
10) Compatible with EIA standard
11) Normal or mirror image output available from common output terminal.

2 Applications

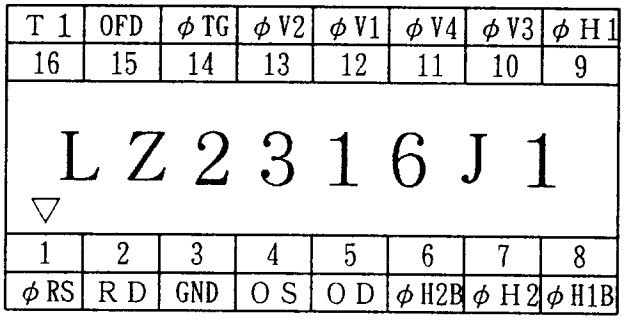
1) Camcorders
2) Monitor cameras(TV doorphone, Video phone, Rear view cameras, etc.)
3) Pattern recognition

※ The circuit diagram and others included in this specification are intended for use to explain typical application examples. Therefore, we take no responsibility for any problem as may occur due to the use of the included circuit and for any problem with industrial proprietary rights or other rights.

2. COMPOSITION OF PIXELS



3. PIN ASSIGNMENT AND PIN IDENTIFICATION



(TOP VIEW)

Symbol	Pin name
RD	Reset transistor drain
OD	Output transistor drain
OS	Video output
φRS	Reset transistor gate clock
φV1, φV2, φV3, φV4	Vertical shift register gate clock
φH1, φH2, φH1B, φH2B	Horizontal shift register gate clock
φTG	Transfer gate clock
OFD	Overflow drain
T1	Test terminals
GND	Ground

4. ABSOLUTE MAXIMUM RATING

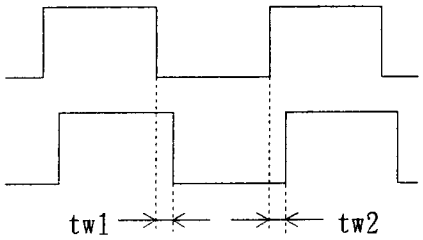
(Ta = 25℃)

Item	Symbol	Rating	Unit
Output transistor drain voltage	VOD	0 to +16	V
Reset transistor drain voltage	VRD	0 to +16	V
Test terminal, T1	VT1	0 to +16	V
Reset gate clock voltage	VφRS	-0.3 to +16	V
Vertical shift register clock voltage	VφV	-0.3 to +16	V
Horizontal shift register clock voltage	VφH	-0.3 to +16	V
Transfer gate clock voltage	VφTG	-0.3 to +16	V
Overflow drain voltage	VOFD	0 to +30	V
Storage temperature	Tstg	-40 to +85	℃
Operating ambient temperature	Topr	-20 to +70	℃

5. RECOMMENDED OPERATING CONDITIONS

Item		Symbol	Minimum	Typical	Maximum	Unit
Operating ambient temperature		Topr		25.0		℃
Output transistor drain voltage		VOD	12.0	12.5	14.0	V
Reset transistor drain voltage		VRD		VOD		V
Overflow drain voltage	When DC is applied(note1)	VOFD	3.0		12.0	V
	When pulse is applied p-p level (note2)	VφOFD	12.0	12.5	14.0	V
Test terminals, T1		VT1		VOD		V
Ground voltage		GND		0.0		V
Transfer gate clock	LOW level	VφTGL	-0.05	0.0	0.05	V
	HIGH level	VφTGH	12.0	12.5	14.0	V
Vertical shift register clock	LOW level	VφV1~4L	-0.05	0.0	0.05	V
	HIGH level	VφV1~4H	4.7	5.0	6.0	V
Horizontal shift register clock	LOW level	VφH1~2L, VφH1~2BL	-0.05	0.0	0.05	V
	HIGH level	VφH1~2H, VφH1~2BH	4.7	5.0	6.0	V
Reset gate clock	LOW level	VφRSL	0.0		VRD-10.5	V
	HIGH level	VφRSH	VRD-6.0		9.5	V
Vertical shift register clock freq.		fφV1~4	--	15.73		kHz
Horizontal shift register clock freq.		fφH1~2, fφH1~2B		9.53		MHz
Reset gate clock freq.		fφRS		9.53		MHz
Horizontal shift register clock phase		tw1, tw2 (note3)	0.0	5.0	10.0	ns

(note1) When DC voltage is applied, shutter speed is 1/60 seconds.
(note2) When pulse is applied, shutter speed is less than 1/60 seconds.
(note3)



φH1, $\overline{\phi H2}$

φH1B, $\overline{\phi H2B}$: Normal image output mode

$\overline{\phi H1B}$, φH2B : Mirror image output mode

※ To apply power, first connect GND and then turn on OFD and then turn on other powers and pulses.
Do not connect the device to or disconnect it from the plug socket while power is being applied.

6. CHARACTERISTICS

No.	Item	Symbol	Note	Min.	Typ.	Max.	Unit
1	Photo response non-uniformity	PRNU	(a)			15	%
2	Saturation signal	Vsat	(b)	500			mV
3	Dark output voltage	Vdark	(c)		5.0	15.0	mV
4	Dark signal non-uniformity	DSNU	(d)		1.5	5.0	mV
5	Sensitivity	R	(e)	320	450		mV
6	Smear ratio	SMR	(f)		0.006	0.016	%
7	Image lag	AI	(g)			1.0	%
8	Blooming suppression ratio	ABL	(h)	1000			
9	Current dissipation	I_{OD}			4.0	8.0	mA
10	Output impedance	Ro			400		Ω

【 Conditions 】

- Drive method : Field accumulation.
- DC and AC conditions : the typical values under the recommended operating conditions.
- Ta : +25℃, but +60℃ for Item No. 3 and 4.
- Temperature of light source : 3200 K.
  Infrared absorbing filter (CM-500, 1 mm) is used.

【 Notes 】

- The standard output voltage is defined as 150 mV by the average output voltage under uniform illumination.
- The standard exposure level is defined when the average output voltage is 150 mV under uniform illumination.

(a) The image area is divided into 10 x 10 segments. The voltage of a segment is the average of output voltage from all the pixels within the segment. PRNU is defined by (Vmax - Vmin) / Vo, where Vmax and Vmin are the maximum and the minimum values of each segment's voltage respectively, when the average output voltage Vo is 150 mV.

(b) The image area is divided into 10 x 10 segments. The saturation signal is defined as the minimum of each segment's voltage which is the average of output voltage from all the pixels within the segment, when the exposure level is set as 10 times, compared to standard level.

(c) The average output voltage under a non-exposure condition.

(d) The image area is divided into 10 x 10 segments. DSNU is defined by (Vdmax - Vdmin) under the non-exposure condition where Vdmax and Vdmin are the maximum and the minimum values of each segment's voltage, respectively, that is the average output voltage over all pixels in the segment.

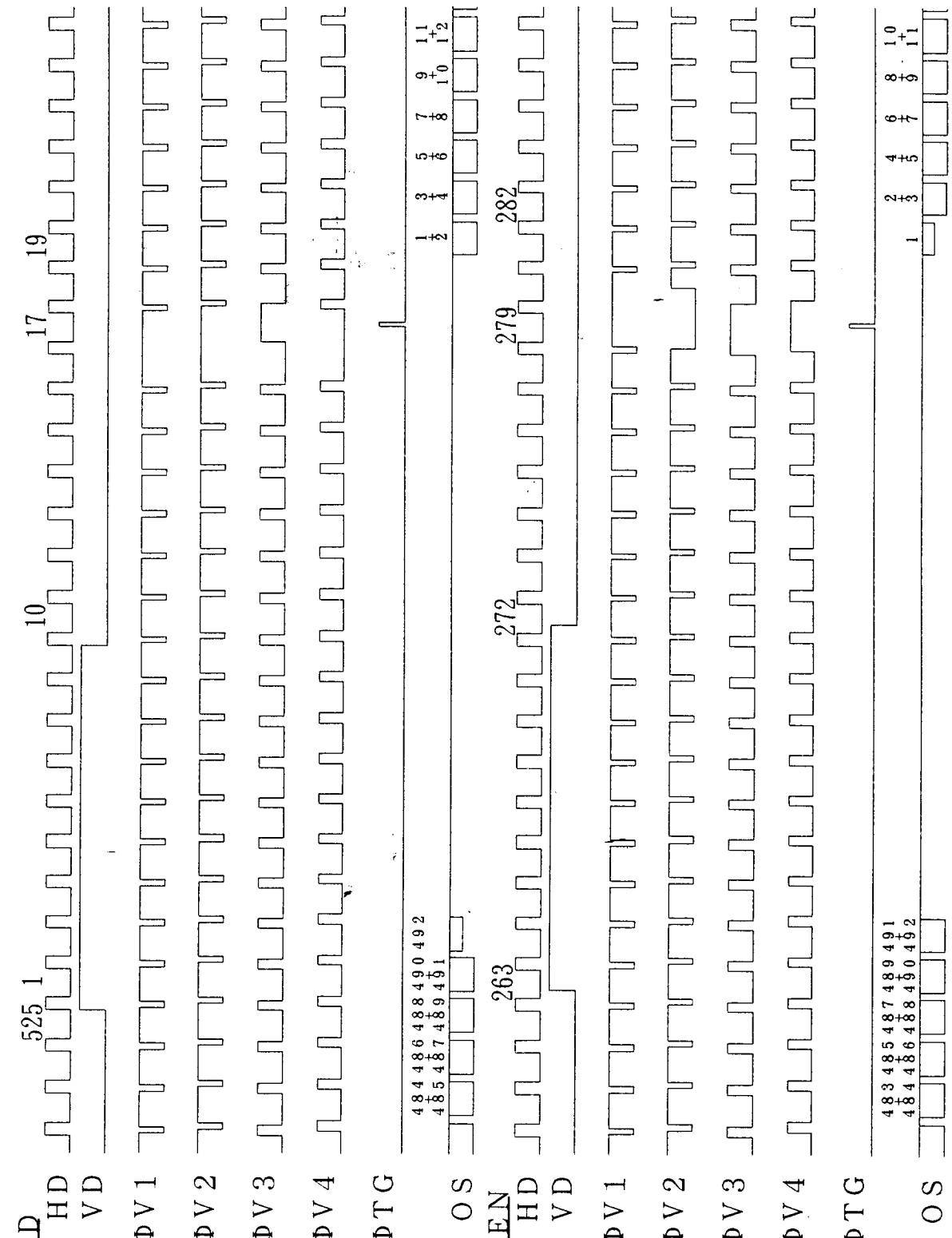
(e) The average output voltage when a 1000 lux light source attached with a 90% reflector is imaged by a lens of F4, f50 mm.

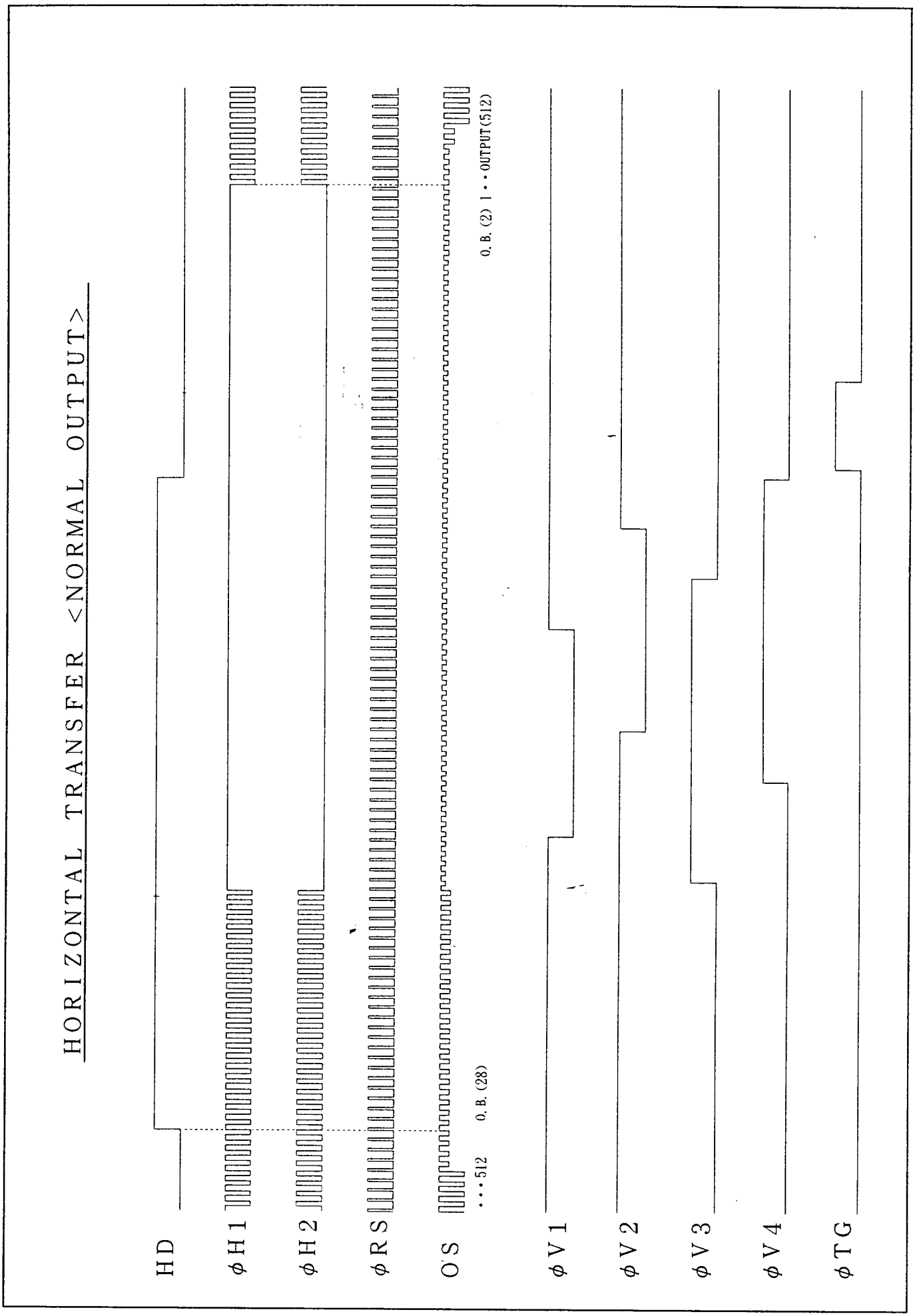
(f) The sensor is adjusted to position a V/10 square at the center of image area where V is the vertical length of the image area. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum of the pixel voltage in the V/10 square.

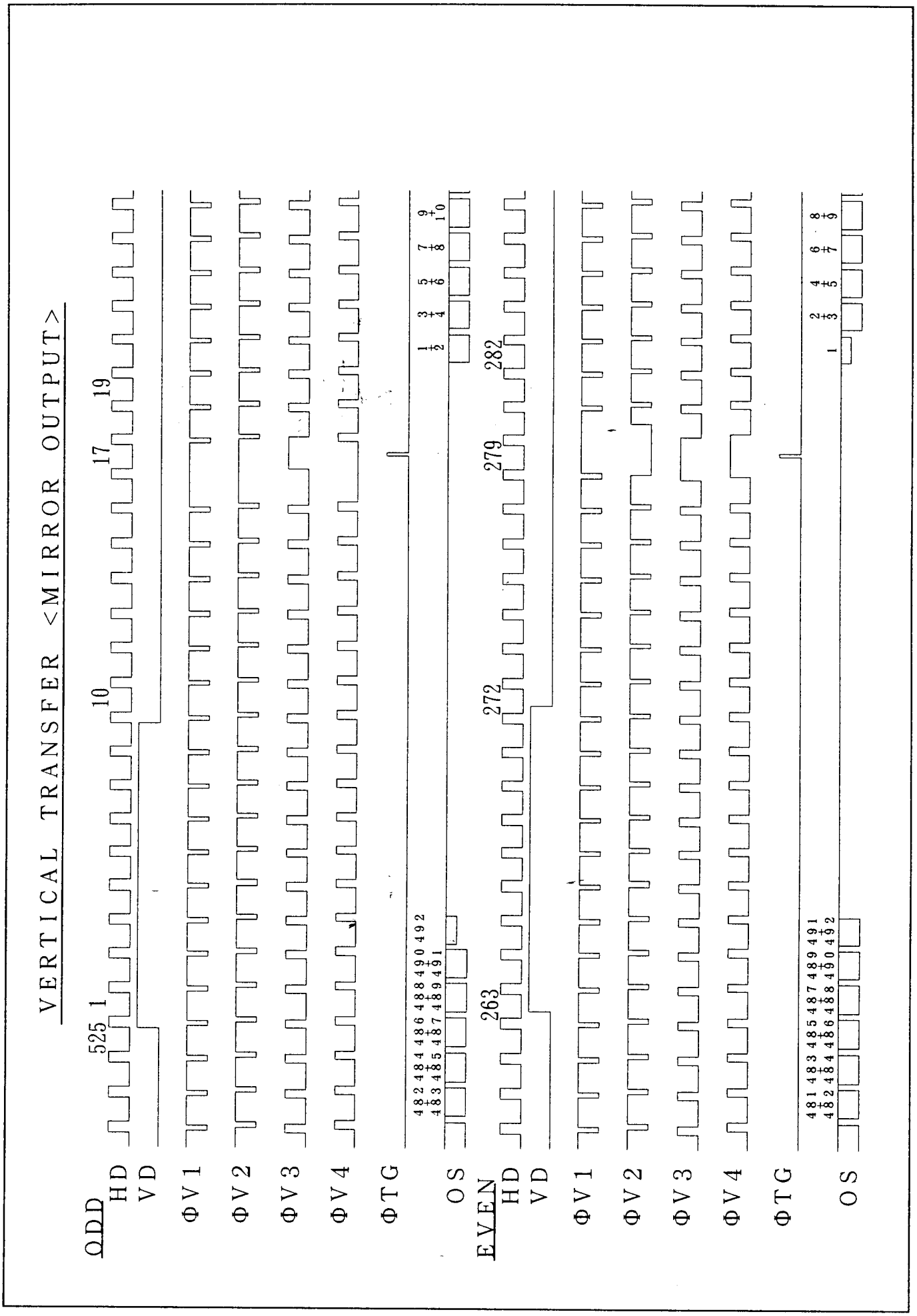
(g) The sensor is exposed at the exposure level corresponding to the standard condition preceding non-exposure condition. AI is defined by the ratio between the output voltage measured at the 1st field during the non-exposure period and the standard output voltage.

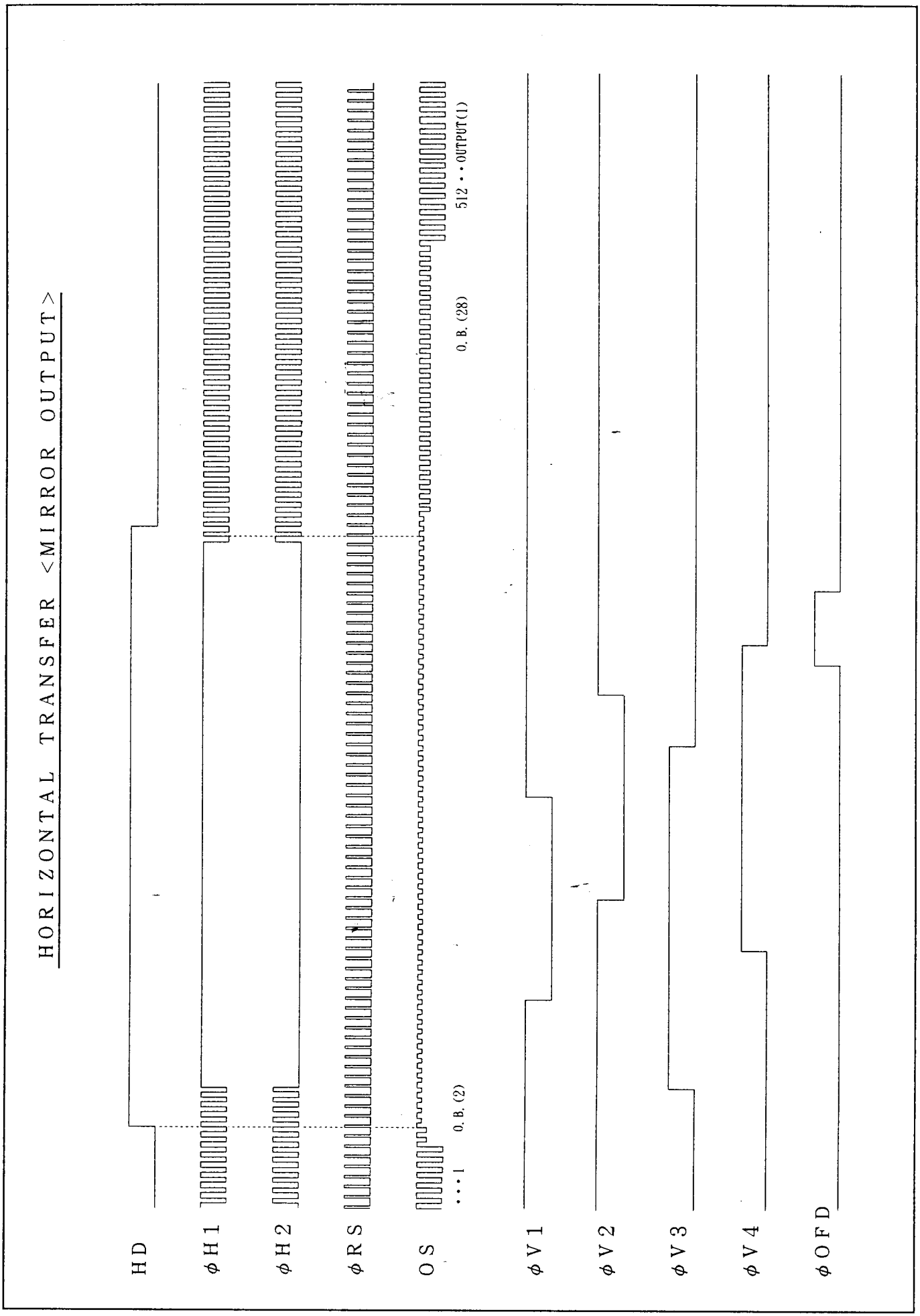
(h) The sensor is adjusted to position a V/10 square at the center of image area. ABL is the ratio between the exposure at the standard condition and the exposure at a point where a blooming is observed.

7. TIMING DIAGRAM EXAMPLE

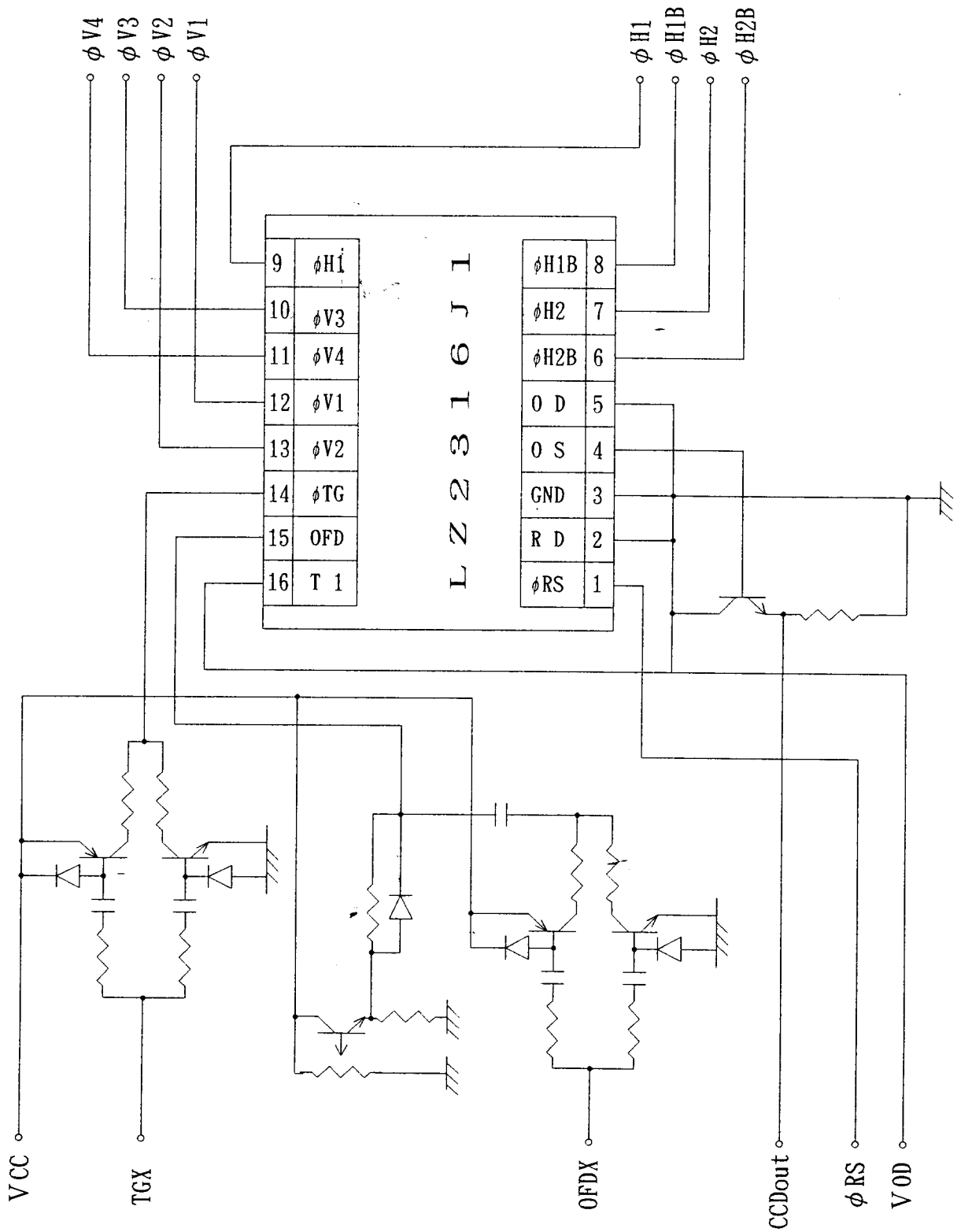



HORIZONTAL TRANSFER <NORMAL OUTPUT>
HD
φH1
φH2
φRS
OS
φV1
φV2
φV3
φV4
φTG
···512
O.B.(28)
O.B.(2) 1··OUTPUT(512)


VERTICAL TRANSFER <MIRROR OUTPUT>
ODD
HD
VD
ΦV1
ΦV2
ΦV3
ΦV4
ΦTG
OS
EVEN
HD
VD
ΦV1
ΦV2
ΦV3
ΦV4
ΦTG
OS
525
1
10
17
19
263
272
279
282


HORIZONTAL TRANSFER <MIRROR OUTPUT>
HD
φH1
φH2
φRS
OS
φV1
φV2
φV3
φV4
φOFD
···1
O. B. (2)
O. B. (28)
512 ··OUTPUT(1)

8. STANDARD OPERATING CIRCUIT EXAMPLE



9. SPECIFICATION FOR BLEMISH

1) Definition of blemish

Blemish	Level of blemish (mV)	Permitted number of blemish	COMMENT
White blemish(Ⅰ) (Exposed)	12 ≦ B	0	• B is defined in fig. 9(a). • Vout = 75mV.
	B < 12	no count	
Black blemish(Ⅰ) (Exposed)	12 ≦ B	0	
	B < 12	no count	
White blemish(Ⅱ) (Non-exposed)	10 ≦ B	0	• B is defined in fig. 9(b). • Non-exposure condition.
	B < 10	no count	
White blemish(Ⅲ) (Shutter mode)	4.5 ≦ B	0	• B is defined in fig. 9(a). • Vout = 15 mV. • The electronic shutter speed is set at 1/10000 s
	B < 4.5	no count	
Black blemish(Ⅲ) (Shutter mode)	4.5 ≦ B	0	
	B < 4.5	no count	

B :Blemish level defined in fig. 9.
Vout :Average output voltage

2) Measuring condition
1. Operating temperature : 60℃
2. Measuring area : Measurement excludes the outer 10 pixels; includes the optical black pixels.

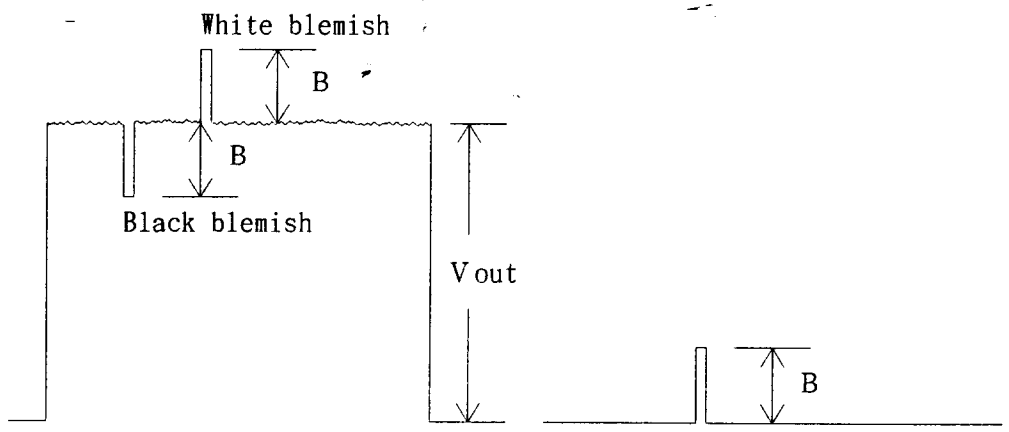


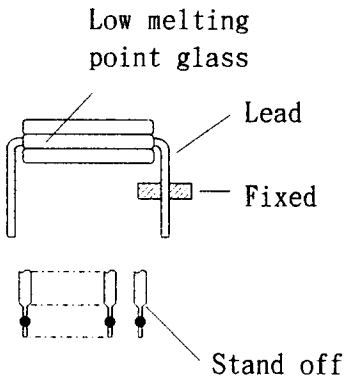
fig. 9 Definition of the blemish level

10. CAUTIONS FOR USE

10.1 Package Breakage

In order to prevent the package from being broken, observe the following instructions:

1) The CCD is a precision optical component and the package material is ceramic. Therefore,
   * Take care not to drop the device when mounting, handling, or transporting.
   * Avoid giving a shock to the package. Especially when leads are fixed to the socket and the circuit board, small shock could break the package more easily than when the package isn't fixed.
2) When applying force for mounting the device or any other purposes, fix the leads between a joint and a stand-off, so that no stress will be given to the jointed part of the lead. In addition, when applying force, do it at a point below the stand-off part.
   ··· The leads of the package are fixed with low melting point glass, so stress added to a lead could cause a crack in the low melting point glass in the jointed part of that lead.
3) When mounting the package on the housing, be sure that the package is not bent.
   ··· If a bent package is forced into place between a hard plate or the like, the package may be broken.
   Example for mounting
   * Place the buffers between the package and the housing.
   * Keep the bottom side of the package free.
4) If any damage or breakage occur on the surface of the glass cap, its characteristics could deteriorate. Therefore,
   * Do not hit the glass cap.
   * Do not give a shock large enough to cause distortion.
   * Do not scrub or scratch the glass surface.
     Even a soft cloth or applicator, if dry, could cause dust to scratch the glass.



10.2 Electrostatic damage

As compared with general MOS-LSI, CCD has lower ESD.
Therefore, please take the following anti-static measures when handling the CCD:

1) Always discharge static electricity by grounding the human body and the instrument to be used.
   To ground the human body, provide resistance of about 1 Meg ohm between the human body and the ground to be on the safe side.
2) When directly handling the device with fingers, hold the part without leads and do not touch any lead.
3) To avoid generating static electricity,
   a. do not scrub the glass surface with cloth or plastic
   b. do not attach any tape or labels
   c. do not clean the glass surface with dust-cleaning tape
4) When storing or transporting the device, put it in a container of conductive material.

10.3 Dust and contamination

Dust or contamination on the glass surface could deteriorate the output characteristic or cause a scar. In order to minimize dust or contamination on the glass surface, take the following precautions:

1) Handle CCD in a clean environment such as a cleaned booth.
(The cleanliness level should be, if possible, class 1000 at least.)
2) Do not touch the glass surface with fingers. If dust or contamination gets on the glass surface, the following cleaning method is recommended:
* Dust from static electricity should be blown off with an ionized air blower. For anti-electrostatic measures, however, ground all the leads on the device before blowing off the dust.
* The contamination on the glass surface should be wiped off with a clean applicator soaked in Isopropyl alcohol. Wipe slowly and gently in one direction only.
••• Frequently replace the application and do not use the same applicator to clean more than one device.

Note: In most cases, dust and contamination are unavoidable, even before the device is first used. It is, therefore, recommended that the above procedures should be taken to wipe out dust and contamination before using the device.

10.4 Cautions

1) Soldering should be manually performed within 5 seconds at 350℃ maximum at soldering iron.
2) Avoid using or storing the CCD at high temperature or high humidity as it is a precision optical component. Do not give a mechanical shock to the CCD.
3) Do not connect the device to or disconnect it from the plug socket while power is being applied.
4) The exit pupil position of lens should be more than 20mm from top surface of CCD.

11 PACKAGE OUTLINE AND PACKING SPECIFICATION

1. Package Outline Specification

Refer to drawing No. GDG016L-12E2.

(The seal resin stick out from the package shall be passed. And, the seal resins are two kinds of colors, white and transparency.)

2. Markings

Marking contents

(1) Product name : LZ2316J1

(2) Campany name : SHARP

(3) Country of origin : JAPAN

(4) Date code : YY WW X XX

- XX — Denotes the production ref. code. (1~2 figures)
- X — Denotes the production day of the week.

1	2	3	4	5	6	7
SUN.	MON.	TUE.	WED.	THU.	FRI.	SAT.

- WW — Denotes the production week. (01, 02, 03, ·····, 52, 53)
- YY — Denotes the production year. (Lower two digits of the year.)

(5) Over flow drain voltage : EE — Denotes the corresponding code of over flow drain voltage.

Positions of markings are shown in the package outline drawing(No. GDG016L-12E2). But, markings shown in that drawing are not provided any measurements of their characters and their positions.

3. Packing Specification

3-1. Packing materiales

Material Name	Material Spec.	Purpose
Device case	Paper (100devices/case)	Device packing (2trays/case)
Device tray	Conductive plastic (50devices/tray)	Device fixing
Cover tray	Conductive plastic (1tray/case)	Device covering
Buffer	Cardboard (1sheet/case)	Shock absorber of device tray
Plastic film bag	Plastic film	Device tray fixing
Air cushion	Plastic film	Shock absorber of device case
Tape	Plastic film	Sealing Plastic film bag

3-2. External appearance of packing

Refer to drawing No. KSEC-100T2-0.

4. Precaution

1) Before unpacking, confirm the imports of the chapter "Handling Precaution" in this device specifications.

2) Unpacking should be done on the stand treated with anti-ESD. At that time, the same anti-ESD treatment should be done to operater's body, too.

3) Printer's ink of over flow drain voltage isn't solvent-proof, so it is possible to be defaced by using a solvent.

ISSUE DATE	'96. 05. 30	M. Konishi	Y. Takeuchi	T. Aoki	(NOTE)
ISSUE NUMBER	65306ADC				
S/C NUMBER	LZ2316J1				

5. Corresponding code of over flow drain voltage

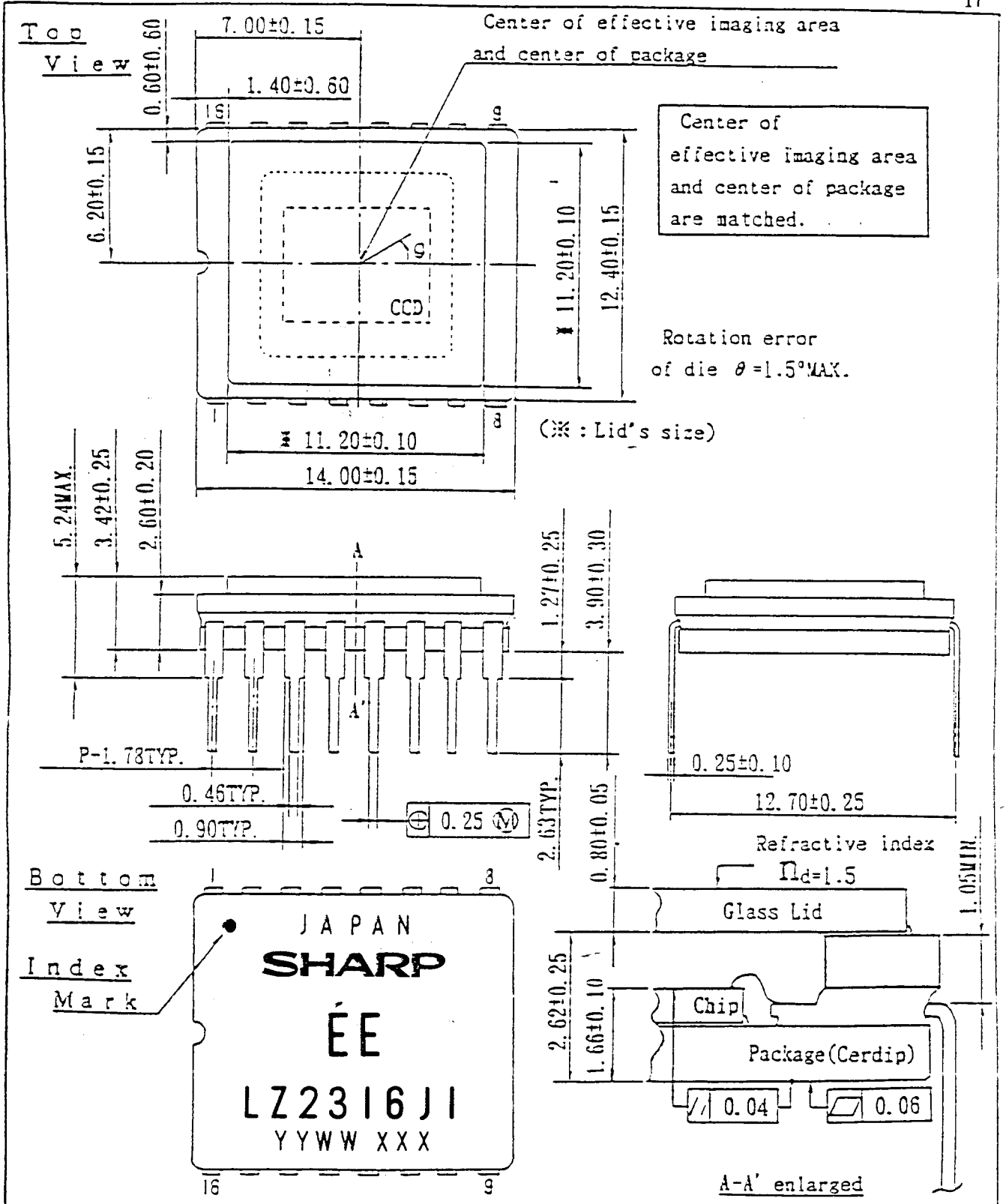
Contents of the corresponding code

Numerical value of over flow drain voltage (V) (Down to one decimal place)		Corresponding code of over flow drain voltage (English alphabet and numeral of two figures)	
Integral value	3.	One figure	3
	4.		4
	5.		5
	6.		6
	7.		7
	8.		8
	9.		9
	10.		A
	11.		B
	12.		C
	13.		D
	14.		E
	15.		F
	16.		G
	17.		H
	18.		J
	19.		K
	20.		L
Decimal value	.0	Two figures	0
	.1		1
	.2		2
	.3		3
	.4		4
	.5		5
	.6		6
	.7		7
	.8		8
	.9		9

Example of the corresponding code

Numerical value of voltage : 9.5(V) → Corresponding code of voltage : 95

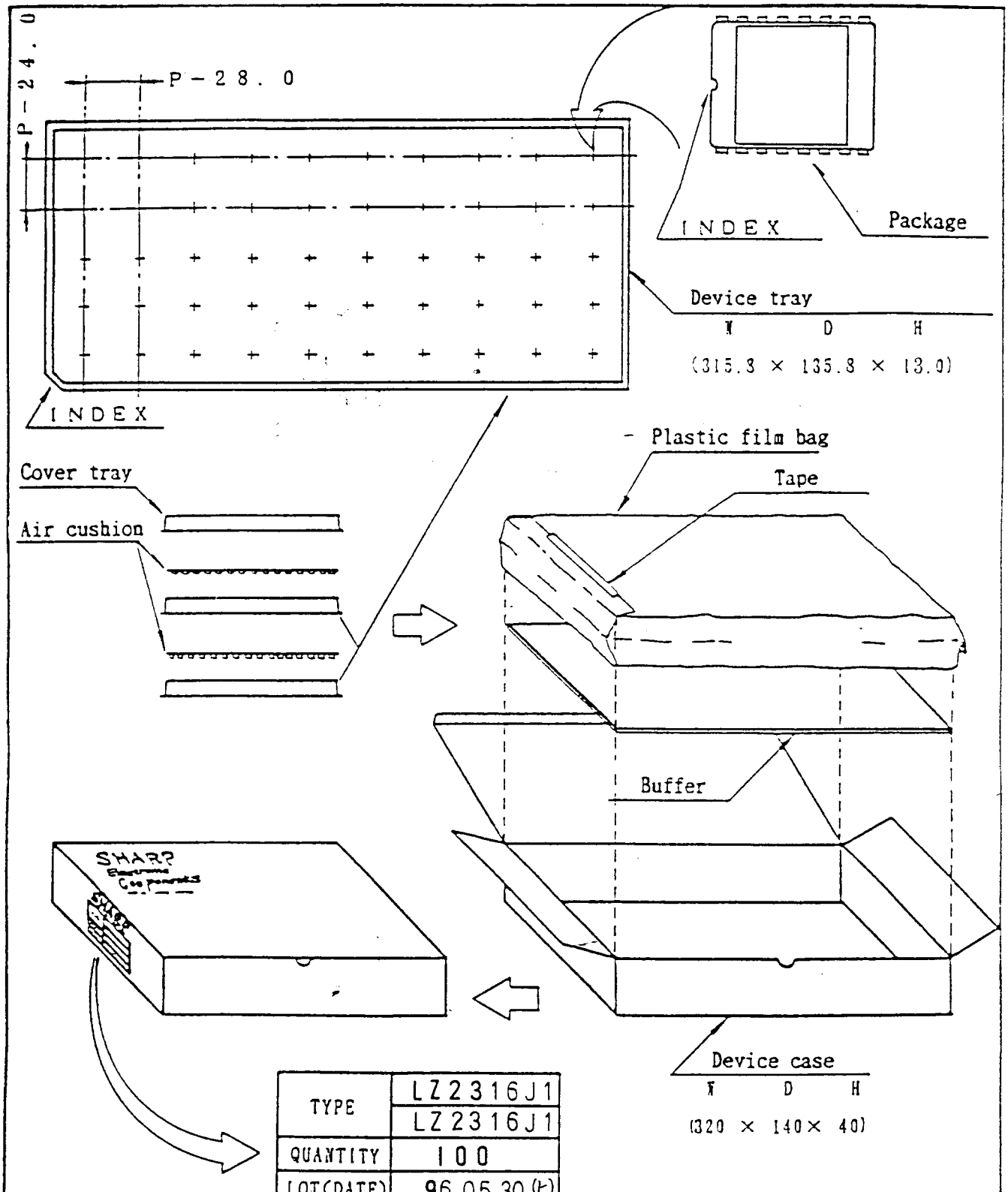
14.3(V) → E3



(Unit : mm)

EE : Corresponding code of over flow drain voltage

MATERIAL	FINISH	NAME	DMPG16C
		CODE	
IC GROUP			
ASSEMBLY ENGINEERING DEPT.		DRAWING No.	GDG016L-12E2
SHARP CORPORATION			



TYPE	LZ2316J1
	LZ2316J1
QUANTITY	100
LOT(DATE)	96.05.30 (土)

尺度 SCALE	単位 UNIT	改訂日 DATE	改訂記事 REVISE / 担当 CHARGE
1/			
材質 MATERIAL	仕上 FINISH	名称 NAME	External Appearance of Packing
		コード CODE	
ワールド株式会社 (IC) GROUP			
ASSEMBLY ENGINEERING DEPT.		図番 DRAWING No.	KSEC-100T2-0
SHARP CORPORATION			