SHARP

SPEC No.	CC057003B
ISSUE:	Nov 18 1993

To ;

PRELIMINARY

SPECIFICATIONS

Product Type 1/3 type solid state color imaging device for NTSC system

Model No. LZ2313H5
(LZ2313H5)

※This specifications contains 18 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED

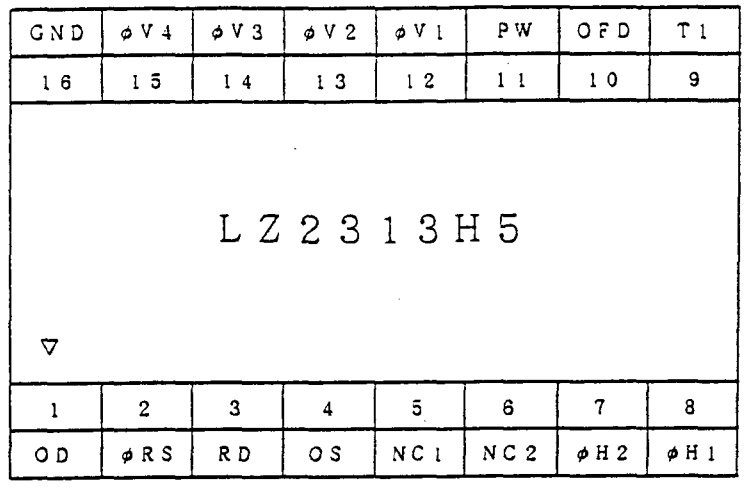
BY: K. Misawa
K. MISAWA
Dept. General Manager

REVIEWED BY:

PREPARED BY: I. Baba

Development Dept. 4
VLSI Laboratories
Integrated Circuits Group
SHARP CORPORATION

3. PIN ASSIGNMENT AND PIN IDENTIFICATION



Symbol	Pin name
RD	Reset transistor drain
OD	Output transistor drain
OS	Video output
φRS	Reset transistor gate clock
φV1, φV2, φV3, φV4	Vertical shift register gate clock
φH1, φH2	Horizontal shift register gate clock
OFD	Overflow drain
PW	P type well
GND	Ground
T1	Test terminals
NC1, NC2	Non-connection (note 1)

(note 1)Connect each pin to GND directly or through a capacitor larger than 0.047μF.

4. ABSOLUTE MAXIMUM RATING

(Ta = 25℃)

Item	Symbol	Rating	Unit
Output transistor drain voltage	VOD	0 to +18	V
Reset transistor drain voltage	VRD	0 to +18	V
Overflow drain voltage	VOFD	0 to +55	V
Test terminal, T1	VT1	0 to +18	V
Reset gate clock voltage	VφRS	-0.3 to +18	V
Vertical shift register clock voltage	VφV	-9.0 to +18	V
Horizontal shift register clock voltage	VφH	-0.3 to +18	V
PW and vertical clock voltage difference	VPW-VφV	- 27 to 0	V
Storage temperature	Tstg	- 40 to +80	℃
Operating ambient temperature	Topr	- 20 to +70	℃

5. RECOMMENDED OPERATING CONDITIONS

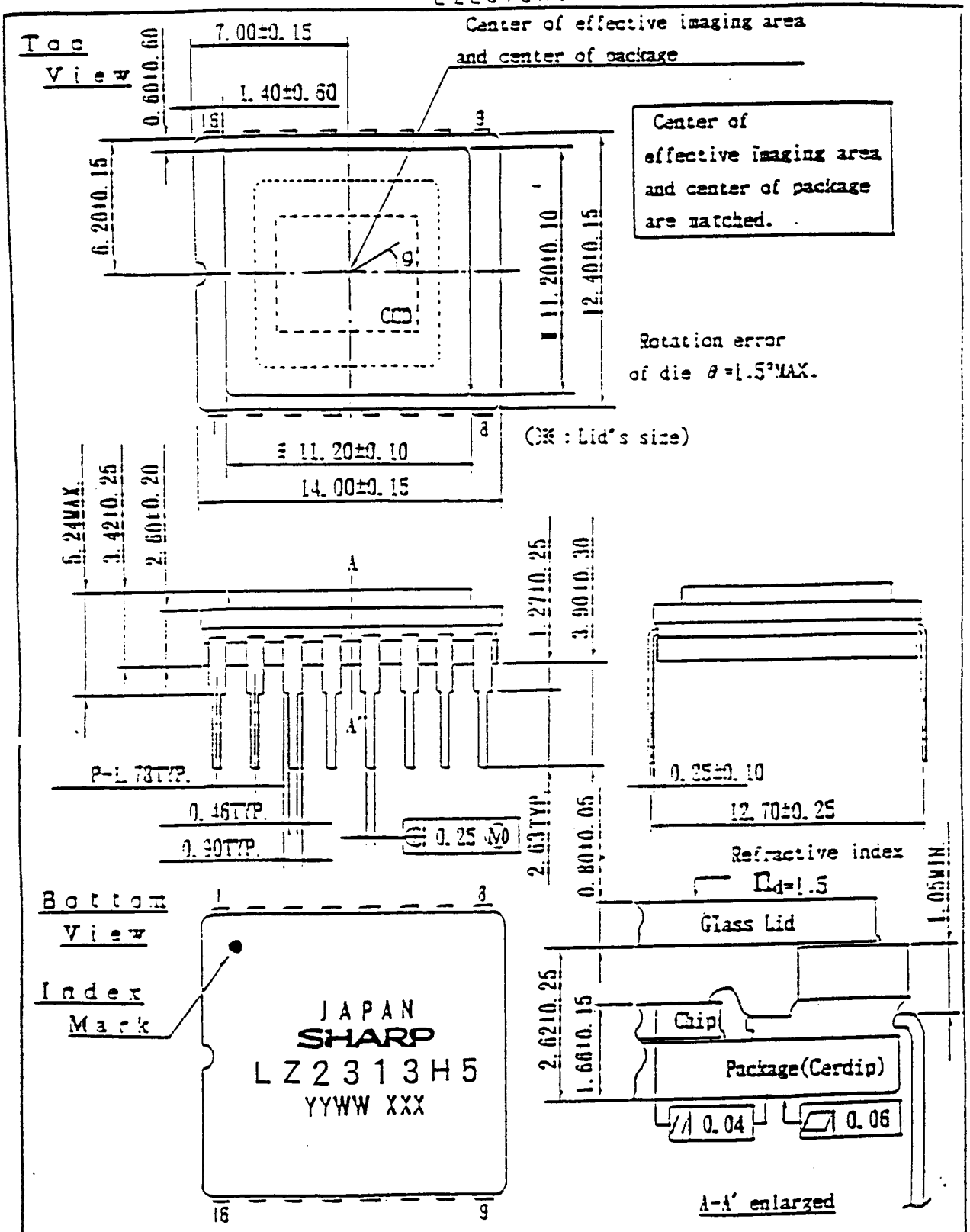
Item		Symbol	Minimum	Typical	Maximum	Unit
Operating ambient tempetarure		Topr		25.0		℃
Output transistor drain voltage		VOD	14.5	15.0	16.0	V
Reset transistor drain voltage		VRD		VOD		V
Overflow drain voltage	When DC is applied(note1)	VOFD	5.0	(adj.)	19.0	V
	When pulse is applied p-p level (note2)	VφOFD	22.0			V
Ground		GND		0.0		V
P-well voltage		VPW	-9.0		VφVL	V
Test terminal, T1		VT1		VOD		V
Vertical shift register clock	LOW level	VφV1L, VφV2L VφV3L, VφV4L	-8.5	-8.0	-7.5	V
	INTERMEDIATE level	VφV1I, VφV2I VφV3I, VφV4I		0.0		V
	HIGH level	VφV1H, VφV3H	16.0	16.5	17.0	V
Horizontal shift register clock	LOW level	VφH1L, VφH2L	-0.05	0.0	0.05	V
	HIGH level	VφH1H, VφH2H	4.7	5.0	6.0	V
Reset gate clock	LOW level	VφRSL	0.0		VRD-13.0	V
	HIGH level	VφRSH	VRD-8.5		9.5	V
Frequency						
Vertical shift register clock		fφV1, fφV2 fφV3, fφV4		15.73		kHz
Horizontal shift register clock		fφH1, fφH2		9.53		MHz
Reset gate clock		fφRS		9.53		MHz

(note1) When DC voltage is applied, shutter speed is 1/60 seconds.
(note2) When pulse is applied, shutter speed is less than 1/60 seconds.

6. CHARACTERISTICS

No.	Item	Symbol	Note	Min.	Typ.	Max.	Unit
1	Photo response non-uniformity	PRNU	(a)			15	%
2	Carrier saturation	Vsat	(b)	450			mV
3	Dark output voltage	Vdark	(c)		0.3	3.0	mV
4	Dark signal non-uniformity	DSNU	(d)		0.6	2.0	mV
5	Sensitivity	R	(e)	440	600		mV
6	Smear ratio	SMR	(f)		0.009	0.016	%
7	Image lag	AI	(g)			1.0	%
8	Blooming suppression ratio	ABL	(h)	100			
9	Current dissipation	I_{OD}			4.0	8.0	mA
10	Output impedance	Ro			350		Ω
11	Vector breakup		(i)			5.0	°, %
12	Line crawling		(j)			3.0	%
13	Luminance flicker		(k)			2.0	%

LZ2313H5



(Unit : mm)

MATERIAL	FINISH	NAME	DMPG16C
IC GROUP		CODE	
(VLSI) DEVELOPMENT DEPT.5	14		

CCD sensor imaging area sensor pattern recognition LZ2 timing generator vertical driver white balance