SHARP

TO: _____

REFERENCE

DEVICE SPECIFICATION FOR

1/2-inch type solid state color imaging device

for NTSC system

MODEL NO.

L Z 2 1 1 3 Y

SPEC. NO.: EL035011A

ISSUE: JUN. 25, 1991

CUSTOMER'S APPROVAL

DATE: _____

BY: _____

PRESENTED BY: S. Naka

S. NAKA

Dept. Manager

APPROVED BY: K. Misawa

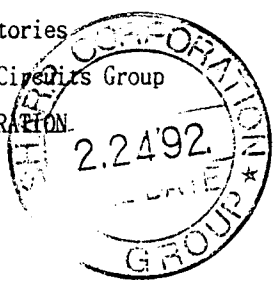
PREPARED BY: E. Kojima

Development Dept. 4

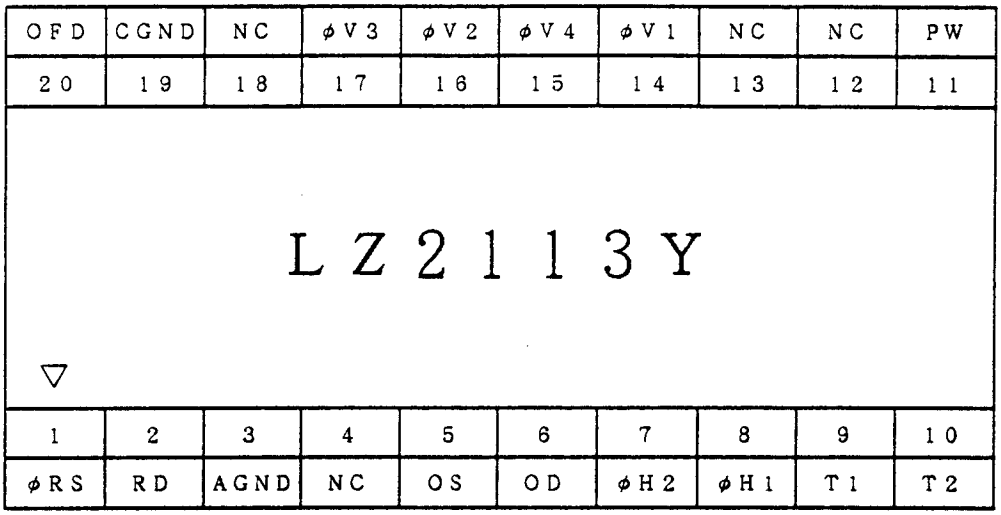
VLSI Laboratories

Integrated Circuits Group

SHARP CORPORATION



3. PIN ASSIGNMENT AND PIN IDENTIFICATION



Symbol	Pin name
RD	Reset transistor drain
OD	Output transistor drain
OS	Video output
φRS	Reset transistor gate clock
φV1, φV2, φV3, φV4	Vertical shift register gate clock
φH1, φH2	Horizontal shift register gate clock
OFD	Overflow drain
PW	P type well
AGND	Analog part ground
CGND	Clock part ground
T1, T2	Test terminals
NC	Non-connection

4. ABSOLUTE MAXIMUM RATING

(Ta = 25℃)

Item	Symbol	Rating	Unit
Output transistor drain voltage	VOD	0 to +18	V
Reset transistor drain voltage	VRD	0 to +18	V
Overflow drain voltage	VOFD	0 to +55	V
Test terminal, T1	VT1	-0.3 to +18	V
Test terminal, T2	VT2	0 to +18	V
Reset gate clock voltage	VφRS	-0.3 to +18	V
Vertical shift register clock voltage	VφV	- 10 to +18	V
Horizontal shift register clock voltage	VφH	-0.3 to +18	V
PW and vertical clock voltage difference	VPW-VφV	- 26 to 0	V
Storage temperature	Tstg	- 20 to +80	℃
Operating ambient temperature	Topr	- 20 to +70	℃

5. RECOMMENDED OPERATING CONDITIONS

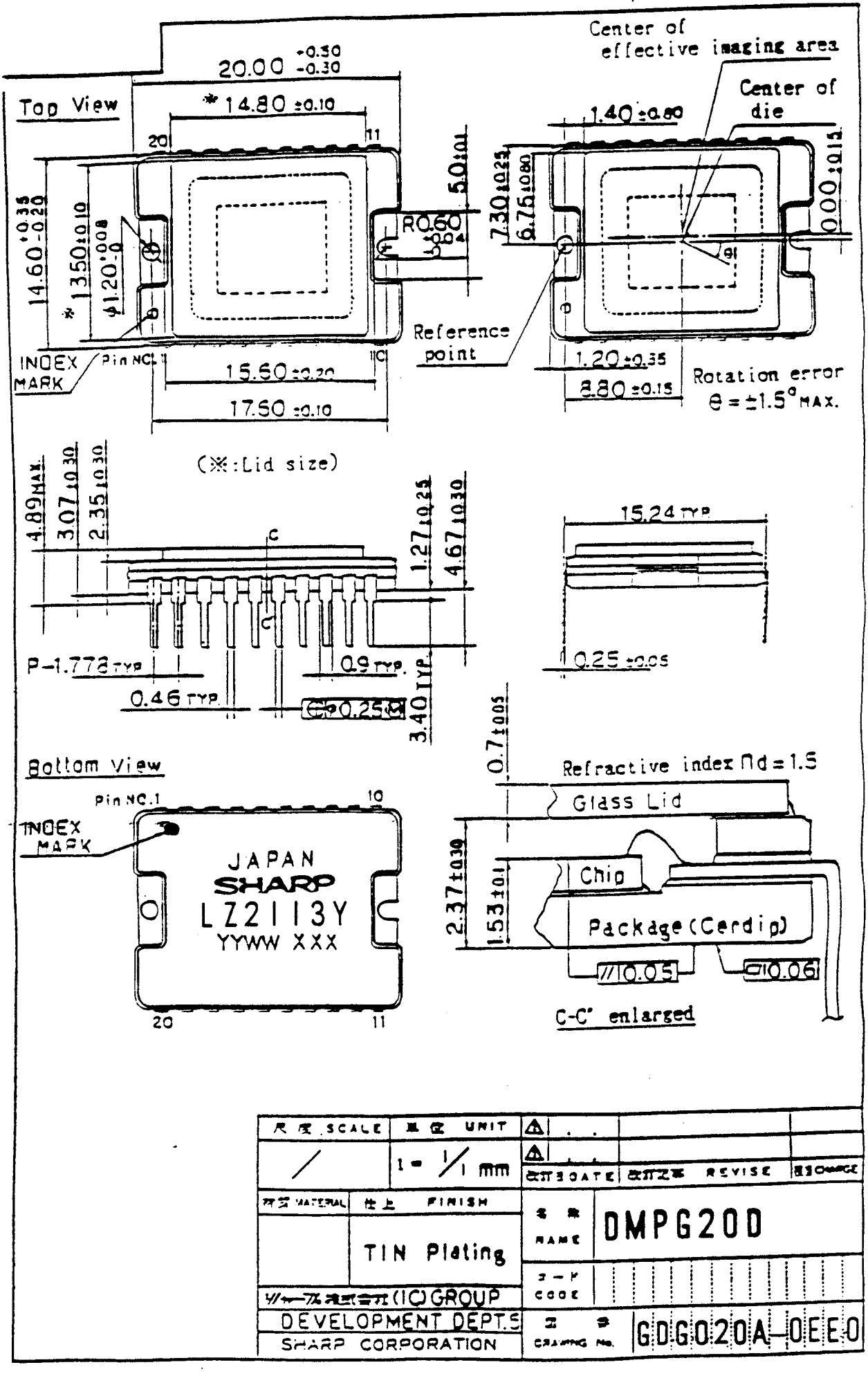
Item		Symbol	Minimum	Typical	Maximum	Unit
Operating ambient tempetarure		Topr		25.0		℃
Output transistor drain voltage		VOD	14.5	15.0	16.0	V
Reset transistor drain voltage		VRD		VOD		V
Overflow drain voltage	When DC is applied(note1)	VOFD	5.0	(adj.)	19.0	V
	When pulse is applied p-p level (note2)	VφOFD	22.0			V
Analog part ground		AGND	-	0.0	-	V
Clock part ground		CGND	-	0.0	-	V
P-well voltage		VPW	-9.5		VφVL	V
Test terminal, T1		VT1	-	0.0	-	V
Test terminal, T2		VT2	-	VOD	-	V
Vertical shift register clock	LOW level	VφV1L, VφV2L VφV3L, VφV4L	-9.5	-9.0	-8.5	V
	INTERMEDIATE level	VφV1I, VφV2I VφV3I, VφV4I		0.0		V
	HIGH level	VφV1H, VφV3H	14.5	15.0	15.5	V
Horizontal shift register clock	LOW level	VφH1L, VφH2L	-0.05	0.0	0.05	V
	HIGH level	VφH1H, VφH2H	4.7	5.0	6.0	V
Reset gate clock	LOW level	VφRSL	-0.1	0.0	0.1	V
	HIGH level	VφRSH	8.0	9.0	10.0	V
Frequency						
Vertical shift register clock		fφV1, fφV2 fφV3, fφV4		15.73		KHz
Horizontal shift register clock		fφH1, fφH2		9.53		MHz
Reset gate clock		fφRS		9.53		MHz

(note1) When DC voltage is applied, shutter speed is 1/60 seconds.

(note2) When pulse is applied, shutter speed is less than 1/60 seconds.

6. CHARACTERISTICS

No.	Item	Symbol	Note	Min.	Typ.	Max.	Unit
1	Photo response non-uniformity	PRNU	(a)			10	%
2	Carrier saturation	Vsat	(b)	450			mV
3	Dark output voltage	Vdark	(c)		0.3	3.0	mV
4	Dark signal non-uniformity	DSNU	(d)		0.6	2.0	mV
5	Sensitivity	R	(e)	400	520		mV
6	Gamma	γ			1		
7	Smear ratio	SMR	(f)		0.005	0.016	%
8	Image lag	AI	(g)			1.0	%
9	Blooming suppression ratio	ABL	(h)	1000			
10	Current dissipation	I_{OD}			4.0	8.0	mA
11	Output impedance	Ro			300		Ω
12	Dark noise	Vnoise	(i)		0.2	0.3	mV
13	OB difference in level		(j)			1.0	mV
14	Vector breakup		(k)			5.0	°, %
15	Line crawling		(l)			3.0	%
16	Luminance flicker		(m)			2.0	%



尺度 SCALE	単位 UNIT		
/	1 = 1/1 mm	改訂日 DATE	改訂文書 REVISE / 担当 CHARGE
材質 MATERIAL	仕上 FINISH	名称 NAME	DMPG20D
	TIN Plating	コード CODE	
ソャープ株式会社 (IC) GROUP			
DEVELOPMENT DEPT.5		図番 DRAWING No.	GDG020A-0EE0
SHARP CORPORATION			

CCD sensor imaging area sensor pattern recognition timing generator vertical driver white balance