

24-Bit μ Power $\Delta\Sigma$ ADC with Differential Input and Differential Reference

FEATURES

- 24-Bit ADC in Narrow SSOP-16 Package (SO-8 Footprint)
- 2ppm INL, No Missing Codes
- 2.5ppm Full-Scale Error
- 0.1ppm Offset
- 0.16ppm Noise
- Internal Oscillator—No External Components Required
- 110dB Min, 50Hz/60Hz Notch Filter
- Single Conversion Settling Time for Multiplexed Applications
- Differential Inputs with GND to V_{CC} Common Mode Range
- Single Supply 2.7V to 5.5V Operation
- Low Supply Current (200 μ A) and Auto Shutdown
- Fully Differential Version of LTC2400

APPLICATIONS

- Direct Sensor Digitizer
- Weight Scales
- Direct Temperature Measurement
- Gas Analyzers
- Strain-Gage Transducers
- Instrumentation
- Data Acquisition
- Industrial Process Control
- 6-Digit DVMs

DESCRIPTION

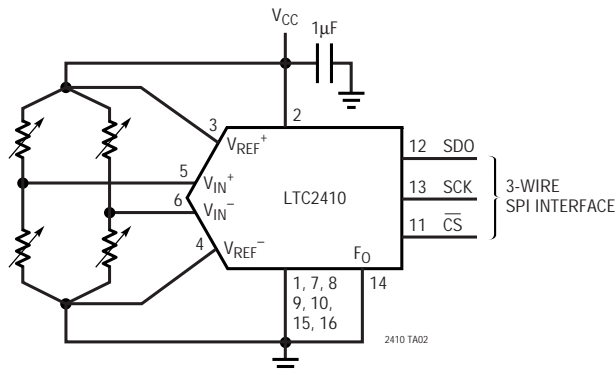
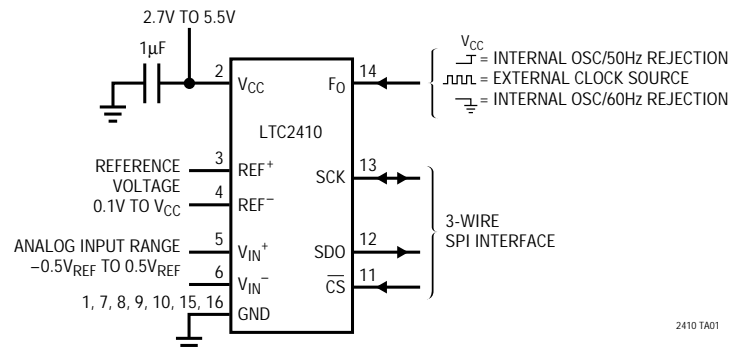
The LTC[®]2410 is a 2.7V to 5.5V micropower 24-bit converter with an integrated oscillator, 2ppm INL and 0.16ppm RMS noise. It uses delta-sigma technology and provides single cycle settling time for multiplexed applications. Through a single pin the LTC2410 can be configured for better than 110dB input differential mode rejection at 50Hz or 60Hz \pm 2%, or it can be driven by an external oscillator for a user defined rejection frequency. The internal oscillator requires no external frequency setting components.

The converter accepts any external differential reference voltage from 0.1V to V_{CC} for flexible ratiometric and remote sensing measurement configurations. The full-scale differential input range is from $-0.5V_{REF}$ to $0.5V_{REF}$. The DC common mode input rejection is better than 140dB.

The LTC2410 communicates through a flexible 3-wire digital interface which is compatible with SPI and MICROWIRE[™] protocols.

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MICROWIRE is a trademark of National Semiconductor Corporation.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND -0.3V to 7V

Analog Input Pins Voltage

to GND -0.3V to ($V_{CC} + 0.3V$)

Reference Input Pins Voltage

to GND -0.3V to ($V_{CC} + 0.3V$)Digital Input Voltage to GND -0.3V to ($V_{CC} + 0.3V$)Digital Output Voltage to GND -0.3V to ($V_{CC} + 0.3V$)

Operating Temperature Range

LTC2410C 0°C to 70°C

LTC2410I -40°C to 85°C

Storage Temperature Range -65°C to 150°C

Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

| TOP VIEW | | ORDER PART NUMBER |
|---|----|-------------------|
| | 16 | GND |
| | 15 | GND |
| | 14 | CS |
| | 13 | SDO |
| | 12 | SCK |
| | 11 | FO |
| | 10 | GND |
| | 9 | GND |
| GN PACKAGE 16-LEAD PLASTIC SSOP NARROW | | GN PART MARKING |
| $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 95^{\circ}\text{C/W}$ | | ???? |

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. (Notes 3, 4)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|--|-----|---------|-----|--------------------------------------|
| Resolution (No Missing Codes) | $0.1V \leq V_{REF+} - V_{REF-} \leq V_{CC}$, $-0.5 \cdot (V_{REF+} - V_{REF-}) \leq V_{IN+} - V_{IN-} \leq 0.5 \cdot (V_{REF+} - V_{REF-})$, (Note 5) | ● | 24 | | Bits |
| Integral Nonlinearity | $V_{REF+} = 2.5V$, $V_{REF-} = \text{GND}$, the Reference Common Mode Voltage and Input Common Mode Voltage May Be Independently Set Anywhere within the GND to V_{CC} Range, $V_{IN+} + V_{IN-} = 2.5V$, (Note 6) | ● | 1 | 10 | ppm of V_{REF} |
| | $5V \leq V_{CC} \leq 5.5V$, $V_{REF+} = 5V$, $V_{REF-} = \text{GND}$, $V_{IN+} + V_{IN-} = 5V$, (Note 6) | ● | 2 | 15 | ppm of V_{REF} |
| Offset Error | $2.5V \leq V_{REF+} \leq V_{CC}$, $V_{REF-} = \text{GND}$, $\text{GND} \leq V_{IN+} = V_{IN-} \leq V_{CC}$ | ● | 0.1 | 2 | ppm of V_{REF} |
| Offset Error Drift | $2.5V \leq V_{REF+} \leq V_{CC}$, $V_{REF-} = \text{GND}$, $\text{GND} \leq V_{IN+} = V_{IN-} \leq V_{CC}$ | | 0.01 | | ppm of $V_{REF}/^{\circ}\text{C}$ |
| Positive Full-Scale Error | $2.5V \leq V_{REF+} \leq V_{CC}$, $V_{REF-} = \text{GND}$, $V_{IN+} = 0.75V_{REF+}$, $V_{IN-} = 0.25 \cdot V_{REF+}$ | ● | 2.5 | | ppm of V_{REF} |
| Positive Full-Scale Error Drift | $2.5V \leq V_{REF+} \leq V_{CC}$, $V_{REF-} = \text{GND}$, $V_{IN+} = 0.75V_{REF+}$, $V_{IN-} = 0.25 \cdot V_{REF+}$ | | 0.04 | | ppm of $V_{REF}/^{\circ}\text{C}$ |
| Negative Full-Scale Error | $2.5V \leq V_{REF+} \leq V_{CC}$, $V_{REF-} = \text{GND}$, $V_{IN+} = 0.25 \cdot V_{REF+}$, $V_{IN-} = 0.75 \cdot V_{REF+}$ | ● | 2.5 | | ppm of V_{REF} |
| Negative Full-Scale Error Drift | $2.5V \leq V_{REF+} \leq V_{CC}$, $V_{REF-} = \text{GND}$, $V_{IN+} = 0.25 \cdot V_{REF+}$, $V_{IN-} = 0.75 \cdot V_{REF+}$ | | 0.04 | | ppm of $V_{REF}/^{\circ}\text{C}$ |
| Total Unadjusted Error | $V_{REF+} = 2.5V$, $V_{REF-} = \text{GND}$, $V_{IN+} + V_{IN-} = 2.5V$ $5V \leq V_{CC} \leq 5.5V$, $V_{REF+} = 5V$, $V_{REF-} = \text{GND}$, $V_{IN+} + V_{IN-} = 5V$ | | 5 10 | | ppm of V_{REF} ppm of V_{REF} |
| Output Noise | $5V \leq V_{CC} \leq 5.5V$, $V_{REF+} = 5V$, $V_{REF-} = \text{GND}$, $\text{GND} \leq V_{IN+} = V_{IN-} \leq 5V$, (Note 13) | | 0.8 | | μV_{RMS} |

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Notes 3, 4)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|-----|-----|-----|-------|
| Input Common Mode Rejection DC | $2.5\text{V} \leq V_{\text{REF}+} \leq V_{\text{CC}}$, $V_{\text{REF}-} = \text{GND}$, $\text{GND} \leq V_{\text{IN}-} = V_{\text{IN}+} \leq 5\text{V}$ | ● | 130 | 140 | | dB |
| Input Common Mode Rejection $60\text{Hz} \pm 2\%$ | $2.5\text{V} \leq V_{\text{REF}+} \leq V_{\text{CC}}$, $V_{\text{REF}-} = \text{GND}$, $\text{GND} \leq V_{\text{IN}-} = V_{\text{IN}+} \leq 5\text{V}$, (Note 7) | ● | 140 | | | dB |
| Input Common Mode Rejection $50\text{Hz} \pm 2\%$ | $2.5\text{V} \leq V_{\text{REF}+} \leq V_{\text{CC}}$, $V_{\text{REF}-} = \text{GND}$, $\text{GND} \leq V_{\text{IN}-} = V_{\text{IN}+} \leq 5\text{V}$, (Note 8) | ● | 140 | | | dB |
| Input Normal Mode Rejection $60\text{Hz} \pm 2\%$ | (Note 7) | ● | 110 | 140 | | dB |
| Input Normal Mode Rejection $50\text{Hz} \pm 2\%$ | (Note 8) | ● | 110 | 140 | | dB |
| Reference Common Mode Rejection DC | $2.5\text{V} \leq V_{\text{REF}+} \leq V_{\text{CC}}$, $\text{GND} \leq V_{\text{REF}-} \leq 2.5\text{V}$, $V_{\text{REF}+} - V_{\text{REF}-} = 2.5\text{V}$, $V_{\text{IN}-} = V_{\text{IN}+} = \text{GND}$ | ● | 130 | 140 | | dB |
| Power Supply Rejection, DC | $V_{\text{REF}+} = 2.5\text{V}$, $V_{\text{REF}-} = \text{GND}$, $V_{\text{IN}-} = V_{\text{IN}+} = \text{GND}$ | | | 100 | | dB |
| Power Supply Rejection, $60\text{Hz} \pm 2\%$ | $V_{\text{REF}+} = 2.5\text{V}$, $V_{\text{REF}-} = \text{GND}$, $V_{\text{IN}-} = V_{\text{IN}+} = \text{GND}$, (Note 7) | | | 110 | | dB |
| Power Supply Rejection, $50\text{Hz} \pm 2\%$ | $V_{\text{REF}+} = 2.5\text{V}$, $V_{\text{REF}-} = \text{GND}$, $V_{\text{IN}-} = V_{\text{IN}+} = \text{GND}$, (Note 8) | | | 110 | | dB |

ANALOG INPUT AND REFERENCE

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 3)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|--|--|---|----------------------------|-----|-------------------------------|-------|
| $V_{\text{IN}+}$ | Absolute/Common Mode $V_{\text{IN}+}$ Voltage | | ● | $\text{GND} - 0.3\text{V}$ | | $V_{\text{CC}} + 0.3\text{V}$ | V |
| $V_{\text{IN}-}$ | Absolute/Common Mode $V_{\text{IN}-}$ Voltage | | ● | $\text{GND} - 0.3\text{V}$ | | $V_{\text{CC}} + 0.3\text{V}$ | V |
| V_{IN} | Input Differential Voltage Range ($V_{\text{IN}+} - V_{\text{IN}-}$) | | ● | $-V_{\text{REF}}/2$ | | $V_{\text{REF}}/2$ | V |
| $V_{\text{REF}+}$ | Absolute/Common Mode $V_{\text{REF}+}$ Voltage | | ● | 0.1 | | V_{CC} | V |
| $V_{\text{REF}-}$ | Absolute/Common Mode $V_{\text{REF}-}$ Voltage | | ● | GND | | $V_{\text{CC}} - 0.1\text{V}$ | V |
| V_{REF} | Reference Differential Voltage Range ($V_{\text{REF}+} - V_{\text{REF}-}$) | | ● | 0.1 | | V_{CC} | V |
| $C_S (V_{\text{IN}+})$ | $V_{\text{IN}+}$ Sampling Capacitance | | | | 18 | | pF |
| $C_S (V_{\text{IN}-})$ | $V_{\text{IN}-}$ Sampling Capacitance | | | | 18 | | pF |
| $C_S (V_{\text{REF}+})$ | $V_{\text{REF}+}$ Sampling Capacitance | | | | 18 | | pF |
| $C_S (V_{\text{REF}-})$ | $V_{\text{REF}-}$ Sampling Capacitance | | | | 18 | | pF |
| $I_{\text{DC_LEAK}} (V_{\text{IN}+})$ | $V_{\text{IN}+}$ DC Leakage Current | $\overline{CS} = V_{\text{CC}}$, $V_{\text{IN}+} = \text{GND}$ | ● | -10 | 1 | 10 | nA |
| $I_{\text{DC_LEAK}} (V_{\text{IN}-})$ | $V_{\text{IN}-}$ DC Leakage Current | $\overline{CS} = V_{\text{CC}}$, $V_{\text{IN}-} = \text{GND}$ | ● | -10 | 1 | 10 | nA |
| $I_{\text{DC_LEAK}} (V_{\text{REF}+})$ | $V_{\text{REF}+}$ DC Leakage Current | $\overline{CS} = V_{\text{CC}}$, $V_{\text{REF}+} = 5\text{V}$ | ● | -10 | 1 | 10 | nA |
| $I_{\text{DC_LEAK}} (V_{\text{REF}-})$ | $V_{\text{REF}-}$ DC Leakage Current | $\overline{CS} = V_{\text{CC}}$, $V_{\text{REF}-} = \text{GND}$ | ● | -10 | 1 | 10 | nA |

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 3)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|----------|--|---------------------------------------|---|-----------------|-----|------|---------------|
| V_{IH} | High Level Input Voltage \overline{CS} , F_0 | $2.7V \leq V_{CC} \leq 5.5V$ | ● | 2.5 | | | V |
| | | $2.7V \leq V_{CC} \leq 3.3V$ | | 2.0 | | | V |
| V_{IL} | Low Level Input Voltage \overline{CS} , F_0 | $4.5V \leq V_{CC} \leq 5.5V$ | ● | | | 0.8 | V |
| | | $2.7V \leq V_{CC} \leq 5.5V$ | | | | 0.6 | V |
| V_{IH} | High Level Input Voltage SCK | $2.7V \leq V_{CC} \leq 5.5V$ (Note 9) | ● | 2.5 | | | V |
| | | $2.7V \leq V_{CC} \leq 3.3V$ (Note 9) | | 2.0 | | | V |
| V_{IL} | Low Level Input Voltage SCK | $4.5V \leq V_{CC} \leq 5.5V$ (Note 9) | ● | | | 0.8 | V |
| | | $2.7V \leq V_{CC} \leq 5.5V$ (Note 9) | | | | 0.6 | V |
| I_{IN} | Digital Input Current \overline{CS} , F_0 | $0V \leq V_{IN} \leq V_{CC}$ | ● | -10 | | 10 | μA |
| I_{IN} | Digital Input Current SCK | $0V \leq V_{IN} \leq V_{CC}$ (Note 9) | ● | -10 | | 10 | μA |
| C_{IN} | Digital Input Capacitance \overline{CS} , F_0 | | | | 10 | | pF |
| C_{IN} | Digital Input Capacitance SCK | (Note 9) | | | 10 | | pF |
| V_{OH} | High Level Output Voltage SDO | $I_O = -800\mu\text{A}$ | ● | $V_{CC} - 0.5V$ | | | V |
| V_{OL} | Low Level Output Voltage SDO | $I_O = 1.6\text{mA}$ | ● | | | 0.4V | V |
| V_{OH} | High Level Output Voltage SCK | $I_O = -800\mu\text{A}$ (Note 10) | ● | $V_{CC} - 0.5V$ | | | V |
| V_{OL} | Low Level Output Voltage SCK | $I_O = 1.6\text{mA}$ (Note 10) | ● | | | 0.4V | V |
| I_{OZ} | High-Z Output Leakage SDO | | ● | -10 | | 10 | μA |

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 3)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|----------|-----------------|------------------------------------|---|-----|-----|-----|---------------|
| V_{CC} | Supply Voltage | | ● | 2.7 | | 5.5 | V |
| I_{CC} | Supply Current | | | | | | |
| | Conversion Mode | $\overline{CS} = 0V$ (Note 12) | ● | | 200 | 300 | μA |
| | Sleep Mode | $\overline{CS} = V_{CC}$ (Note 12) | ● | | 20 | 30 | μA |

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 3)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------|---|---|-------------|---|-------------------------|----------------|
| f_{EOSC} | External Oscillator Frequency Range | ● | 2.56 | | 2000 | kHz |
| t_{HEO} | External Oscillator High Period | ● | 0.25 | | 390 | μs |
| t_{LEO} | External Oscillator Low Period | ● | 0.25 | | 390 | μs |
| t_{CONV} | Conversion Time | $F_0 = 0\text{V}$ $F_0 = V_{\text{CC}}$ External Oscillator (Note 11) | ● ● ● | 130.66 156.80 20480/ f_{EOSC} (in kHz) | 133.33 160 163.20 | ms ms ms |
| f_{ISCK} | Internal SCK Frequency | Internal Oscillator (Note 10) External Oscillator (Notes 10, 11) | | 19.2 $f_{\text{EOSC}}/8$ | | kHz kHz |
| D_{ISCK} | Internal SCK Duty Cycle | (Note 10) | ● | 45 | 55 | % |
| f_{ESCK} | External SCK Frequency Range | (Note 9) | ● | | 2000 | kHz |
| t_{LESCK} | External SCK Low Period | (Note 9) | ● | 250 | | ns |
| t_{HESCK} | External SCK High Period | (Note 9) | ● | 250 | | ns |
| $t_{\text{DOUT_ISCK}}$ | Internal SCK 32-Bit Data Output Time | Internal Oscillator (Notes 10, 12) External Oscillator (Notes 10, 11) | ● ● | 1.64 256/ f_{EOSC} (in kHz) | 1.67 1.70 | ms ms |
| $t_{\text{DOUT_ESCK}}$ | External SCK 32-Bit Data Output Time | (Note 9) | ● | 32/ f_{ESCK} (in kHz) | | ms |
| t_1 | $\overline{\text{CS}} \downarrow$ to SDO Low Z | | ● | 0 | 150 | ns |
| t_2 | $\overline{\text{CS}} \uparrow$ to SDO High Z | | ● | 0 | 150 | ns |
| t_3 | $\overline{\text{CS}} \downarrow$ to SCK \downarrow | (Note 10) | ● | 0 | 150 | ns |
| t_4 | $\overline{\text{CS}} \downarrow$ to SCK \uparrow | (Note 9) | ● | 50 | | ns |
| t_{KQMAX} | SCK \downarrow to SDO Valid | | ● | | 200 | ns |
| t_{KQMIN} | SDO Hold After SCK \downarrow | (Note 5) | ● | 15 | | ns |
| t_5 | SCK Set-Up Before $\overline{\text{CS}} \downarrow$ | | ● | 50 | | ns |
| t_6 | SCK Hold After $\overline{\text{CS}} \downarrow$ | | ● | | 50 | ns |

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: $V_{\text{CC}} = 2.7$ to 5.5V unless otherwise specified.

Note 4: F_0 pin tied to GND or to V_{CC} or to external conversion clock source with $f_{\text{EOSC}} = 153600\text{Hz}$ unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: $F_0 = 0\text{V}$ (internal oscillator) or $f_{\text{EOSC}} = 153600\text{Hz} \pm 2\%$ (external oscillator).

Note 8: $F_0 = V_{\text{CC}}$ (internal oscillator) or $f_{\text{EOSC}} = 128000\text{Hz} \pm 2\%$ (external oscillator).

Note 9: The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in kHz.

Note 10: The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the SCK pin has a total equivalent load capacitance $C_{\text{LOAD}} = 20\text{pF}$.

Note 11: The external oscillator is connected to the F_0 pin. The external oscillator frequency, f_{EOSC} , is expressed in kHz.

Note 12: The converter uses the internal oscillator.
 $F_0 = 0\text{V}$ or $F_0 = V_{\text{CC}}$.

Note 13: The output noise includes the contribution of the internal calibration operations.

PIN FUNCTIONS

GND (Pins 1, 7, 8, 9, 10, 15, 16): Ground. Multiple ground pins internally connected for optimum ground current flow and V_{CC} decoupling. It is recommended to the user to connect each one of these pins to a ground plane through a low impedance connection.

V_{CC} (Pin 2): Positive Supply Voltage. Bypass to GND (Pin 1) with a 10 μ F tantalum capacitor in parallel with 0.1 μ F ceramic capacitor as close to the part as possible.

V_{REF+} (Pin 3), V_{REF-} (Pin 4): Differential Reference Input. The voltage on these pins can have any value between GND and V_{CC} as long as the reference positive input, V_{REF+} , is maintained more positive than the reference negative input, V_{REF-} , by at least 0.1V.

V_{IN+} (Pin 5), V_{IN-} (Pin 6): Differential Analog Input. The voltage on these pins can have any value between $GND - 0.3V$ and $V_{CC} + 0.3V$. Within these limits the converter bipolar input range ($V_{IN+} - V_{IN-}$) extends from $-0.5 \cdot (V_{REF+} - V_{REF-})$ to $0.5 \cdot (V_{REF+} - V_{REF-})$. Outside this input range the converter produces unique overrange and underrange output codes.

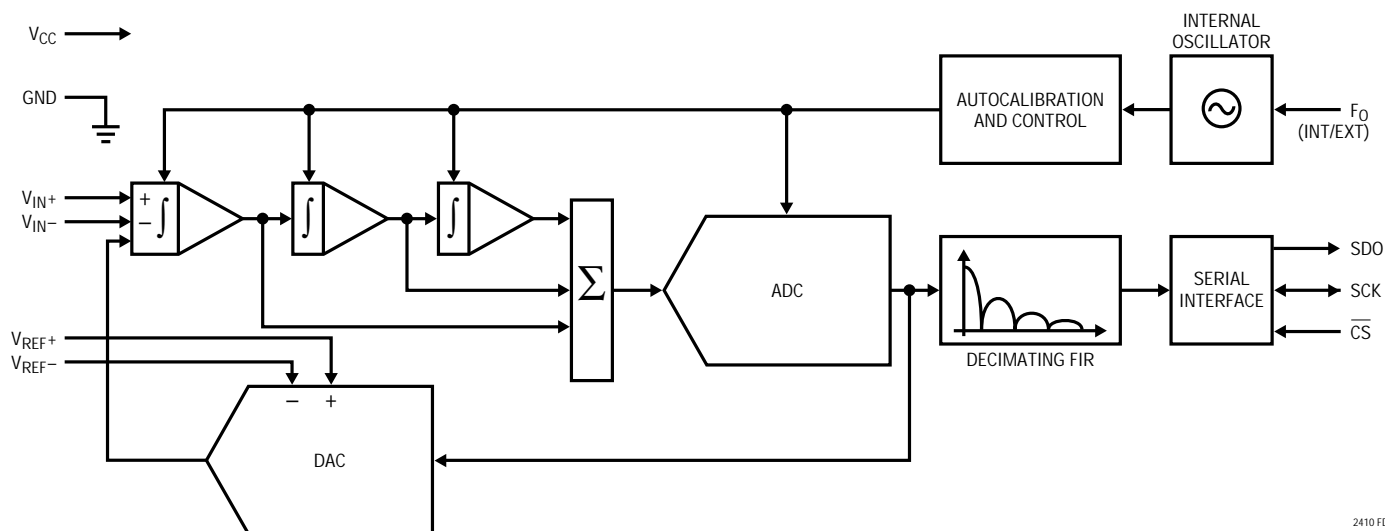
\overline{CS} (Pin 11): Active LOW Digital Input. A LOW on this pin enables the SDO digital output and wakes up the ADC. Following each conversion the ADC automatically enters the Sleep mode and remains in this low power state as long as \overline{CS} is HIGH. A LOW-to-HIGH transition on \overline{CS} during the Data Output transfer aborts the data transfer and starts a new conversion.

SDO (Pin 12): Three-State Digital Output. During the Data Output period this pin is used as serial data output. When the chip select \overline{CS} is HIGH ($\overline{CS} = V_{CC}$) the SDO pin is in a high impedance state. During the Conversion and Sleep periods this pin is used as the conversion status output. The conversion status can be observed by pulling \overline{CS} LOW.

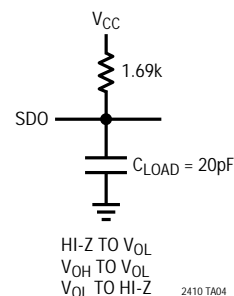
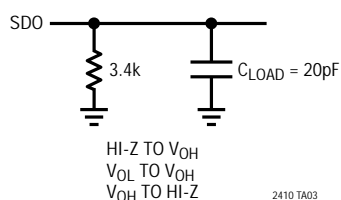
SCK (Pin 13): Bidirectional Digital Clock Pin. In Internal Serial Clock Operation mode, SCK is used as digital output for the internal serial interface clock during the Data Output period. In External Serial Clock Operation mode, SCK is used as digital input for the external serial interface clock during the Data Output period. A weak internal pull-up is automatically activated in Internal Serial Clock Operation mode. The Serial Clock Operation mode is determined by the logic level applied to the SCK pin at power up or during the most recent falling edge of \overline{CS} .

F_0 (Pin 14): Frequency Control Pin. Digital input that controls the ADC's notch frequencies and conversion time. When the F_0 pin is connected to V_{CC} ($F_0 = V_{CC}$) the converter uses its internal oscillator and the digital filter first null is located at 50Hz. When the F_0 pin is connected to GND ($F_0 = 0V$) the converter uses its internal oscillator and the digital filter first null is located at 60Hz. When F_0 is driven by an external clock signal with a frequency f_{EOSC} the converter uses this signal as its system clock and the digital filter first null is located at a frequency $f_{EOSC}/2560$.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS



APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2410 is a low power, delta-sigma analog-to-digital converter with an easy to use 3-wire serial interface. Its operation is made up of three states. The converter operating cycle begins with the conversion, followed by the low power sleep state and ends with the data output (see Figure 1). The 3-wire interface consists of serial data output (SDO), serial clock (SCK) and chip select ($\overline{\text{CS}}$).

Initially, the LTC2410 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in this sleep state, power consumption is reduced by an order of magnitude. The part remains in the sleep state as long as $\overline{\text{CS}}$ is HIGH. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

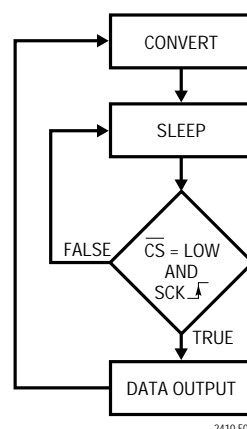


Figure 1. LTC2410 State Transition Diagram

APPLICATIONS INFORMATION

Once \overline{CS} is pulled LOW, the device begins outputting the conversion result. There is no latency in the conversion result. The data output corresponds to the conversion just performed. This result is shifted out on the serial data out pin (SDO) under the control of the serial clock (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising edge of SCK (see Figure 3). The data output state is concluded once 32 bits are read out of the ADC or when \overline{CS} is brought HIGH. The device automatically initiates a new conversion and the cycle repeats.

Through timing control of the \overline{CS} and SCK pins, the LTC2410 offers several flexible modes of operation (internal or external SCK and free-running conversion modes). These various modes do not require programming configuration registers; moreover, they do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

Conversion Clock

A major advantage the delta-sigma converter offers over conventional type converters is an on-chip digital filter (commonly implemented as a Sinc or Comb filter). For high resolution, low frequency applications, this filter is typically designed to reject line frequencies of 50 or 60Hz plus their harmonics. The filter rejection performance is directly related to the accuracy of the converter system clock. The LTC2410 incorporates a highly accurate on-chip oscillator. This eliminates the need for external frequency setting components such as crystals or oscillators. Clocked by the on-chip oscillator, the LTC2410 achieves a minimum of 110dB rejection at the line frequency (50Hz or 60Hz $\pm 2\%$).

Ease of Use

The LTC2410 data output has no latency, filter settling delay or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog voltages is easy.

The LTC2410 performs offset and full-scale calibrations every conversion cycle. This calibration is transparent to

the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

Power-Up Sequence

The LTC2410 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 2.2V. This feature guarantees the integrity of the conversion result and of the serial interface mode selection. (See the 2-wire I/O sections in the Serial Interface Timing Modes section.)

When the V_{CC} voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 0.5ms. The POR signal clears all internal registers. Following the POR signal, the LTC2410 starts a normal conversion cycle and follows the succession of states described above. The first conversion result following POR is accurate within the specifications of the device if the power supply voltage is restored within the operating range (2.7V to 5.5V) before the end of the POR time interval.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage specification for the V_{REF+} and V_{REF-} pins covers the entire range from GND to V_{CC} . For correct converter operation, the V_{REF+} pin must always be more positive than the V_{REF-} pin.

The LTC2410 can accept a differential reference voltage from 0.1V to V_{CC} . The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in microvolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a reduced reference voltage will improve the overall converter INL performance.

Input Voltage Range

The analog input is truly differential with an absolute/common mode range for the V_{IN+} and V_{IN-} input pins extending from $GND - 0.3V$ to $V_{CC} + 0.3V$. Outside

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these limits the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits the LTC2410 converts the bipolar differential input signal, $V_{IN+} - V_{IN-}$, from $-FS = -0.5 \cdot (V_{REF+} - V_{REF-})$ to $+FS = 0.5 \cdot (V_{REF+} - V_{REF-})$. Outside this range the converter indicates the overrange or the underrange condition using distinct output codes.

Input signals applied to V_{IN+} and V_{IN-} pins may extend by 300mV below ground and above V_{CC} . In order to limit any fault current, resistors of up to 5k may be added in series with the V_{IN+} and V_{IN-} pins without affecting the performance of the device. In the physical layout, it is important to maintain the parasitic capacitance of the connection between these series resistors and the corresponding pins as low as possible; therefore, the resistors should be located as close as practical to the pins. The effect of the series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent offset error due to the input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if $V_{REF} = 5V$. This error has a very strong temperature dependency.

Output Data Format

The LTC2410 serial output data stream is 32 bits long. The first 3 bits represent status information indicating the sign and conversion state. The next 24 bits are the conversion result, MSB first. The remaining 5 bits are sub LSBs beyond the 24-bit level that may be included in averaging or discarded without loss of resolution. The third and fourth bit together are also used to indicate an underrange condition (the differential input voltage is below $-FS$) or an overrange condition (the differential input voltage is above $+FS$).

Bit 31 (first output bit) is the end of conversion (\overline{EOC}) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the \overline{CS} pin is LOW. This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 30 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 29 (third output bit) is the conversion result sign indicator (SIG). If V_{IN} is >0 , this bit is HIGH. If V_{IN} is <0 , this bit is LOW.

Bit 28 (fourth output bit) is the most significant bit (MSB) of the result. This bit in conjunction with Bit 29 also provides the underrange or overrange indication. If both Bit 29 and Bit 28 are HIGH, the differential input voltage is above $+FS$. If both Bit 29 and Bit 28 are LOW, the differential input voltage is below $-FS$.

The function of these bits is summarized in Table 1.

Table 1. LTC2410 Status Bits

| Input Range | Bit 31 EOC | Bit 30 DMY | Bit 29 SIG | Bit 28 MSB |
|--|---------------|---------------|---------------|---------------|
| $V_{IN+} - V_{IN-} \geq 0.5 \cdot (V_{REF+} - V_{REF-})$ | 0 | 0 | 1 | 1 |
| $0V \leq V_{IN+} - V_{IN-} < 0.5 \cdot (V_{REF+} - V_{REF-})$ | 0 | 0 | 1 | 0 |
| $-0.5 \cdot (V_{REF+} - V_{REF-}) \leq V_{IN+} - V_{IN-} < 0V$ | 0 | 0 | 0 | 1 |
| $V_{IN+} - V_{REF-} < -0.5 \cdot (V_{REF+} - V_{REF-})$ | 0 | 0 | 0 | 0 |

Bits 28-5 are the 24-bit conversion result MSB first.

Bit 5 is the least significant bit (LSB).

Bits 4-0 are sub LSBs below the 24-bit level. Bits 4-0 may be included in averaging or discarded without loss of resolution.

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 3. Whenever \overline{CS} is HIGH, SDO remains high impedance and any externally generated SCK clock pulses are ignored by the internal data out shift register.

In order to shift the conversion result out of the device, \overline{CS} must first be driven LOW. \overline{EOC} is seen at the SDO pin of the device once \overline{CS} is pulled LOW. \overline{EOC} changes real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 31 (\overline{EOC}) can be captured on the first rising edge of SCK. Bit 30 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the falling edge of the 31st SCK and may be latched on the rising edge of the 32nd SCK pulse. On the falling edge of the 32nd SCK pulse, SDO goes HIGH indicating a new conversion cycle has been initiated. This bit serves as \overline{EOC} (Bit 31) for the next conversion cycle. Table 2 summarizes the output data format.

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As long as the voltage on the V_{IN+} and V_{IN-} pins is maintained within the $-0.3V$ to $(V_{CC} + 0.3V)$ absolute maximum operating range, a conversion result is generated for any differential input voltage $V_{IN+} - V_{IN-}$ from $-FS = -0.5 \cdot (V_{REF+} - V_{REF-})$ to $+FS = 0.5 \cdot (V_{REF+} - V_{REF-})$. For differential input voltages greater than $+FS$, the conversion result is clamped to the value corresponding to the $+FS + 1LSB$. For differential input voltages below $-FS$, the conversion result is clamped to the value corresponding to $-FS - 1LSB$.

Frequency Rejection Selection (F_0)

The LTC2410 internal oscillator provides better than 110dB normal mode rejection at the line frequency and all its harmonics for $50Hz \pm 2\%$ or $60Hz \pm 2\%$. For 60Hz rejection,

F_0 should be connected to GND while for 50Hz rejection the F_0 pin should be connected to V_{CC} .

The selection of 50Hz or 60Hz rejection can also be made by driving F_0 to an appropriate logic level. A selection change during the sleep or data output states will not disturb the converter operation. If the selection is made during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected.

When a fundamental rejection frequency different from 50Hz or 60Hz is required or when the converter must be synchronized with an outside source, the LTC2410 can operate with an external conversion clock. The converter automatically detects the presence of an external clock signal at the F_0 pin and turns off the internal oscillator. The

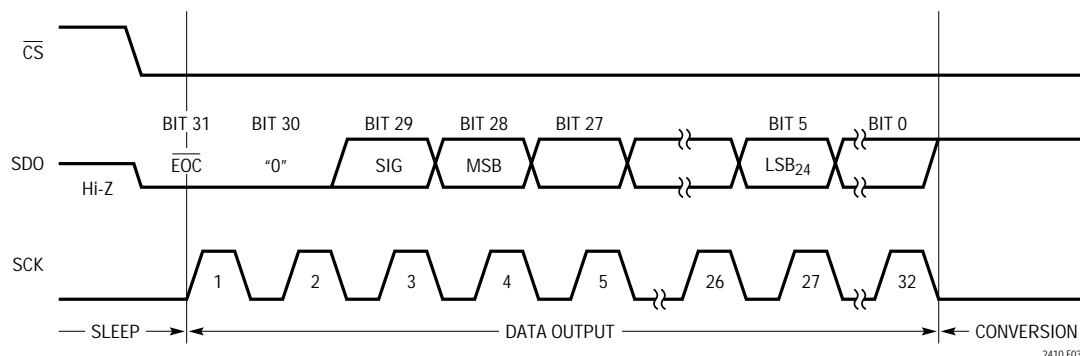


Figure 3. Output Data Timing

Table 2. LTC2410 Output Data Format

| Differential Input Voltage $V_{IN+} - V_{IN-}$ | Bit 31 EOC | Bit 30 DMY | Bit 29 SIG | Bit 28 MSB | Bit 27 | Bit 26 | Bit 25 | ... | Bit 0 |
|---|---------------|---------------|---------------|---------------|--------|--------|--------|-----|-------|
| $V_{IN+} \geq 0.5 \cdot V_{REF}^{**}$ | 0 | 0 | 1 | 1 | 0 | 0 | 0 | ... | 0 |
| $0.5 \cdot V_{REF}^{**} - 1LSB$ | 0 | 0 | 1 | 0 | 1 | 1 | 1 | ... | 1 |
| $0.25 \cdot V_{REF}^{**}$ | 0 | 0 | 1 | 0 | 1 | 0 | 0 | ... | 0 |
| $0.25 \cdot V_{REF}^{**} - 1LSB$ | 0 | 0 | 1 | 0 | 0 | 1 | 1 | ... | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | ... | 0 |
| -1LSB | 0 | 0 | 0 | 1 | 1 | 1 | 1 | ... | 1 |
| $-0.25 \cdot V_{REF}^{**}$ | 0 | 0 | 0 | 1 | 1 | 0 | 0 | ... | 0 |
| $-0.25 \cdot V_{REF}^{**} - 1LSB$ | 0 | 0 | 0 | 1 | 0 | 1 | 1 | ... | 1 |
| $-0.5 \cdot V_{REF}^{**}$ | 0 | 0 | 0 | 1 | 0 | 0 | 0 | ... | 0 |
| $V_{IN+} < -0.5 \cdot V_{REF}^{**}$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | ... | 1 |

*The differential input voltage $V_{IN} = V_{IN+} - V_{IN-}$.

**The differential reference voltage $V_{REF} = V_{REF+} - V_{REF-}$.

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frequency f_{EOSC} of the external signal must be at least 2560Hz (1Hz notch frequency) to be detected. The external clock signal duty cycle is not significant as long as the minimum and maximum specifications for the high and low periods t_{HEO} and t_{LEO} are observed.

While operating with an external conversion clock of a frequency f_{EOSC} , the LTC2410 provides better than 110dB normal mode rejection in a frequency range $f_{EOSC}/2560 \pm 4\%$ and its harmonics. The normal mode rejection as a function of the input frequency deviation from $f_{EOSC}/2560$ is shown in Figure 4.

Whenever an external clock is not present at the F_0 pin the converter automatically activates its internal oscillator and enters the Internal Conversion Clock mode. The LTC2410 operation will not be disturbed if the change of conversion clock source occurs during the sleep state or during the data output state while the converter uses an external serial clock. If the change occurs during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected. If the change occurs during the data output state and the converter is in the Internal SCK mode, the serial clock duty cycle may be affected but the serial data stream will remain valid.

Table 3 summarizes the duration of each state and the achievable output data rate as a function of F_0 .

Table 3. LTC2410 State Duration

| State | Operating Mode | | Duration |
|-------------|--|--|--|
| CONVERT | Internal Oscillator | F_0 = LOW (60Hz Rejection) | 133ms, Output Data Rate ≤ 7.5 Readings/s |
| | | F_0 = HIGH (50Hz Rejection) | 160ms, Output Data Rate ≤ 6.2 Readings/s |
| | External Oscillator | F_0 = External Oscillator with Frequency f_{EOSC} kHz ($f_{EOSC}/2560$ Rejection) | $20480/f_{EOSC}$ S, Output Data Rate $\leq f_{EOSC}/20480$ Readings/s |
| SLEEP | | | As Long As \overline{CS} = HIGH Until \overline{CS} = LOW and SCK \uparrow |
| DATA OUTPUT | Internal Serial Clock | F_0 = LOW/HIGH (Internal Oscillator) | As Long As \overline{CS} = LOW But Not Longer Than 1.67ms (32 SCK cycles) |
| | | F_0 = External Oscillator with Frequency f_{EOSC} kHz | As Long As \overline{CS} = LOW But Not Longer Than $256/f_{EOSC}$ ms (32 SCK cycles) |
| | External Serial Clock with Frequency f_{SCK} kHz | | As Long As \overline{CS} = LOW But Not Longer Than $32/f_{SCK}$ ms (32 SCK cycles) |

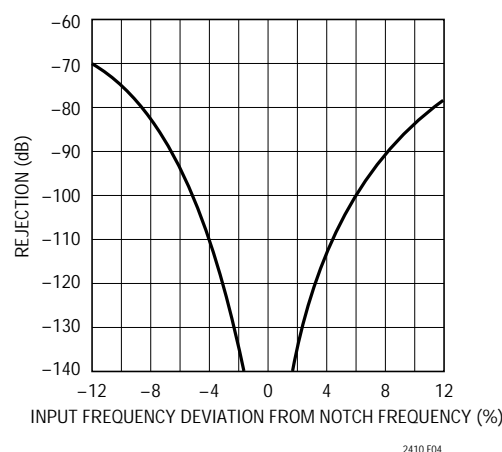


Figure 4. LTC2410 Normal Mode Rejection When Using an External Oscillator of Frequency f_{EOSC}

SERIAL INTERFACE PINS

The LTC2410 transmits the conversion results and receives the start of conversion command through a synchronous 3-wire interface. During the conversion and sleep states, this interface can be used to assess the converter status and during the data output state it is used to read the conversion result.

Serial Clock Input/Output (SCK)

The serial clock signal present on SCK (Pin 13) is used to synchronize the data transfer. Each bit of data is shifted out the SDO pin on the falling edge of the serial clock.

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In the Internal SCK mode of operation, the SCK pin is an output and the LTC2410 creates its own serial clock by dividing the internal conversion clock by 8. In the External SCK mode of operation, the SCK pin is used as input. The internal or external SCK mode is selected on power-up and then reselected every time a HIGH-to-LOW transition is detected at the \overline{CS} pin. If SCK is HIGH or floating at power-up or during this transition, the converter enters the internal SCK mode. If SCK is LOW at power-up or during this transition, the converter enters the external SCK mode.

Serial Data Output (SDO)

The serial data output pin, SDO (Pin 12), provides the result of the last conversion as a serial bit stream (MSB first) during the data output state. In addition the SDO pin is used as an end of conversion indicator during the conversion and sleep states.

When \overline{CS} (Pin 11) is HIGH, the SDO driver is switched to a high impedance state. This allows sharing the serial interface with other devices. If \overline{CS} is LOW during the convert or sleep state, SDO will output EOC. If \overline{CS} is LOW during the conversion phase, the \overline{EOC} bit appears HIGH on the SDO pin. Once the conversion is complete, \overline{EOC} goes LOW. The device remains in the sleep state until the first rising edge of SCK occurs while \overline{CS} = LOW.

Chip Select Input (CS)

The active LOW chip select, \overline{CS} (Pin 11), is used to test the conversion status and to enable the data output transfer as described in the previous sections.

In addition, the \overline{CS} signal can be used to trigger a new conversion cycle before the entire serial data transfer has been completed. The LTC2410 will abort any serial data transfer in progress and start a new conversion cycle

anytime a LOW-to-HIGH transition is detected at the \overline{CS} pin after the converter has entered the data output state (i.e., after the first rising edge of SCK occurs with \overline{CS} = LOW).

Finally, \overline{CS} can be used to control the free-running modes of operation, see Serial Interface Timing Modes section. Grounding \overline{CS} will force the ADC to continuously convert at the maximum output rate selected by F_0 . Tying a capacitor to \overline{CS} will reduce the output rate and power dissipation by a factor proportional to the capacitor's value, see Figures 12 to 14.

SERIAL INTERFACE TIMING MODES

The LTC2410's 3-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 2- or 3-wire I/O, single cycle conversion and autostart. The following sections describe each of these serial interface timing modes in detail. In all these cases the converter can use the internal oscillator (F_0 = LOW or F_0 = HIGH) or an external oscillator connected to the F_0 pin. Refer to Table 4 for a summary.

External Serial Clock, Single Cycle Operation (SPI/MICROWIRE Compatible)

This timing mode uses an external serial clock to shift out the conversion result and a \overline{CS} signal to monitor and control the state of the conversion cycle, see Figure 5.

The serial clock mode is selected on the falling edge of \overline{CS} . To select the external serial clock mode, the serial clock pin (SCK) must be LOW during each \overline{CS} falling edge.

The serial data output pin (SDO) is HI-Z as long as \overline{CS} is HIGH. At any time during the conversion cycle, \overline{CS} may be

Table 4. LTC2410 Interface Timing Modes

| Configuration | SCK Source | Conversion Cycle Control | Data Output Control | Connection and Waveforms |
|---|------------|----------------------------|----------------------------|--------------------------|
| External SCK, Single Cycle Conversion | External | \overline{CS} and SCK | \overline{CS} and SCK | Figures 5, 6 |
| External SCK, 2-Wire I/O | External | SCK | SCK | Figure 7 |
| Internal SCK, Single Cycle Conversion | Internal | $\overline{CS} \downarrow$ | $\overline{CS} \downarrow$ | Figures 8, 9 |
| Internal SCK, 2-Wire I/O, Continuous Conversion | Internal | Continuous | Internal | Figure 10 |
| Internal SCK, Autostart Conversion | Internal | C_{EXT} | Internal | Figure 11 |

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pulled LOW in order to monitor the state of the converter. While \overline{CS} is pulled LOW, \overline{EOC} is output to the SDO pin. $\overline{EOC} = 1$ while a conversion is in progress and $\overline{EOC} = 0$ if the device is in the sleep state. Independent of \overline{CS} , the device automatically enters the low power sleep state once the conversion is complete.

When the device is in the sleep state ($\overline{EOC} = 0$), its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen while \overline{CS} is LOW. Data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. \overline{EOC} can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. On the 32nd falling edge of SCK, the device begins a new conversion. SDO goes HIGH ($\overline{EOC} = 1$) indicating a conversion is in progress.

At the conclusion of the data cycle, \overline{CS} may remain LOW and \overline{EOC} monitored as an end-of-conversion interrupt. Alternatively, \overline{CS} may be driven HIGH setting SDO to HI-Z. As described above, \overline{CS} may be pulled LOW at any time in order to monitor the conversion status.

Typically, \overline{CS} remains LOW during the data output state. However, the data output state may be aborted by pulling \overline{CS} HIGH anytime between the first rising edge and the 32nd falling edge of SCK, see Figure 6. On the rising edge of \overline{CS} , the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle or synchronizing the start of a conversion.

External Serial Clock, 2-Wire I/O

This timing mode utilizes a 2-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal, see Figure 7. \overline{CS} may be permanently tied to ground, simplifying the user interface or isolation barrier.

The external serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 0.5ms after V_{CC} exceeds 2.2V. The level applied to SCK at this time determines if SCK is internal or external. SCK must be driven LOW prior to the end of POR in order to enter the external serial clock timing mode.

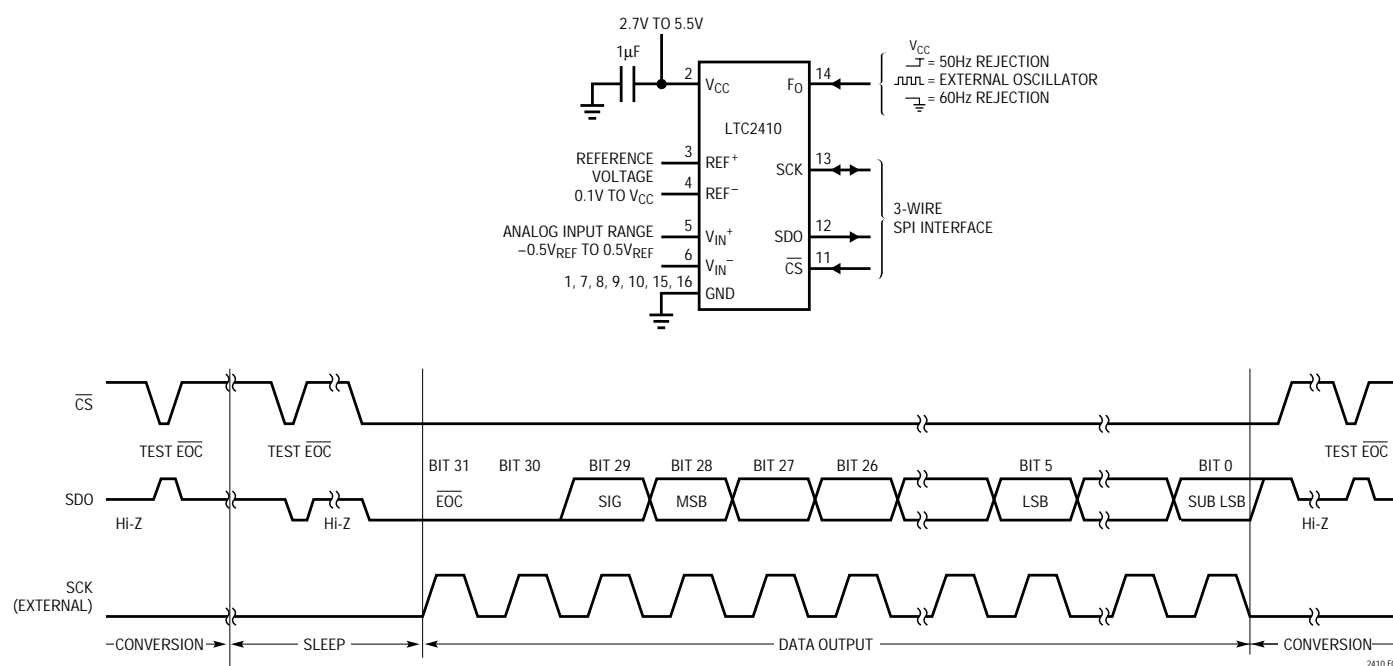


Figure 5. External Serial Clock, Single Cycle Operation

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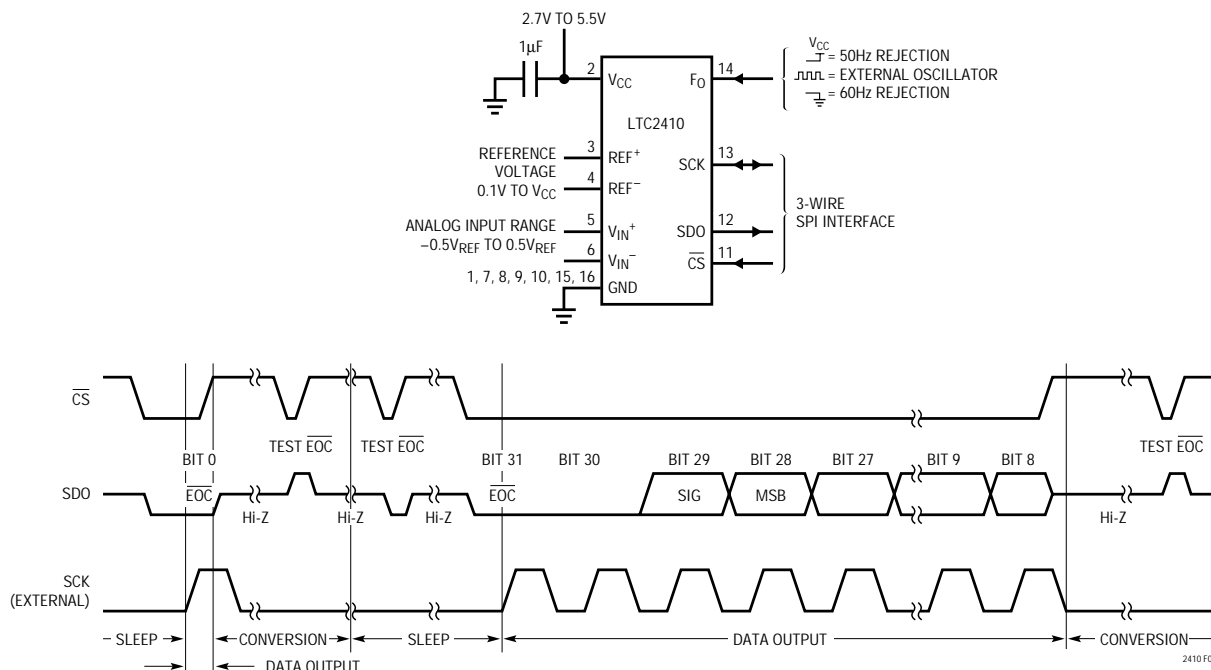


Figure 6. External Serial Clock, Reduced Data Output Length

Since \overline{CS} is tied LOW, the end-of-conversion (\overline{EOC}) can be continuously monitored at the SDO pin during the convert and sleep states. \overline{EOC} may be used as an interrupt to an external controller indicating the conversion result is ready. $\overline{EOC} = 1$ while the conversion is in progress and $\overline{EOC} = 0$ once the conversion enters the low power sleep state. On the falling edge of \overline{EOC} , the conversion result is loaded into an internal static shift register. The device remains in the sleep state until the first rising edge of SCK. Data is shifted out the SDO pin on each falling edge of SCK enabling external circuitry to latch data on the rising edge of SCK. \overline{EOC} can be latched on the first rising edge of SCK. On the 32nd falling edge of SCK, SDO goes HIGH ($\overline{EOC} = 1$) indicating a new conversion has begun.

Internal Serial Clock, Single Cycle Operation

This timing mode uses an internal serial clock to shift out the conversion result and a \overline{CS} signal to monitor and control the state of the conversion cycle, see Figure 8.

In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating (HI-Z) or pulled HIGH prior to the falling edge of \overline{CS} . The device will not

enter the internal serial clock mode if SCK is driven LOW on the falling edge of \overline{CS} . An internal weak pull-up resistor is active on the SCK pin during the falling edge of \overline{CS} ; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven.

The serial data output pin (SDO) is HI-Z as long as \overline{CS} is HIGH. At any time during the conversion cycle, \overline{CS} may be pulled LOW in order to monitor the state of the converter. Once \overline{CS} is pulled LOW, SCK goes LOW and \overline{EOC} is output to the SDO pin. $\overline{EOC} = 1$ while a conversion is in progress and $\overline{EOC} = 0$ if the device is in the sleep state.

When testing \overline{EOC} , if the conversion is complete ($\overline{EOC} = 0$), the device will exit the sleep state and enter the data output state if \overline{CS} remains LOW. In order to prevent the device from exiting the low power sleep state, \overline{CS} must be pulled HIGH before the first rising edge of SCK. In the internal SCK timing mode, SCK goes HIGH and the device begins outputting data at time $t_{EOCtest}$ after the falling edge of \overline{CS} (if $\overline{EOC} = 0$) or $t_{EOCtest}$ after \overline{EOC} goes LOW (if \overline{CS} is LOW during the falling edge of \overline{EOC}). The value of $t_{EOCtest}$ is 23µs if the device is using its internal oscillator ($F_0 = \text{logic LOW or HIGH}$). If F_0 is driven by an external oscillator of

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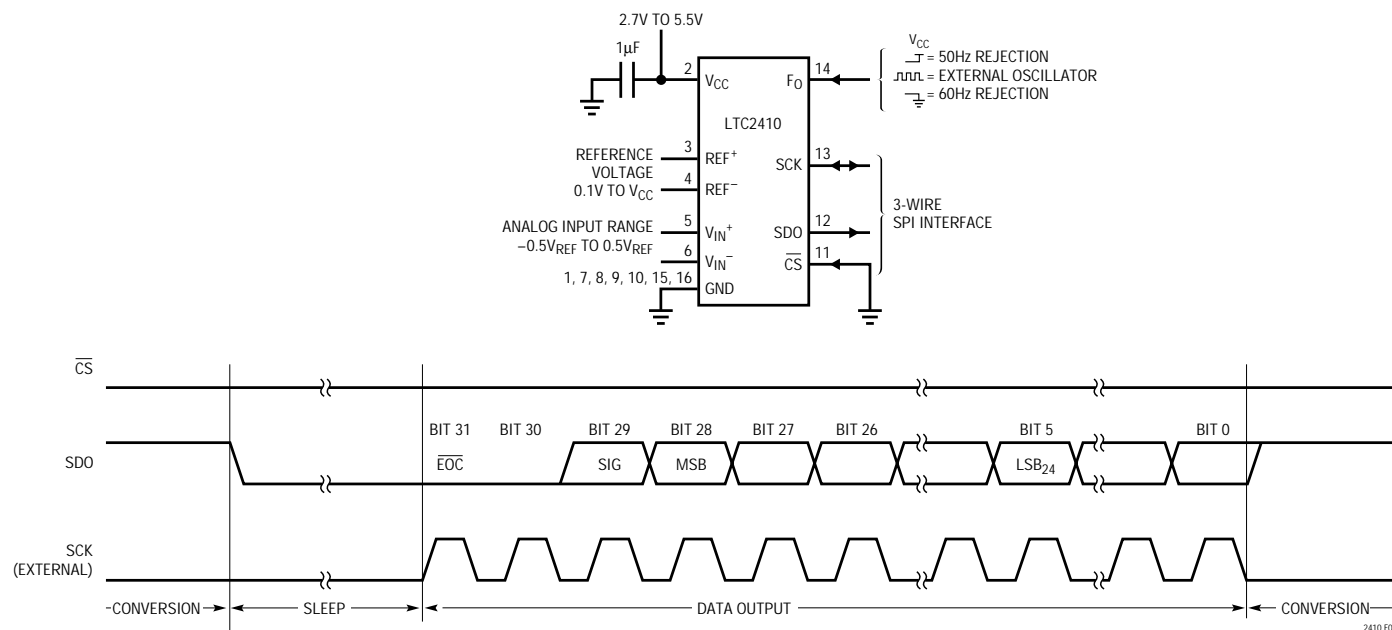
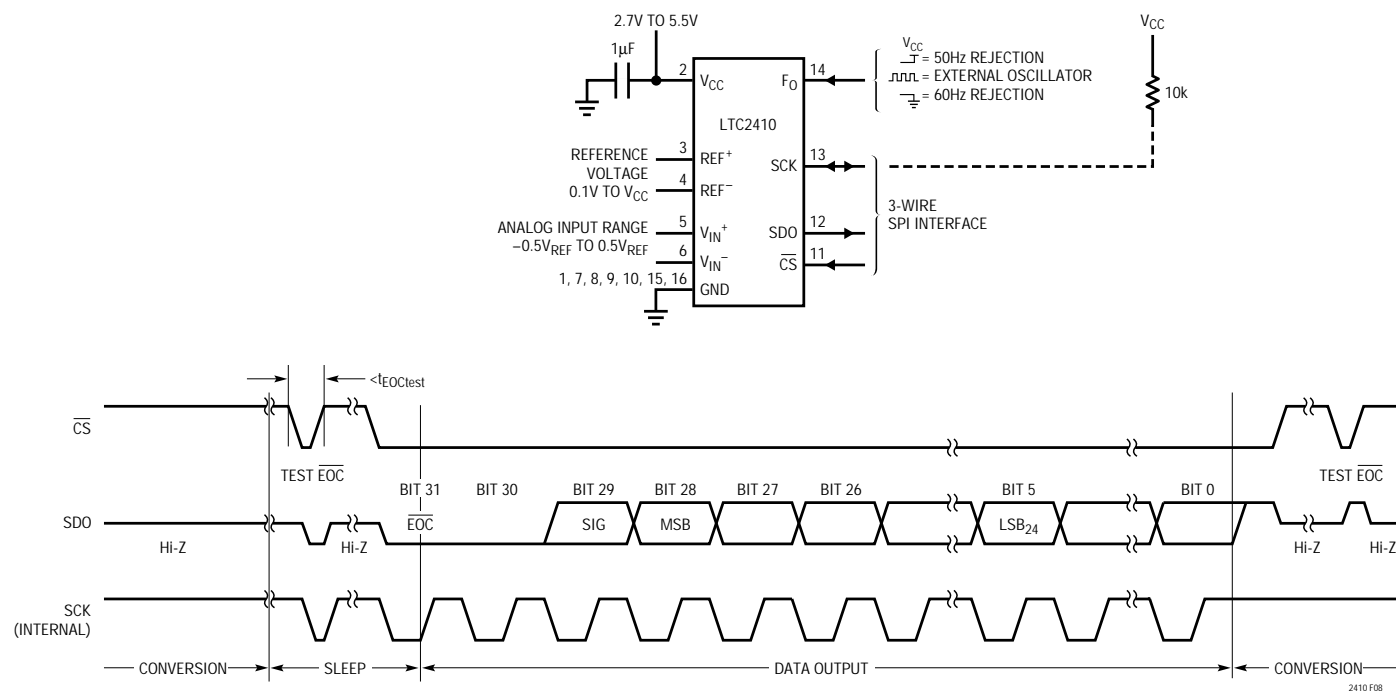
Figure 7. External Serial Clock, $\overline{CS} = 0$ Operation

Figure 8. Internal Serial Clock, Single Cycle Operation

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frequency f_{EOSC} , then t_{EOCtest} is $3.6/f_{\text{EOSC}}$. If $\overline{\text{CS}}$ is pulled HIGH before time t_{EOCtest} , the device remains in the sleep state. The conversion result is held in the internal static shift register.

If $\overline{\text{CS}}$ remains LOW longer than t_{EOCtest} , the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data output cycle begins on this first rising edge of SCK and concludes after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{\text{EOC}}$ can be latched on the first rising edge of SCK and the last bit of the conversion result on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ($\overline{\text{EOC}} = 1$), SCK stays HIGH and a new conversion starts.

Typically, $\overline{\text{CS}}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{\text{CS}}$ HIGH anytime between the first and 32nd rising edge of SCK, see Figure 9. On the rising edge of $\overline{\text{CS}}$, the device aborts the data output state and immediately initiates a

new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle, or synchronizing the start of a conversion. If $\overline{\text{CS}}$ is pulled HIGH while the converter is driving SCK LOW, the internal pull-up is not available to restore SCK to a logic HIGH state. This will cause the device to exit the internal serial clock mode on the next falling edge of $\overline{\text{CS}}$. This can be avoided by adding an external 10k pull-up resistor to the SCK pin or by never pulling $\overline{\text{CS}}$ HIGH when SCK is LOW.

Whenever SCK is LOW, the LTC2410's internal pull-up at pin SCK is disabled. Normally, SCK is not externally driven if the device is in the internal SCK timing mode. However, certain applications may require an external driver on SCK. If this driver goes HI-Z after outputting a LOW signal, the LTC2410's internal pull-up remains disabled. Hence, SCK remains LOW. On the next falling edge of $\overline{\text{CS}}$, the device is switched to the external SCK timing mode. By adding an external 10k pull-up resistor to SCK, this pin goes HIGH once the external driver goes HI-Z. On the next $\overline{\text{CS}}$ falling edge, the device will remain in the internal SCK timing mode.

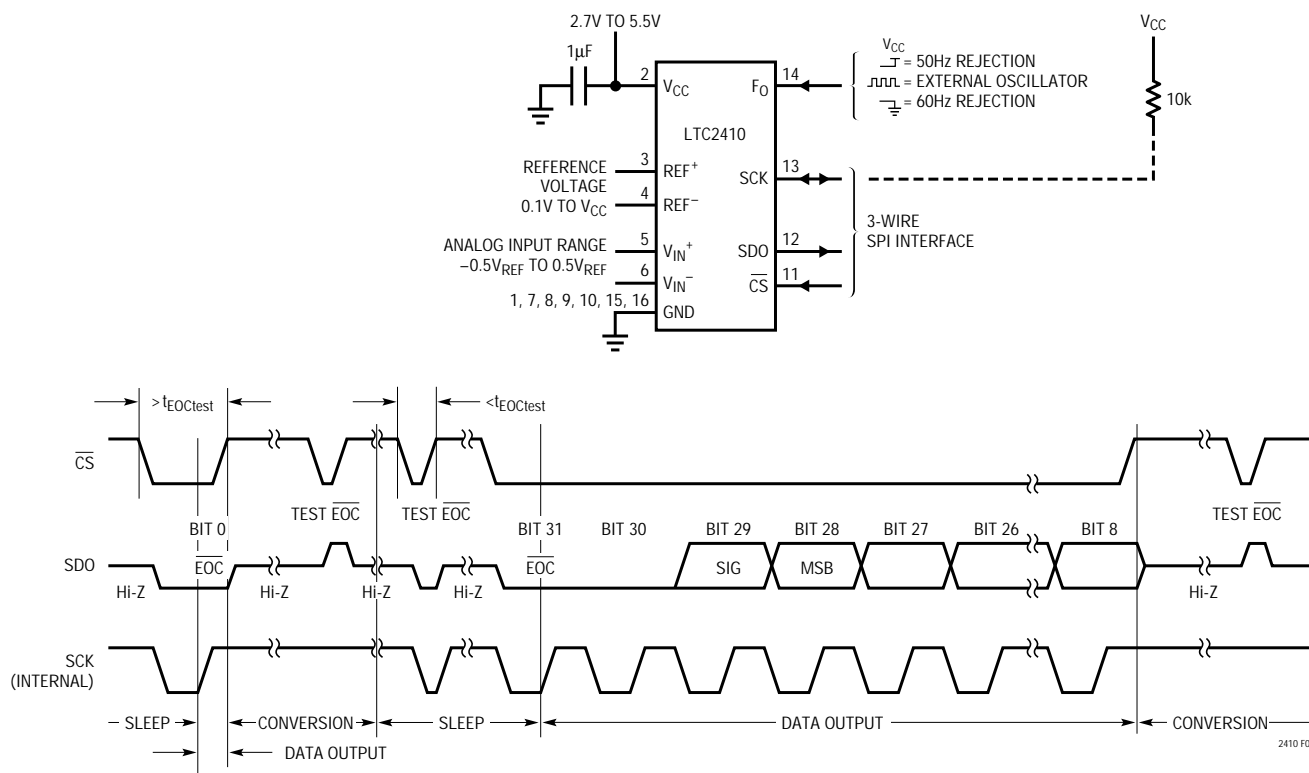


Figure 9. Internal Serial Clock, Reduced Data Output Length

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Internal Serial Clock, Autostart Conversion

This timing mode is identical to the internal serial clock, 2-wire I/O described above with one additional feature. Instead of grounding $\overline{\text{CS}}$, an external timing capacitor is tied to $\overline{\text{CS}}$.

While the conversion is in progress, the $\overline{\text{CS}}$ pin is held HIGH by an internal weak pull-up. Once the conversion is complete, the device enters the low power sleep state and an internal 25nA current source begins discharging the capacitor tied to $\overline{\text{CS}}$, see Figure 11. The time the converter spends in the sleep state is determined by the value of the external timing capacitor, see Figures 12 and 13. Once the voltage at $\overline{\text{CS}}$ falls below an internal threshold ($\approx 1.4\text{V}$), the device automatically begins outputting data. The data output cycle begins on the first rising edge of SCK and ends on the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be

used to shift the conversion result into external circuitry. After the 32nd rising edge, $\overline{\text{CS}}$ is pulled HIGH and a new conversion is immediately started. This is useful in applications requiring periodic monitoring and ultralow power. Figure 14 shows the average supply current as a function of capacitance on $\overline{\text{CS}}$.

It should be noticed that the external capacitor discharge current is kept very small in order to decrease the converter power dissipation in the sleep state. In the autostart mode the analog voltage on the $\overline{\text{CS}}$ pin cannot be observed without disturbing the converter operation using a regular oscilloscope probe. When using this configuration it is important to minimize the external leakage current at the $\overline{\text{CS}}$ pin by using a low leakage external capacitor and properly cleaning the PCB surface.

The internal serial clock mode is selected every time the voltage on the $\overline{\text{CS}}$ pin crosses an internal threshold voltage. An internal weak pull-up at the SCK pin is active while

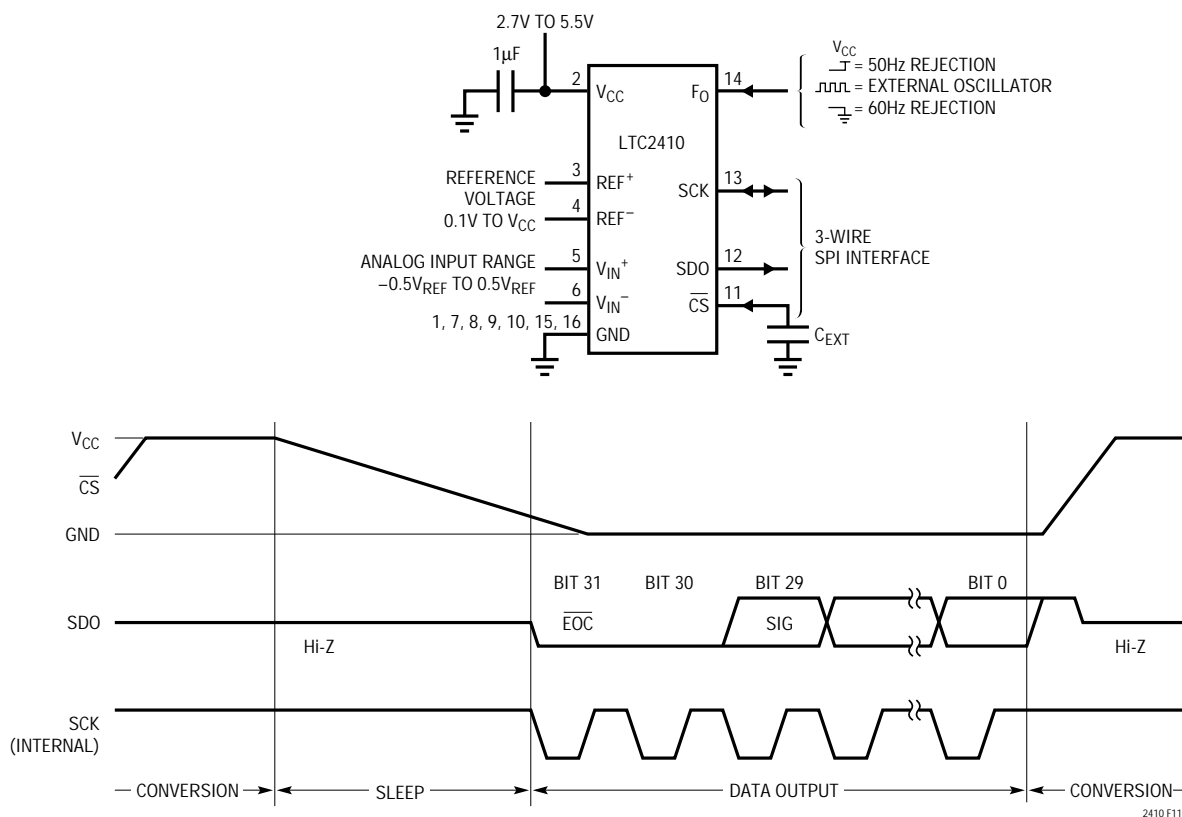
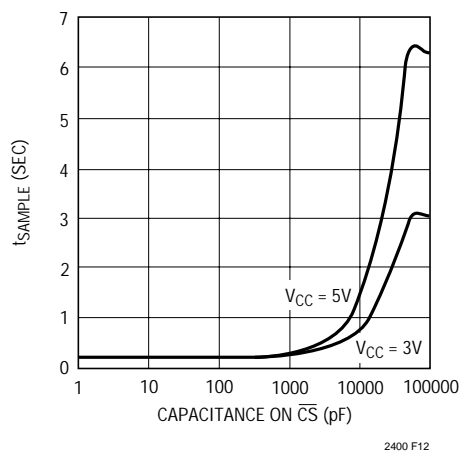
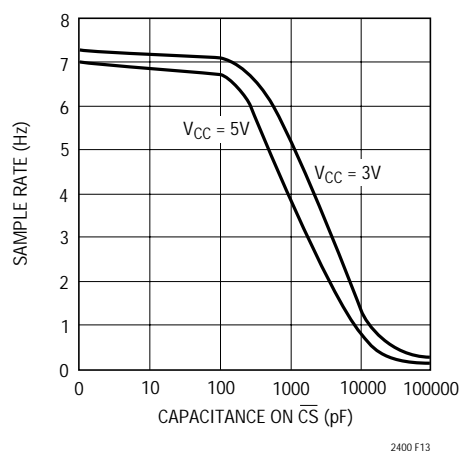
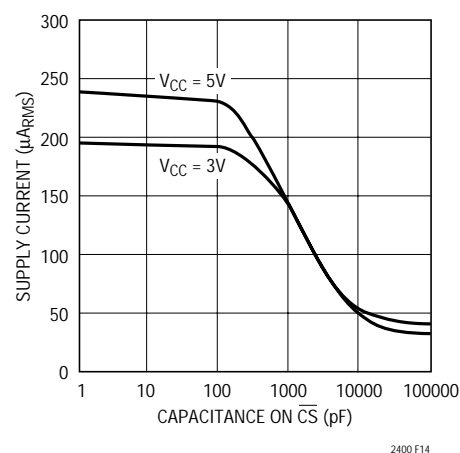


Figure 11. Internal Serial Clock, Autostart Operation

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Figure 12. $\overline{\text{CS}}$ Capacitance vs t_{SAMPLE} Figure 13. $\overline{\text{CS}}$ Capacitance vs Output RateFigure 14. $\overline{\text{CS}}$ Capacitance vs Supply Current

$\overline{\text{CS}}$ is discharging; therefore, the internal serial clock timing mode is automatically selected if SCK is floating. It is important to ensure there are no external drivers pulling SCK LOW while $\overline{\text{CS}}$ is discharging.

PRESERVING THE CONVERTER ACCURACY

The LTC2410 is designed to reduce as much as possible the conversion result sensitivity to device decoupling, PCB layout, antialiasing circuits, line frequency perturbations and so on. Nevertheless, in order to preserve the extreme accuracy capability of this part, some simple precautions are desirable.

Digital Signal Levels

The LTC2410's digital interface is easy to use. Its digital inputs (F_0 , $\overline{\text{CS}}$ and SCK in External SCK mode of operation) accept standard TTL/CMOS logic levels and the internal hysteresis receivers can tolerate edge rates as slow as $100\mu\text{s}$. However, some considerations are required to take advantage of the exceptional accuracy and low supply current of this converter.

The digital output signals (SDO and SCK in Internal SCK mode of operation) are less of a concern because they are not generally active during the conversion state.

While a digital input signal is in the range 0.5V to $(V_{\text{CC}} - 0.5\text{V})$, the CMOS input receiver draws additional current from the power supply. It should be noted that, when any one of the digital input signals (F_0 , $\overline{\text{CS}}$ and SCK in External SCK mode of operation) is within this range, the LTC2410 power supply current may increase even if the signal in question is at a valid logic level. For micropower operation, it is recommended to drive all digital input signals to full CMOS levels [$V_{\text{IL}} < 0.4\text{V}$ and $V_{\text{OH}} > (V_{\text{CC}} - 0.4\text{V})$].

During the conversion period, the undershoot and/or overshoot of a fast digital signal connected to the LTC2410 pins may severely disturb the analog to digital conversion process. Undershoot and overshoot can occur because of the impedance mismatch at the converter pin when the transition time of an external control signal is less than twice the propagation delay from the driver to LTC2410. For reference, on a regular FR-4 board, signal propagation

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velocity is approximately 183ps/inch for internal traces and 170ps/inch for surface traces. Thus, a driver generating a control signal with a minimum transition time of 1ns must be connected to the converter pin through a trace shorter than 2.5 inches. This problem becomes particularly difficult when shared control lines are used and multiple reflections may occur. The solution is to carefully terminate all transmission lines close to their characteristic impedance.

Parallel termination near the LTC2410 pin will eliminate this problem but will increase the driver power dissipation. A series resistor between 27Ω and 56Ω placed near the driver or near the LTC2410 pin will also eliminate this problem without additional power dissipation. The actual resistor value depends upon the trace impedance and connection topology.

An alternate solution is to reduce the edge rate of the control signals. It should be noted that using very slow edges will increase the converter power supply current during the transition time. The multiple ground pins used in this package configuration, as well as the differential input and reference architecture, reduce substantially the converter sensitivity to ground currents.

Particular attention must be given to the connection of the F_0 signal when the LTC2410 is used with an external conversion clock. This clock is active during the conversion time and the normal mode rejection provided by the internal digital filter is not very high at its frequency. A normal mode signal of this frequency at the converter reference terminals may result into DC gain and INL errors. A normal mode signal of this frequency at the converter input terminals may result into a DC offset error. Such perturbations may occur due to asymmetric capacitive coupling between the F_0 signal trace and the converter input and/or reference connection traces. An immediate solution is to maintain maximum possible separation between the F_0 signal trace and the input/reference signals. When the F_0 signal is parallel terminated near the converter substantial AC current is flowing in the loop formed by the F_0 connection trace, the termination and the ground return path. Thus, perturbation signals may be inductively coupled into the converter input and/or reference. In this situation the user must reduce to a minimum

the loop area for the F_0 signal as well as the loop for the differential input and reference connections.

Driving the Input and Reference

The input and reference pins of the LTC2410 converter are directly connected to a network of sampling capacitors. Depending upon the relation between the differential input voltage and the differential reference voltage these capacitors are switching between these four pins transferring small amounts of charge in the process. A simplified equivalent circuit is shown in Figure 15.

The key to understanding the effects of this dynamic input current is based on a simple first order RC time constant model. Using the internal oscillator, the LTC2410's internal switched capacitor network is clocked at 76800Hz corresponding to a $13\mu\text{s}$ sampling period. Fourteen time constants are required each time a capacitor is switched in order to achieve 1ppm settling accuracy.

Therefore, the equivalent time constant at V_{IN+} , V_{IN-} , V_{REF+} and V_{REF-} should be less than $13\mu\text{s}/14 = 920\text{ns}$ in order to achieve 1ppm accuracy.

Input Current

If complete settling occurs on the input, conversion results will be unaffected by the dynamic input current. An incomplete settling of the input signal sampling process may result in gain and offset errors but it will not degrade the INL performance of the converter. Figure 15 shows the mathematical expressions for the average bias currents flowing through the V_{IN+} and V_{IN-} pins as a result of the sampling charge transfers when integrated over a substantial time period (longer than 64 internal clock cycles).

The effect of this input dynamic current can be analyzed using the test circuit of Figure 16. For simplicity two distinct situations can be considered.

For relatively small values of the input capacitors ($C_{IN} < 0.01\mu\text{F}$) the voltage on the sampling capacitor settles almost completely and relatively large values for the source impedance result in only small errors. Such values for C_{IN} will deteriorate the converter offset and gain performance without significant benefits of signal filtering and the user is advised to avoid them. Nevertheless, when

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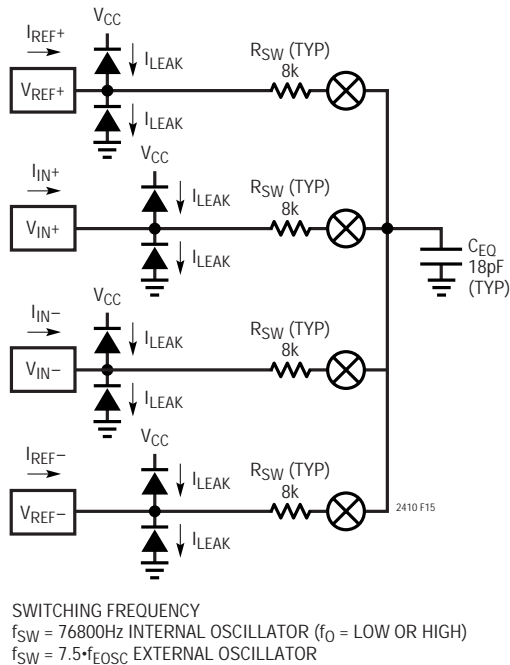


Figure 15. LTC2410 Equivalent Analog Input Circuit

small values of C_{IN} are unavoidably present as parasitics of input multiplexers, wires, connectors or sensors the LTC2410 can maintain its exceptional accuracy while operating with relative large values of source resistance as shown in Figures 17 and 18. For small C_{IN} values, the settling on IN^+ and IN^- occurs independently and there is little benefit in trying to match the source impedance for the two pins.

$$I_{+(AVG)} = \frac{V_{INDIFF}}{R_{EQ}} + 2 \left(\frac{V_{IN^+} - V_{REFCM}}{R_{EQ}} \right)$$

$$I_{-(AVG)} = -\frac{V_{INDIFF}}{R_{EQ}} + 2 \left(\frac{V_{IN^-} - V_{REFCM}}{R_{EQ}} \right)$$

$$I_{R^+ (AVG)} = 2 \left(\frac{V_{REFDIFF}}{R_{EQ}} \right) + 2 \left(\frac{V_{R^+} - V_{INCM}}{R_{EQ}} \right) - \left(\frac{V_{INDIFF}}{R_{EQ}} \right) \left(\frac{V_{INDIFF}}{V_{REFDIFF}} \right)$$

$$I_{R^- (AVG)} = -2 \left(\frac{V_{REFDIFF}}{R_{EQ}} \right) + 2 \left(\frac{V_{R^-} - V_{INCM}}{R_{EQ}} \right) + \left(\frac{V_{INDIFF}}{R_{EQ}} \right) \left(\frac{V_{INDIFF}}{V_{REFDIFF}} \right)$$

where:

$$V_{REFDIFF} = V_{R^+} - V_{R^-}$$

$$V_{REFCM} = \left(\frac{V_{R^+} + V_{R^-}}{2} \right)$$

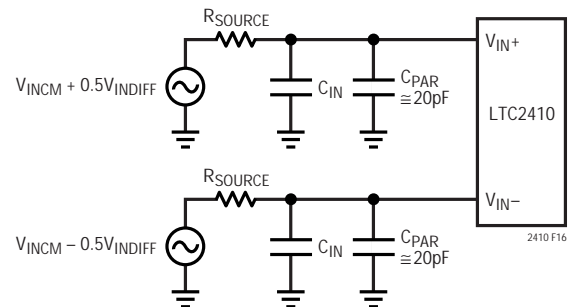
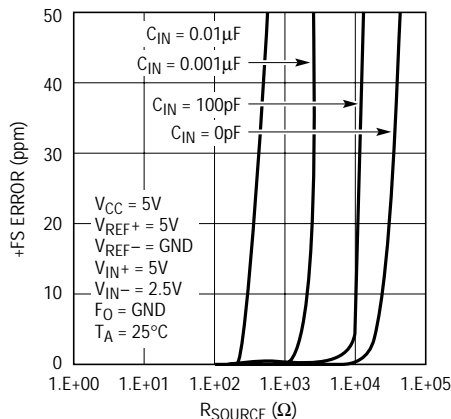
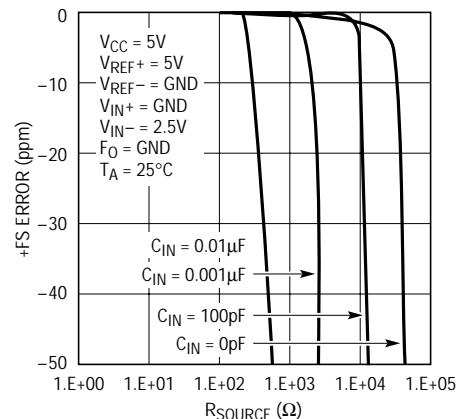
$$V_{INDIFF} = V_{I^+} - V_{I^-}$$

$$V_{INCM} = \left(\frac{V_{I^+} + V_{I^-}}{2} \right)$$

$$R_{EQ} = 3.61\text{M}\Omega \text{ INTERNAL OSCILLATOR } 60\text{Hz Notch } (F_0 = \text{LOW})$$

$$R_{EQ} = 4.32\text{M}\Omega \text{ INTERNAL OSCILLATOR } 50\text{Hz Notch } (F_0 = \text{HIGH})$$

$$R_{EQ} = (0.555 \cdot 10^{12}) / f_{OSC} \text{ EXTERNAL OSCILLATOR}$$

Figure 16. An RC Network at V_{IN} Figure 17. +FS Error vs R_{SOURCE} at V_{IN^+} or V_{IN^-} (Small C_{IN})Figure 18. -FS Error vs R_{SOURCE} at V_{IN^+} or V_{IN^-} (Small C_{IN})

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Larger values of input capacitors ($C_{IN} > 0.01\mu F$) may be required in certain configurations for antialiasing or general input signal filtering. Such capacitors will average the input sampling charge and the external source resistance will see a quasi constant input differential impedance. When $F_O = \text{LOW}$ (internal oscillator and 60Hz notch), the typical differential input resistance is $1.8M\Omega$ which will generate a gain error of approximately 0.28ppm for each ohm of source resistance driving IN^+ or IN^- . When $F_O = \text{HIGH}$ (internal oscillator and 50Hz notch), the typical differential input resistance is $2.16M\Omega$ which will generate a gain error of approximately 0.23ppm for each ohm of source resistance driving IN^+ or IN^- . When F_O is driven by an external oscillator with a frequency f_{EOSC} (external conversion clock operation), the typical differential input resistance is $0.28 \cdot 10^{12} / f_{EOSC} \Omega$ and each ohm of source resistance driving IN^+ or IN^- will result in $1.78 \cdot 10^{-6} \cdot f_{EOSC} \text{ppm}$ gain error. The effect of the source resistance on the two input pins is additive with respect to this gain error. The typical +FS and -FS errors as a function of the sum of the source resistance seen by IN^+ and IN^- for large values of C_{IN} are shown in Figures 19 and 20.

In addition to this gain error an offset error term may also appear. The offset error is proportional with the mismatch between the source impedance driving the two input pins V_{IN+} and V_{IN-} and with the difference between the input and reference common mode voltages. While the input drive circuit nonzero source impedance combined with the converter average input current will not degrade the INL performance indirect distortion may result from the modulation of the offset error by the common mode component of the input signal. Thus, when using large C_{IN} capacitor values, it is advisable to carefully match the source impedance seen by the V_{IN+} and V_{IN-} pins. When $F_O = \text{LOW}$ (internal oscillator and 60Hz notch), every 1Ω mismatch in source impedance transforms a full-scale common mode input signal into a differential mode input signal of 0.28ppm. When $F_O = \text{HIGH}$ (internal oscillator and 50Hz notch), every 1Ω mismatch in source impedance transforms a full-scale common mode input signal into a differential mode input signal of 0.23ppm. When F_O is driven by an external oscillator with a frequency f_{EOSC} , every 1Ω mismatch in source impedance transforms a

full-scale common mode input signal into a differential mode input signal of $1.78 \cdot 10^{-6} \cdot f_{EOSC} \text{ppm}$. Figure 21 shows the typical offset error due to input common mode voltage for various values of source resistance imbalance between the IN^+ and IN^- pins when large C_{IN} values are used.

If possible, it is desirable to operate with the input signal common mode voltage very close to the reference signal common mode voltage as is the case in the ratiometric measurement of a symmetric bridge. This configuration eliminates the offset error caused by mismatched source impedances.

The magnitude of the dynamic input current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typical better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance seen by V_{IN+} and V_{IN-} the expected drift of the dynamic current offset and gain errors will be insignificant (about 1% of their respective values over the entire temperature and voltage range). Even for the most stringent applications a one-time calibration operation may be sufficient.

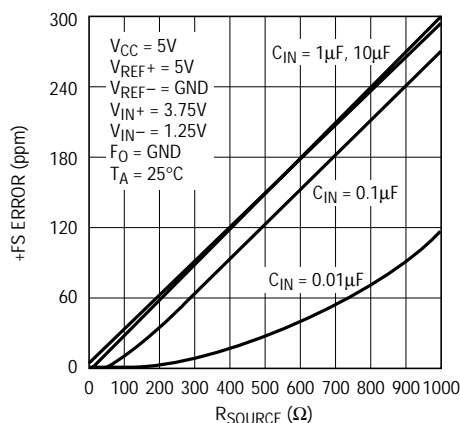
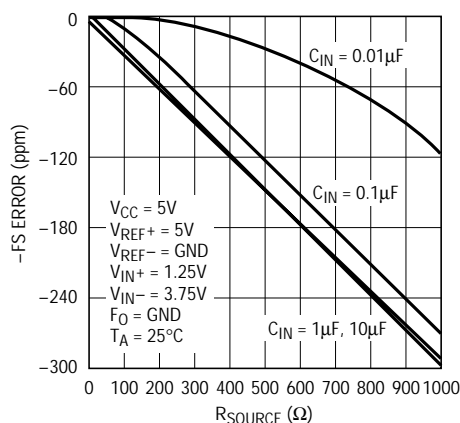
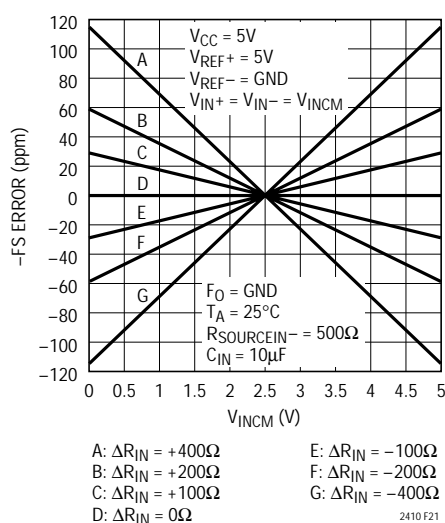
In addition to the input sampling charge, the input ESD protection diodes have a temperature dependent leakage current. This current, nominally 1nA ($\pm 10\text{nA max}$), results in a small offset shift. A 100Ω source resistance will create a 0.1 μV typical and 1 μV maximum offset voltage.

Reference Current

In a similar fashion the LTC2410 samples the differential reference pins V_{REF+} and V_{REF-} transferring small amount of charge to and from the external driving circuits thus producing a dynamic reference current. This current does not change the converter offset but it may degrade the gain and INL performance. The effect of this current can be analyzed in the same two distinct situations.

For relatively small values of the external reference capacitors ($C_{REF} < 0.01\mu F$) the voltage on the sampling capacitor settles almost completely and relatively large values for the source impedance result in only small errors. Such

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Figure 19. +FS Error vs R_{SOURCE} at V_{IN+} and V_{IN-} (Large C_{IN})Figure 20. -FS Error vs R_{SOURCE} at V_{IN+} and V_{IN-} (Large C_{IN})Figure 21. Offset Error vs Common Mode Voltage ($V_{INCM} = V_{IN+} = V_{IN-}$) and Input Source Resistance Imbalance ($\Delta R_{IN} = R_{SOURCEIN+} - R_{SOURCEIN-}$) for Large C_{IN} Values ($C_{IN} \geq 1\mu F$)

values for C_{REF} will deteriorate the converter offset and gain performance without significant benefits of reference filtering and the user is advised to avoid them.

Larger values of reference capacitors ($C_{REF} > 0.01\mu F$) may be required as reference filters in certain configurations. Such capacitors will average the reference sampling charge and the external source resistance will see a quasi constant reference differential impedance. When $F_O = LOW$ (internal oscillator and 60Hz notch), the typical differential reference resistance is $1.3M\Omega$ which will generate a gain error of approximately 0.38ppm for each ohm of source resistance driving REF^+ or REF^- . When $F_O = HIGH$ (internal oscillator and 50Hz notch), the typical differential reference resistance is $1.56M\Omega$ which will generate a gain error of approximately 0.32ppm for each ohm of source resistance driving REF^+ or REF^- . When F_O is driven by an external oscillator with a frequency f_{EOSC} (external conversion clock operation), the typical differential reference resistance is $0.20 \cdot 10^{12} / f_{EOSC} \Omega$ and each ohm of source resistance driving REF^+ or REF^- will result in $2.47 \cdot 10^{-6} \cdot f_{EOSC} ppm$ gain error. The effect of the source resistance on the two reference pins is additive with respect to this gain error. The typical +FS and -FS errors for various combinations of source resistance seen by the REF^+ and REF^- pins and external capacitance C_{REF} connected to these pins are shown in Figures 22, 23, 24 and 25.

In addition to this gain error the converter INL performance is degraded by the reference source impedance. When $F_O = LOW$ (internal oscillator and 60Hz notch), every 100Ω of source resistance driving REF^+ or REF^- translates into about 1.34ppm additional INL error. When $F_O = HIGH$ (internal oscillator and 50Hz notch), every 100Ω of source resistance driving REF^+ or REF^- translates into about 1.1ppm additional INL error. When F_O is driven by an external oscillator with a frequency f_{EOSC} , every 100Ω of source resistance driving REF^+ or REF^- translates into about $8.73 \cdot 10^{-6} \cdot f_{EOSC} ppm$ additional INL error. Figure 26 shows the typical INL error due to the source resistance driving the REF^+ or REF^- pins when large C_{REF} values are used. The effect of the source resistance on the two reference pins is additive with respect to this INL error. In general, matching of source impedance for the V_{REF+} and V_{REF-} pins does not help the gain or the INL error. The user

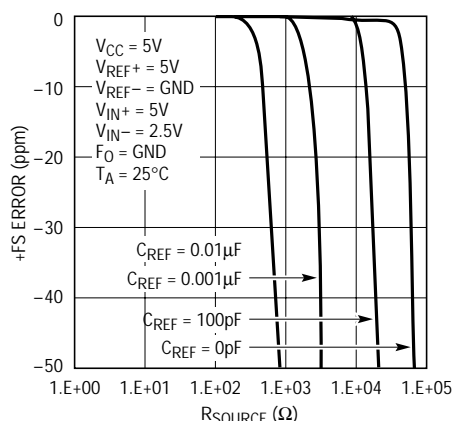
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is thus advised to minimize the combined source impedance driving the V_{REF+} and V_{REF-} pins rather than to try to match it.

The magnitude of the dynamic reference current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typical better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance

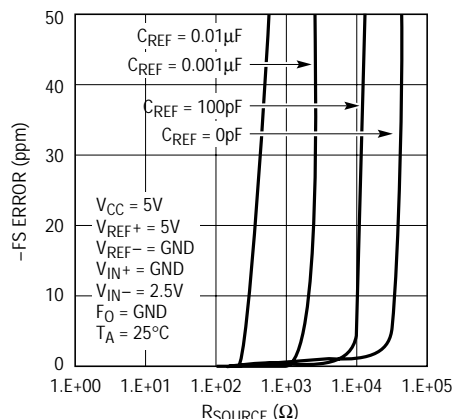
seen by V_{REF+} and V_{REF-} the expected drift of the dynamic current gain error will be insignificant (about 1% of its value over the entire temperature and voltage range). Even for the most stringent applications a one-time calibration operation may be sufficient.

In addition to the reference sampling charge, the reference pins ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (± 10 nA max), results in a small gain error. A 100 Ω source resistance will create a 0.05 μ V typical and 0.5 μ V maximum full-scale error.



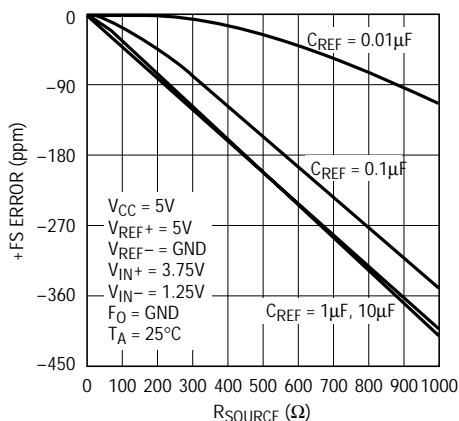
2410 F22

Figure 22. +FS Error vs R_{SOURCE} at V_{REF+} or V_{REF-} (Small C_{IN})



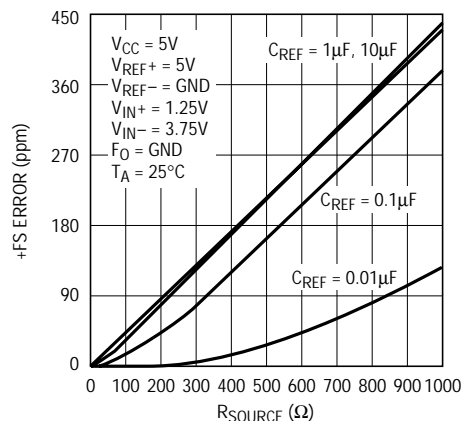
2410 F23

Figure 23. -FS Error vs R_{SOURCE} at V_{REF+} or V_{REF-} (Small C_{IN})



2410 F24

Figure 24. +FS Error vs R_{SOURCE} at V_{REF+} and V_{REF-} (Large C_{REF})



2410 F25

Figure 25. -FS Error vs R_{SOURCE} at V_{REF+} and V_{REF-} (Large C_{REF})

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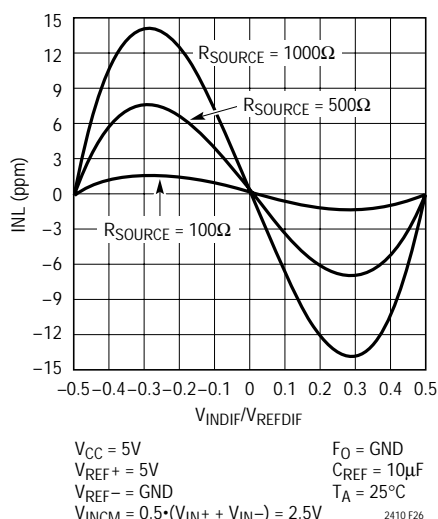


Figure 26. INL vs Differential Input Voltage ($V_{INDIF} = V_{IN+} - V_{IN-}$) and Reference Source Resistance (R_{SOURCE} at V_{REF+} and V_{REF-} for Large C_{REF} Values ($C_{REF} \geq 1\mu F$)

ANTI_ALIASING

One of the advantages delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large oversampling ratio, the LTC2410 significantly simplifies antialiasing filter requirements.

The digital filter provides very high rejection except at integer multiples of the modulator sampling frequency (f_S), see Figure 27. The modulator sampling frequency is $256 \cdot F_0$, where F_0 is the notch frequency (typically 50Hz or 60Hz). The bandwidth of signals not rejected by the digital filter is narrow ($\approx 0.2\%$) compared to the bandwidth of the frequencies rejected.

As a result of the oversampling ratio (256) and the digital filter, minimal (if any) antialias filtering is required in front of the LTC2410. If passive RC components are placed in front of the LTC2410 the input dynamic current should be considered (see Input Current section). In cases where large effective RC time constants are used, an external buffer amplifier may be required to minimize the effects of input dynamic current.

The modulator contained within the LTC2410 can handle large-signal level perturbations without saturating. Signal levels up to 40% of V_{REF} do not saturate the analog modulator. These signals are limited by the input ESD protection to 300mV below ground and 300mV above V_{CC} .

SYNCHRONIZATION OF MULTIPLE LTC2410s

Since the LTC2410's absolute accuracy (total unadjusted error) is 2.5ppm, applications utilizing multiple matched ADCs are possible.

Simultaneous Sampling with Two LTC2410s

One such application is synchronizing multiple LTC2410s, see Figure 28. The start of conversion is synchronized to the rising edge of \overline{CS} . In order to synchronize multiple LTC2410s, \overline{CS} is a common input to all the ADCs. To prevent the converters from autostarting a new conversion at the end of data output read, 31 or fewer SCK clock signals are applied to the LTC2410 instead of 32 (the 32nd falling edge would start a conversion). The exact timing and frequency for the SCK signal is not critical since it is only shifting out the data. In this case, two LTC2410's simultaneously start and end their conversion cycles under the external control of \overline{CS} .

Increasing the Output Rate Using Multiple LTC2410s

A second application uses multiple LTC2410s to increase the effective output rate by $4\times$, see Figure 29. In this case, four LTC2410s are interleaved under the control of separate \overline{CS} signals. This increases the effective output rate from 7.5Hz to 30Hz (up to a maximum of 60Hz). Additionally, the one-shot output spectrum is unfolded allowing further digital signal processing of the conversion results. SCK and SDO may be common to all four LTC2410s. The four \overline{CS} rising edges equally divide one LTC2410 conversion cycle (7.5Hz for 60Hz notch frequency). In order to synchronize the start of conversion to \overline{CS} , 31 or less SCK clock pulses must be applied to each ADC.

Both the synchronous and $4\times$ output rate applications use the external serial clock and single cycle operation with reduced data output length (see Serial Interface Timing Modes section and Figure 6). An external oscillator clock is applied commonly to the F_0 pin of each LTC2410 in order to synchronize the sampling times. Both circuits may be extended to include more LTC2410s.

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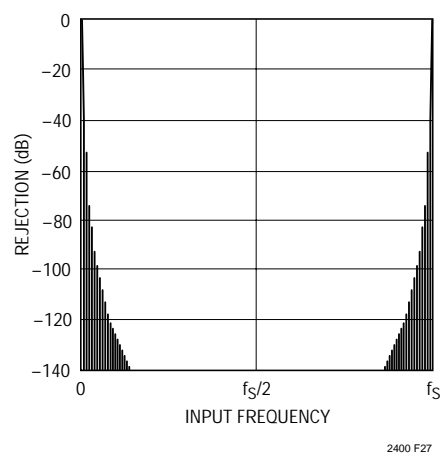


Figure 27. Sync⁴ Filter Rejection

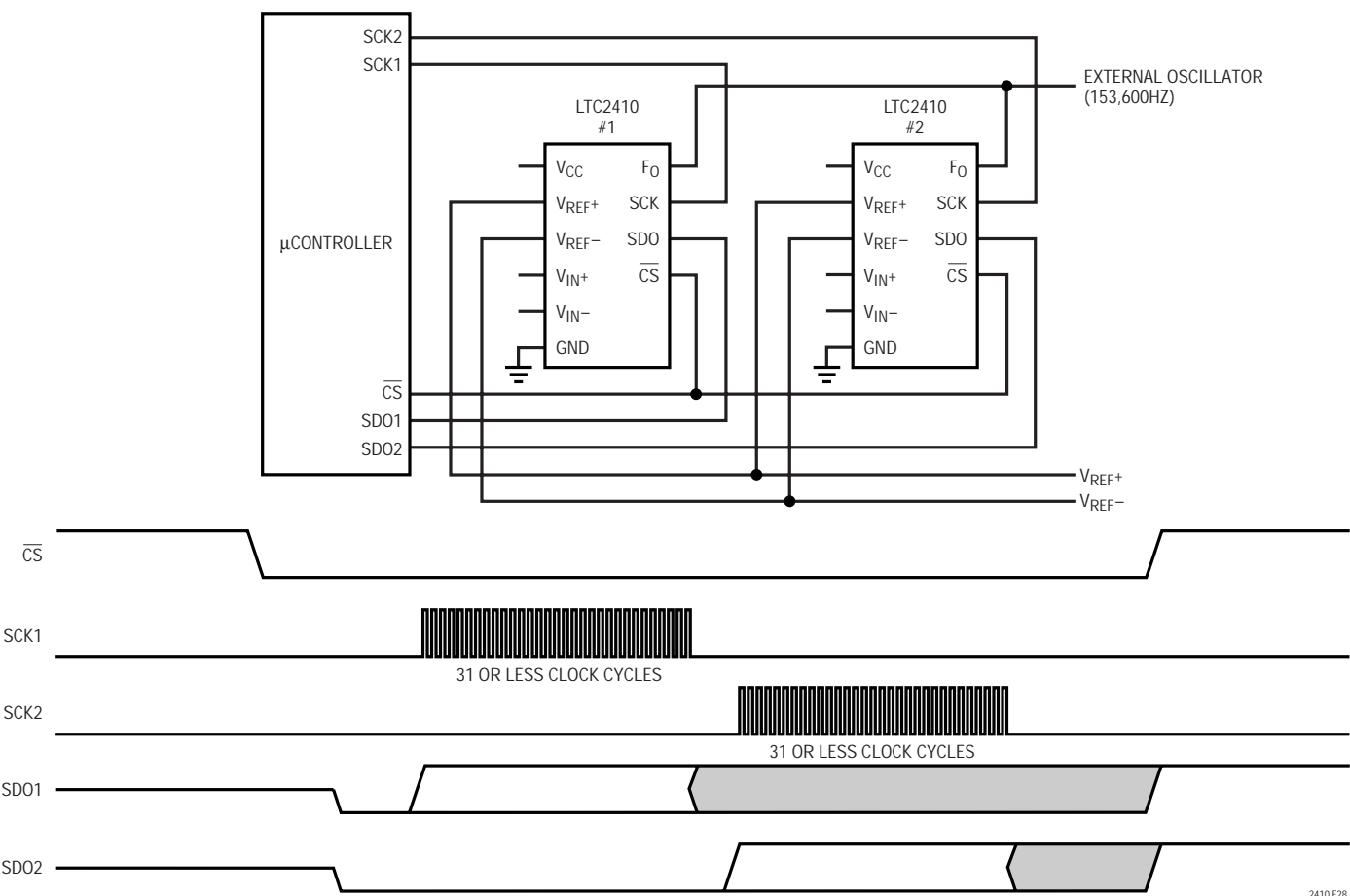


Figure 28. Synchronous Conversion—Extendable

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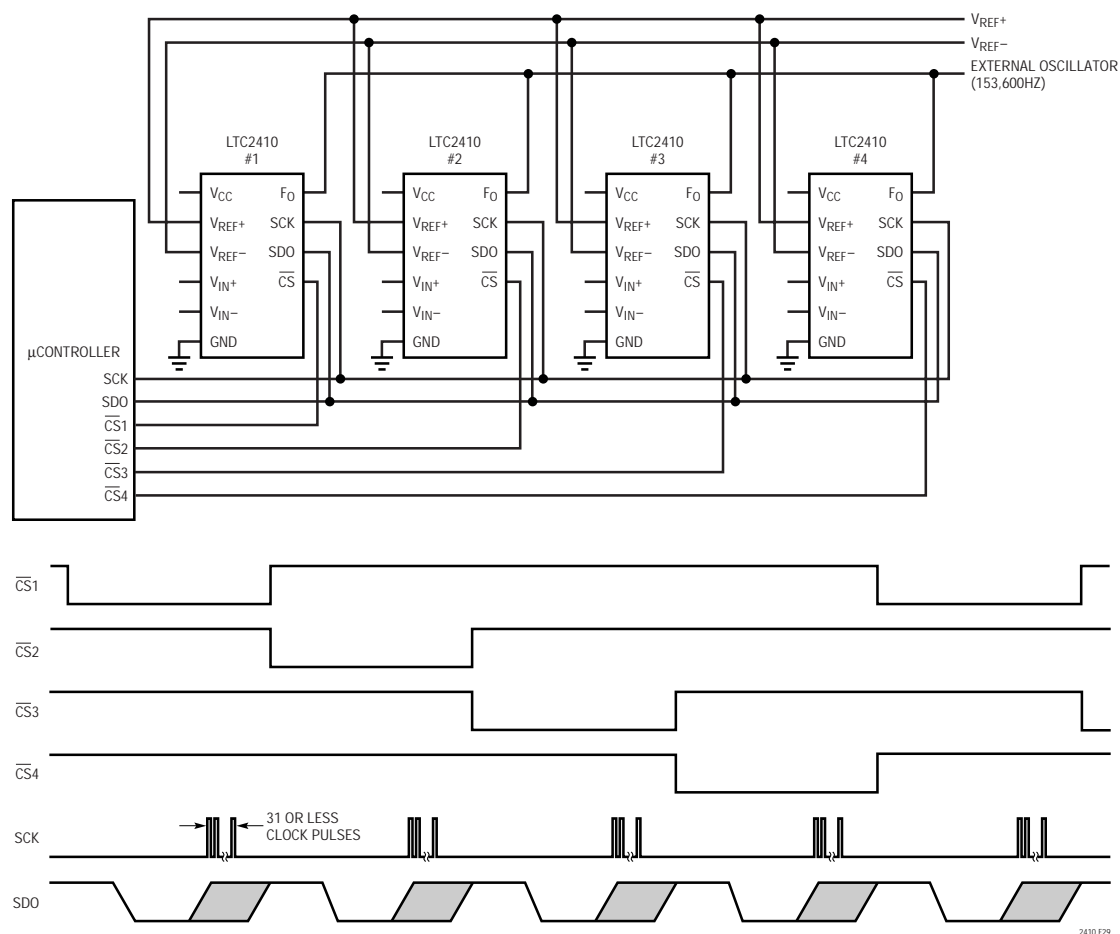


Figure 29. 4x Output Rate LTC2410 System

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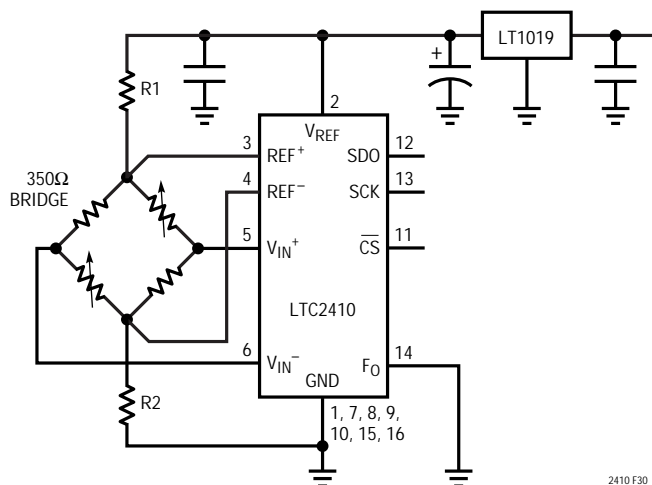
BRIDGE APPLICATIONS

At first glance, it may seem that the lack of a gain stage in the LTC2410 may make it less desirable for bridge applications than more complex parts that do incorporate gain. A second glance may tell otherwise. Typical strain gauge based bridges deliver only 2mV/Volt of excitation. As the maximum reference voltage of the LTC2410 is 5V, remote sensing of applied excitation without additional circuitry requires that excitation be limited to 5V. This gives only 10mV full scale, which can be resolved to 1 part in 10000 without averaging. For many sensors, for example most solid state sensors, this is still better than the sensor. As an example, averaging 64 samples however reduces the noise level by a factor of eight, bringing the resolving power to 1 part in 80000, comparable to better weighing systems. Hysteresis and creep effects in the load cells are typically much greater than this. Most applications that require strain measurements to this level of accuracy are measuring slowly changing phenomena, hence the time required to average a large number of readings is usually not an issue. For those systems that require accurate measurement of a small incremental change on a significant tare weight, the lack of history effects in the LTC2400 family is of great benefit.

For those applications that cannot be fulfilled by the LTC2410 alone, compensating for error in external amplification can be done effectively due to the “no latency” feature of the LTC2410. No latency operation allows samples of the amplifier offset and gain to be interleaved with weighing measurements. The use of correlated double sampling allows suppression of 1/f noise, offset and thermocouple effects within the bridge. Correlated double sampling involves alternating the polarity of excitation and dealing with the reversal of input polarity mathematically. Alternatively, bridge excitation can be increased to as much as $\pm 10V$, if one of several precision attenuation techniques is used to produce a precision divide operation on the reference signal. Another option is the use of a reference within the 5V input range of the LTC2410 and developing excitation via fixed gain, or LTC1043 based voltage multiplication, along with remote feedback in the excitation amplifiers, as shown in Figures 34 and 35.

Figure 30 shows an example of a simple bridge connection. This is the simplest example possible. Note that it is suitable for any bridge application where speed is not of the utmost importance. For many applications where large tanks or hoppers are weighed, the average weight over an extended period of time is of concern and short term weight is not readily determined due to movement of contents, or mechanical resonance. Often, large weighing applications involve load cells located at each load bearing point, the output of which can be summed passively prior to the signal processing circuitry, actively with amplification prior to the ADC, or can be digitized via multiple ADC channels and summed mathematically. The mathematical summation of the output of multiple LTC2410's provides the benefit of a root N reduction in noise. The low power consumption of the LTC2410 makes it attractive for multidrop communication schemes where the ADC is located within the load-cell housing.

A direct connection to a load cell is perhaps best incorporated into the load-cell body, as minimizing the distance to the sensor largely eliminates the need for protection devices, RFI suppression and wiring. The LTC2410 exhibits extremely low temperature dependent drift, as a result, exposure to external ambient temperature ranges does not compromise performance. The incorporation of any amplification considerably complicates the thermal stability situation, as input offset voltages and currents, temperature coefficient of gain settling resistors all become issues.



R1 AND R2 CAN BE USED TO INCREASE TOLERABLE AC COMPONENT ON REF SIGNALS

Figure 30. Simple Bridge Connection

The gain stability and accuracy of this approach is very good, due to a statistical improvement in resistor matching due to individual error contribution being reduced. Note that the gain that is produced in this case is the result of happenstance and is accepted as a reasonable gain that can be produced with a minimum error. Attempting to produce an arbitrary gain in order to make the math simpler, or in order to produce a nice round number like 50, may result in difficulty achieving a high degree of stability, as good matching between dissimilar values is less likely. A gain of 34 may seem low, when compared to common practice in earlier generations of load-cell interfaces, however the accuracy of the LTC2410 changes the rationale. Achieving high gain accuracy and linearity at higher gains may prove difficult, while providing little benefit in terms of noise reduction.

Figure 31. Differential Amplification Using Two Amplifiers

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At a gain of 100, the gain error that could result from typical open-loop gain of 160dB is –1ppm, however, worst-case is at the minimum gain of 116dB, giving a gain error of –158ppm. Worst-case gain error at a gain of 34, is –54ppm, better. The use of the LTC1051A reduces the worst-case gain error to –33ppm. The advantage of gain higher than 34, then becomes dubious, as the input referred noise sees little improvement* and gain accuracy is potentially compromised. *Input referred noise at $AV = 34$ is approximately $0.05\mu V_{RMS}$, whereas at a gain of 50, it would be $0.048\mu V$.

Note that this 2-amplifier topology has advantages over the typical integrated 3-amplifier instrumentation amplifier in that it does not have the high noise level common in the output stage that usually dominates when an instrumentation amplifier is used at low gain*. If this dual amplifier is used at a gain of 10, the gain error is only 10ppm and input referred noise is reduced to $0.1\mu V_{RMS}$. *As an example, the LT1167, has an output stage noise density of $60nV/\sqrt{Hz}$.

Figure 32 shows an example of the use of a single amplifier used to produce single ended gain. This topology is best used in instances where the gain setting resistor can be made to match the temperature coefficient of the strain gauges. If the bridge is partially composed of precision resistors, with only one or two variable elements, the reference arm of the bridge can be made to act in conjunction with the feedback resistor to determine the gain. If the feedback resistor is incorporated into the design of the load cell, using resistors which match the temperature coefficient of the load-cell elements, good results can be had without the need for resistors with a high degree of absolute accuracy. The common mode voltage in this case, is again a function of the bridge output. Differential gain as used with a 350Ω bridge is $AV = 1 + R2/(R1 + 175\Omega)$. Common mode gain is half the differential gain. The maximum differential signal that can be used is $1/4 V_{REF}$, as opposed to $1/2 V_{REF}$ in the 2-amplifier topology above.

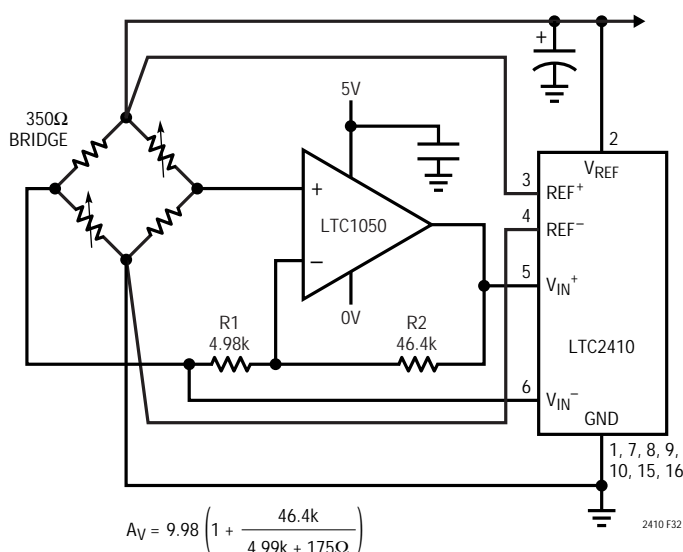


Figure 32. Bridge Amplification Using a Single Amplifier

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Remote Half Bridge Interface

As opposed to full bridge applications, typical half bridge applications must contend with nonlinearity in the bridge output, as signal swing is often much greater. Applications include RTD's, thermistors and other resistive elements that undergo significant changes over their span. For single variable element bridges, the nonlinearity of the half bridge output can be eliminated completely however if the reference arm of the bridge is used as the reference to the ADC, as shown in Figure 33. The LTC2410 can accept inputs up to $1/2 V_{REF}$, hence, the reference resistor R1 must be at least 2x the highest value of the variable resistor.

In the case of 100Ω platinum RTD's, this would suggest a value of 800Ω for R1, not advisable however due to self-heating effects. A value of 25.5k is shown for R1, reducing self-heating effects to acceptable levels for most sensors.

The basic circuit shown in Figure 33 shows connections for a full 4-wire connection to the sensor, which may be located remotely with a few caveats. The differential input connections will reject induced or coupled 60Hz interference, however, the reference inputs do not have the same rejection. If one must contend with 60Hz or other noise on the reference input, you must pass the signal through a low pass filter, which necessitates a buffer as shown in

Figure 34. Note that you cannot place a significant capacitor directly at the junction of R1 and R2, as it will store charge from the sampling process, producing errors. A better approach is to produce a low pass filter decoupled from the input lines with a high value resistor.

The use of a third resistor in the half bridge, between the variable and fixed elements gives essentially the same result as the two resistor version, but has a few benefits. If, for example, a 25k reference resistor is used to determine excitation current with a 100Ω RTD, the negative reference input is sampling the same external node, as the positive input. This is fine for instances where there is little cable capacitance associated with this node, but may result in errors if used with a long cable. If instead, the single 25k resistor is replaced with 10k 5% and a 10k 0.1% negative reference resistor, the noise level introduced at the reference, at least at higher frequencies, will be reduced. A filter can be introduced into the network, in the form of one or more capacitors, or ferrite beads, as long as the sampling pulses are not translated into error. The reference voltage is also reduced of course, but this is not undesirable, as it will decrease the value of the LSB, although, not the input referred noise level.

The circuit shown in Figure 34 shows a more rigorous example of Figure 33, with increased noise suppression and more protection for remote applications.

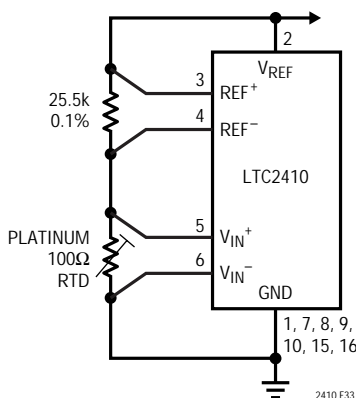


Figure 33. Remote Half Bridge Interface

APPLICATIONS INFORMATION

Figure 35 shows an example of gain in the excitation circuit and remote feedback from the bridge. The LTC1043's provide voltage multiplication, providing $\pm 10\text{V}$ from a 5V reference with only 1ppm error. The amplifiers are used at unity-gain, and hence, introduce very little error due to gain error, or due to offset voltages. $1\mu\text{V}/^\circ\text{C}$ offset voltage drift translates into $0.05\text{ppm}/^\circ\text{C}$ gain error. Simpler alternatives, with the amplifiers providing gain using resistor arrays for feedback, can produce results that are similar to bridge sensing schemes via attenuators. Note that the amplifiers must have high open-loop gain or gain error will be a source of error. The fact that input offset voltage has relatively little effect on overall error may lead one to use low performance amplifiers for this application. Note that the gain of a device such as the LF156, ($25\text{V}/\text{mV}$ over temperature) will produce an error of worst-case -180ppm at a noise gain of 3, such as would be encountered in an inverting gain of 2, to produce -10V from a 5V reference.

The error associated with the 10V excitation would be -80ppm . Hence, overall reference error could be as high as 130ppm , the average of the two.

Figure 36 shows a similar scheme to provide excitation using resistor arrays to produce precise gain. The circuit is configured to provide 10V and -5V excitation to the bridge, producing a common mode voltage at the input to the LTC2410 of 2.5V , maximizing the AC input range for applications where induced 60Hz could reach amplitudes up to 2V_{RMS} .

The last two example circuits could be used where multiple bridge circuits are involved and bridge output can be multiplexed onto a single LTC2410, via an inexpensive multiplexer such as the 74HC4052.

Figure 37 shows the use of an LTC2410, with a differential multiplexer. This is an inexpensive multiplexer that will contribute some error due to leakage if used directly with the output from the bridge, or if resistors are inserted as a protection mechanism from overvoltage. Although the bridge output may be within the input range of the A/D and multiplexer in normal operation, some thought should be given to fault conditions that could result in full excitation voltage at the inputs to the multiplexer or ADC. The use of amplification prior to the multiplexer will largely eliminate errors associated with channel leakage developing error voltages in the source impedance.

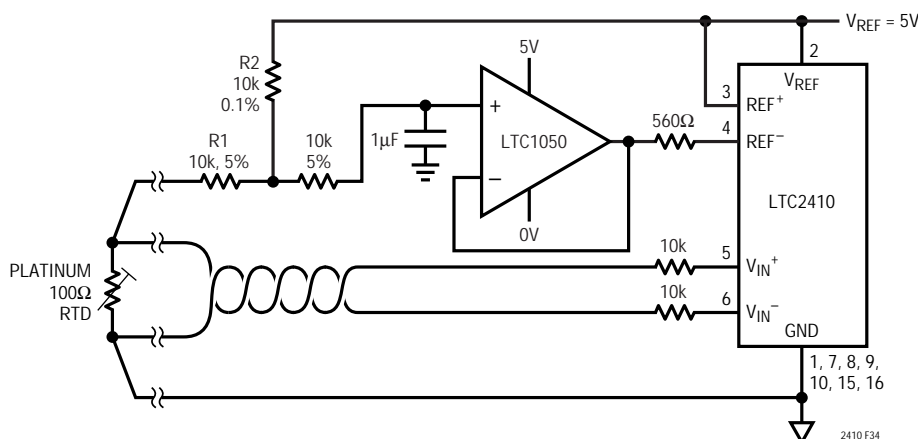


Figure 34. Remote Half Bridge Sensing with Noise Suppression on Reference

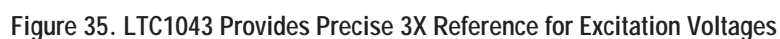




Figure 36. Use Resistor Arrays to Provide Precise Matching in Excitation Amplifier

APPLICATIONS INFORMATION

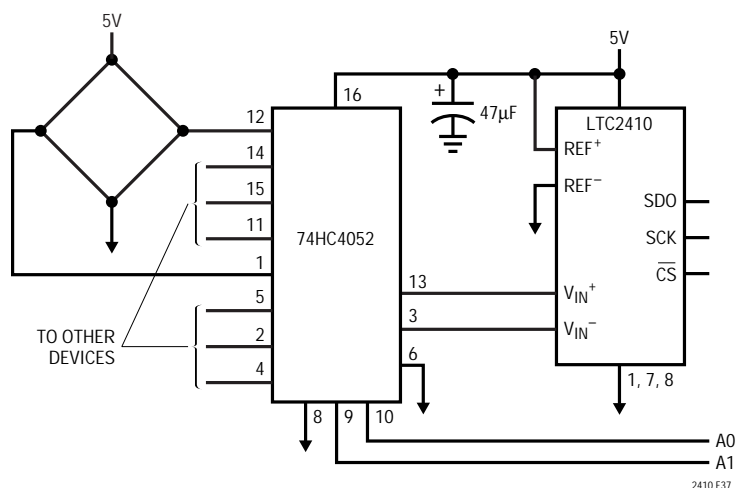
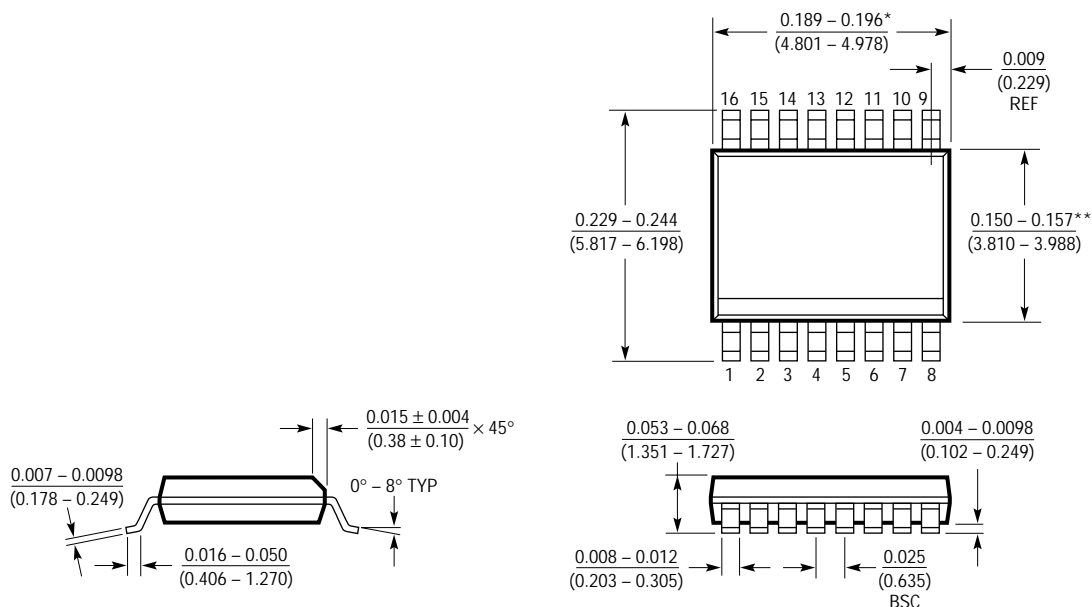


Figure 37. Use a Differential Multiplexer to Expand Channel Capability

PACKAGE INFORMATION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0398

RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|-------------|--|--|
| LTC1019 | Precision Bandgap Reference, 2.5V, 5V | 3ppm/°C Drift, 0.05% Max |
| LTC1025 | Micropower Thermocouple Cold Junction Compensator | |
| LTC1043 | Dual Precision Instrumentation Switched Capacitor Building Block | Precise Charge, Balanced Switching, Low Power |
| LTC1050 | Precision Chopper Stabilized Op Amp | No External Components 5μV Offset, 1.6μV _{p-p} Noise |
| LT1236A-5 | Precision Bandgap Reference, 5V | 0.05% Max, 5ppm/°C Drift |
| LTC1391 | 8-Channel Multiplexer | |
| LT1460 | Micropower Series Reference | 0.075% Max, 10ppm/°C Max Drift, 2.5V, 5V and 10V Versions, MSOP, PDIP, SO-8, SOT-23 and TO-92 Packages |