8-Channel 24-Bit µPower No Latency ΔΣ™ ADC

July 1999

FEATURES

- 24-Bit ADC with 8-Channel MUX
- **Single Conversion Settling Time Simplifies Multiplexing**
- **4ppm INL, No Missing Codes**
- **4ppm Full-Scale Error**
- **0.5ppm Offset**
- **0.3ppm Noise**
- Internal Oscillator—No External Components Required
- 110dB Min, 50Hz/60Hz Notch Filter
- Reference Input Voltage: 0.1V to V_{CC}
- Live Zero—Extended Input Range Accommodates 12.5% Overrange and Underrange
- Single Supply 2.7V to 5.5V Operation
- Low Supply Current (200µA) and Auto Shutdown

APPLICATIONS

- Weight Scales
- Direct Temperature Measurement
- Gas Analyzers
- Strain-Gage Transducers
- Instrumentation
- Data Acquisition
- Industrial Process Control
- 6-Digit DVMs

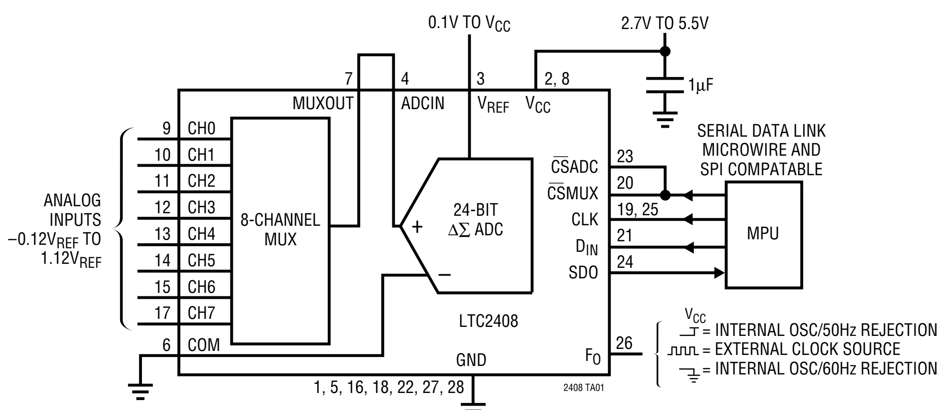
DESCRIPTION

The LTC®2408 is an 8-channel 2.7V to 5.5V micropower 24-bit converter with an integrated oscillator, a 4ppm INL and 0.3ppm RMS noise. It uses delta-sigma technology and it provides single cycle settling time (no latency delay) for multiplexed applications. The first conversion after the channel is changed is valid. Through a single pin the LTC2408 can be configured for better than 110dB rejection at 50Hz or 60Hz ±2%, or it can be driven by an external oscillator for a user defined rejection frequency in the range 1Hz to 120Hz. The internal oscillator requires no external frequency setting components.

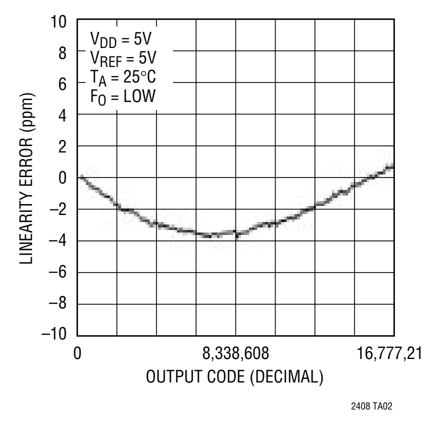
The converter accepts any external reference voltage from 0.1V to V_{CC}. With its extended input conversion range of –12.5% V_{REF} to 112.5% V_{REF} the LTC2408 smoothly resolves the offset and overrange problems of preceding sensors or signal conditioning circuits.

The LTC2408 communicates through a flexible 4-wire digital interface which is compatible with SPI and MICROWIRE™ protocols.

TYPICAL APPLICATION



Total Unadjusted Error vs Output Code

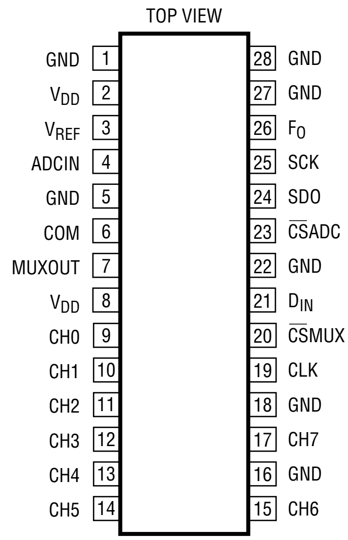


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND .... –0.3V to 7V
Analog Input Voltage to GND .... –0.3V to (V_{CC} + 0.3V)
Reference Input Voltage to GND .. –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND .... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
  LTC2408C .... 0°C to 70°C
  LTC2408I .... –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 110°C, θ_{JA} = 95°C/W

ORDER PART NUMBER
LTC2408CG LTC2408IG

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	2.5V ≤ V_{REF} ≤ V_{CC}, (Note 5)	●	24			Bits
Integral Nonlinearity	V_{REF} = 2.5V (Note 6) V_{REF} = 5V (Note 6)	● ●		2 4	10 15	ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ V_{REF} ≤ V_{CC}	●		0.5	2	ppm of V_{REF}
Offset Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}			0.01		ppm of V_{REF}/°C
Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}	●		4	10	ppm of V_{REF}
Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}			0.02		ppm of V_{REF}/°C
Total Unadjusted Error	V_{REF} = 2.5V V_{REF} = 5V			5 10		ppm of V_{REF} ppm of V_{REF}
Output Noise	V_{IN} = 0V (Note 13)			1.5		μV_{RMS}
Normal Mode Rejection 60Hz ±2%	(Note 7)	●	110	130		dB
Normal Mode Rejection 50Hz ±2%	(Note 8)	●	110	130		dB
Reference Input Rejection 60Hz ±2%	(Note 7)	●	110	130		dB
Reference Input Rejection 50Hz ±2%	(Note 8)	●	110	130		dB
Power Supply Rejection DC	V_{REF} = 2.5V, V_{IN} = 0V			100		dB
Power Supply Rejection 60Hz ±2%	V_{REF} = 2.5V, V_{IN} = 0V, (Note 7)			110		dB
Power Supply Rejection 50Hz ±2%	V_{REF} = 2.5V, V_{IN} = 0V, (Note 8)			110		dB

ANALOG INPUT AND REFERENCE

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range	(Note 14)		●	$-0.125 \bullet V_{REF}$		$1.125 \bullet V_{REF}$	V
V_{REF}	Reference Voltage Range			●	0.1		V_{CC}	V
$C_{S(IN)}$	Input Sampling Capacitance					10		pF
$C_{S(REF)}$	Reference Sampling Capacitance					15		pF
I_{IN}	Input Leakage Current	$\overline{CS} = V_{CC}$		●	–10	1	10	nA
I_{REF}	Reference Leakage Current	V_{REF} = 2.5V, $\overline{CS} = V_{CC}$		●	–10	1	10	nA
$I_{IN(MUX)}$	Multiplexer Input Leakage Current			●			±20	nA
R_{ON}	MUX On-Resistance	I_O = 1mA	V_{CC} = 2.7V	●		250	300	Ω
			V_{CC} = 5V	●		120	250	Ω
	MUXΔ R_{ON} vs Temp					0.5		%/°C
	Δ R_{ON} vs V_S (Note 15)					20		%
$I_{S(OFF)}$	MUX Off Input Leakage	Channel Off		●			±20	nA
$I_{D(OFF)}$	MUX Off Output Leakage	Channel Off		●			±20	nA
t_{OPEN}	MUX Break Before Make Interval				125	290		ns
t_{ON}	Enable Turn-On Time	V_S = 1.5V, R_L = 3.4k, C_L = 15pF				490	800	ns
t_{OFF}	Enable Turn-Off Time	V_S = 1.5V, R_L = 3.4k, C_L = 15pF				190	400	ns
QIRR	MUX Off Isolation	V_{IN} = 2V_{P-P}, R_L = 1k, f = 100kHz				70		dB
QINJ	Charge Injection	R_S = 0Ω, C_L = 1000pF, V_S = 1V				±1	±5	pC
$C_{S(OFF)}$	Input Off Capacitance (MUX)					10		pF
$C_{D(OFF)}$	Output Off Capacitance (MUX)					10		pF

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage $\overline{CS}$, F_O	2.7V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 3.3V	●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage $\overline{CS}$, F_O	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V	●			0.8 0.6	V V
V_{IH}	High Level Input Voltage SCK	2.7V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 3.3V (Note 9)	●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage SCK	4.5V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 5.5V (Note 9)	●			0.8 0.6	V V
I_{IN}	Digital Input Current $\overline{CS}$, F_O	0V ≤ V_{IN} ≤ V_{CC}	●	–10		10	µA
I_{IN}	Digital Input Current SCK	0V ≤ V_{IN} ≤ V_{CC} (Note 9)	●	–10		10	µA
C_{IN}	Digital Input Capacitance $\overline{CS}$, F_O				10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 9)			10		pF

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OH}	High Level Output Voltage SDO	I_O = –800µA	●	V_{CC} – 0.5V			V
V_{OL}	Low Level Output Voltage SDO	I_O = 1.6mA	●			0.4V	V
V_{OH}	High Level Output Voltage SCK	I_O = –800µA (Note 10)	●	V_{CC} – 0.5V			V
V_{OL}	Low Level Output Voltage SCK	I_O = 1.6mA (Note 10)	●			0.4V	V
I_{OZ}	High-Z Output Leakage SDO		●	–10		10	µA
V_{IN} H_{MUX}	MUX High Level Input Voltage	V^+ = 3V	●	2			V
V_{IN} L_{MUX}	MUX Low Level Input Voltage	V^+ = 2.4V	●			0.8	V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current Conversion Mode Sleep Mode	 $\overline{CS}$ = 0V (Note 12) $\overline{CS}$ = V_{CC} (Note 12)	 ● ●		 200 20	 300 30	 µA µA
$I_{CC(MUX)}$	Multiplexer Supply Current	All Logic Inputs Tied Together V_{IN} = 0V or 5V	●		15	40	µA

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	2.56		307.2	kHz
t_{HEO}	External Oscillator High Period		●	0.5		390	µs
t_{LEO}	External Oscillator Low Period		●	0.5		390	µs
t_{CONV}	Conversion Time	F_O = 0V F_O = V_{CC} External Oscillator (Note 11)	● ● ●	130.66 156.80	133.33 160 20480/f_{EOSC} (in kHz)	136 163.20	ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10) External Oscillator (Notes 10, 11)			19.2 $f_{EOSC}/8$		kHz kHz
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)		45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 9)	●			2000	kHz
t_{LESCK}	External SCK Low Period	(Note 9)	●	250			ns
t_{HESCK}	External SCK High Period	(Note 9)	●	250			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 10, 12) External Oscillator (Notes 10, 11)	● ●	1.64	1.67 256/f_{EOSC} (in kHz)	1.7	ms ms
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 9)	●		32/f_{ESCK} (in kHz)		ms

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_1	$\overline{CS}$ ↓ to SDO Low Z		●	0		150	ns
t2	$\overline{CS}$ ↑ to SDO High Z		●	0		150	ns
t3	$\overline{CS}$ ↓ to SCK ↓	(Note 10)	●	0		150	ns
t4	$\overline{CS}$ ↓ to SCK ↑	(Note 9)	●	50			ns
t_{KQMAX}	SCK ↓ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK ↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$ ↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$ ↓		●			50	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7 to 5.5V unless otherwise specified.

Note 4: Internal Conversion Clock source with the F_O pin tied to GND or to V_{CC} or to external conversion clock source with f_{EOSC} = 153600Hz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: F_O = 0V (internal oscillator) or f_{EOSC} = 153600Hz ±2% (external oscillator).

Note 8: F_O = V_{CC} (internal oscillator) or f_{EOSC} = 128000Hz ±2% (external oscillator).

Note 9: The converter is in External SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the Data Output is f_{ESCK} and is expressed in kHz.

Note 10: The converter is in Internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the SCK pin has a total equivalent load capacitance C_{LOAD} = 20pF.

Note 11: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses the internal oscillator. F_O = 0V or F_O = V_{CC}.

Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: For reference voltage values V_{REF} > 2.5V the extended input of –0.125 • V_{REF} to 1.125 • V_{REF} is limited by the absolute maximum rating of the Analog Input Voltage pin (Pin 3). For 2.5V < V_{REF} ≤ 0.267V + 0.89 • V_{CC} the Input Voltage Range is –0.3V to 1.125 • V_{REF}. For 0.267V + 0.89 • V_{CC} < V_{REF} ≤ V_{CC} the Input Voltage Range is –0.3V to V_{CC} + 0.3V.

Note 15: V_S is the voltage applied to a channel input.

PIN FUNCTIONS

GND (Pins 1, 5, 16, 18, 22, 27, 28): Ground. Shared pin for analog ground, digital ground and reference ground. Should be connected directly to a ground plane through a minimum length trace or it should be the single-point-ground in a single point grounding system.

V_{CC} (Pins 2, 8): Positive Supply Voltage. Bypass to GND with a 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitor as close to the part as possible.

V_{REF} (Pin 3): Reference Input. The reference voltage range is 0.1V to V_{CC}.

ADCIN (Pin 4): Analog Input. The input voltage range is $-0.125 \bullet V_{REF}$ to $1.125 \bullet V_{REF}$. For $V_{REF} > 2.5V$ the input voltage range may be limited by the pin absolute maximum rating of $-0.3V$ to $V_{CC} + 0.3V$.

COM (Pin 6): Signal Ground. Should be connected directly to a ground plane through minimum length trace.

MUXOUT (Pin 7): MUX Output. This pin is the output of the multiplexer. Tie to ADCIN for normal operation.

CH0 (Pin 9): Analog Multiplexer Input

CH1 (Pin 10): Analog Multiplexer Input

CH2 (Pin 11): Analog Multiplexer Input

CH3 (Pin 12): Analog Multiplexer Input

CH4 (Pin 13): Analog Multiplexer Input

CH5 (Pin 14): Analog Multiplexer Input

CH6 (Pin 15): Analog Multiplexer Input

CH7 (Pin 17): Analog Multiplexer Input

CLK (Pins 19, 25): Shift Clock. This clock synchronizes the serial data transfer to both MUX and ADC. This signal must be low on $\overline{\text{A}}$DC CS high-to-low transition.

$\overline{\text{CS}}$MUX (Pin 20): MUX Chip Select Input. A logic high on this input allows the MUX to receive a channel address. A logic low enables the selected MUX channel and connects it to the MUXOUT pin for A/D conversion. For normal operation, drive this pin in parallel with $\overline{\text{CS}}$ADC.

D_{IN} (Pin 21): Digital Data Input. The multiplexer address is shifted into this input.

$\overline{\text{CS}}$ADC (Pin 23): Active Low Digital Input. A low on this pin enables the SDO digital output. Following each conversion the ADC automatically enters the Sleep mode and remains in this low power state as long as $\overline{\text{CS}}$ is high. A low on $\overline{\text{CS}}$ wakes up the ADC. A high on this pin disables the SDO digital output. A low-to-high transition on $\overline{\text{CS}}$ during the Data Output state aborts the data transfer and starts a new conversion.

SDO (Pin 24): Three-State Digital Output. During the data output period this pin is used for serial data output. When the chip select $\overline{\text{CS}}$ is high ($\overline{\text{CS}} = V_{CC}$) the SDO pin is in a high impedance state. During the Conversion and Sleep periods this pin can be used as a conversion status output. The conversion status can be observed by pulling $\overline{\text{CS}}$ low.

F_O (Pin 26): Digital input which controls the ADC's notch frequencies and conversion time. When the F_O pin is connected to V_{CC} ($F_O = V_{CC}$) the converter uses its internal oscillator and the digital filter first null is located at 50Hz. When the F_O pin is connected to GND (F_O = 0V) the converter uses its internal oscillator and the digital filter first null is located at 60Hz. When F_O is driven by an external clock signal with a frequency f_{EOSC} the converter uses this signal as its clock and the digital filter first null is located at a frequency $f_{EOSC}/2560$.

APPLICATIONS INFORMATION

Figure 1 shows the timing diagram of a typical conversion sequence. $\overline{CS}$, tied to $\overline{CSADC}$ and $\overline{CSMUX}$, is high during MUX channel selection. The CLK pin shifts data into the MUX for channel selection. Data is shifted through the D_{IN} pin on the rising edge of CLK. Table 1 shows the bit combinations for channel selection. In order to enable the multiplexer output, $\overline{CS}$ must first be pulled low. The multiplexer should be programmed after the previous conversion is complete. In order to guarantee the conversion is complete, the multiplexer addressing should be delayed a minimum t_{CONV} (≈135ms for 60Hz notch) after the data out is read. To ensure proper operation, CLK should be low on the falling edge of $\overline{CS}$.

While the multiplexer is being programmed, the ADC is in a low power sleep state. Once MUX addressing is complete, the data from the preceeding conversion can be read. A new conversion cycle is initiated following the data read cycle with the analog input tied to the newly selected channel.

Data is shifted out the SDO pin under the control of CLK. This data may be latched on the rising edge of CLK. After 32 clock cycles, SDO goes high indicating a new conversion is beginning. If $\overline{CS}$ remains low the previous multiplexer channel remains selected. A new channel can be selected by pulling $\overline{CS}$ high and shifting data into the D_{IN} pin after time t_{CONV} as described above. Since the LTC2408 has a single cycle settling time, a new channel may be selected each conversion cycle. There is no latency or delay associated with each conversion result. Each conversion is statistically independent of the previous one regardless of which channel is selected.

Table 1. Logic Table for Channel Selection

CHANNEL STATUS	EN	D2	D1	D0
All Off	0	X	X	X
CH0	1	0	0	0
CH1	1	0	0	1
CH2	1	0	1	0
CH3	1	0	1	1
CH4	1	1	0	0
CH5	1	1	0	1
CH6	1	1	1	0
CH7	1	1	1	1

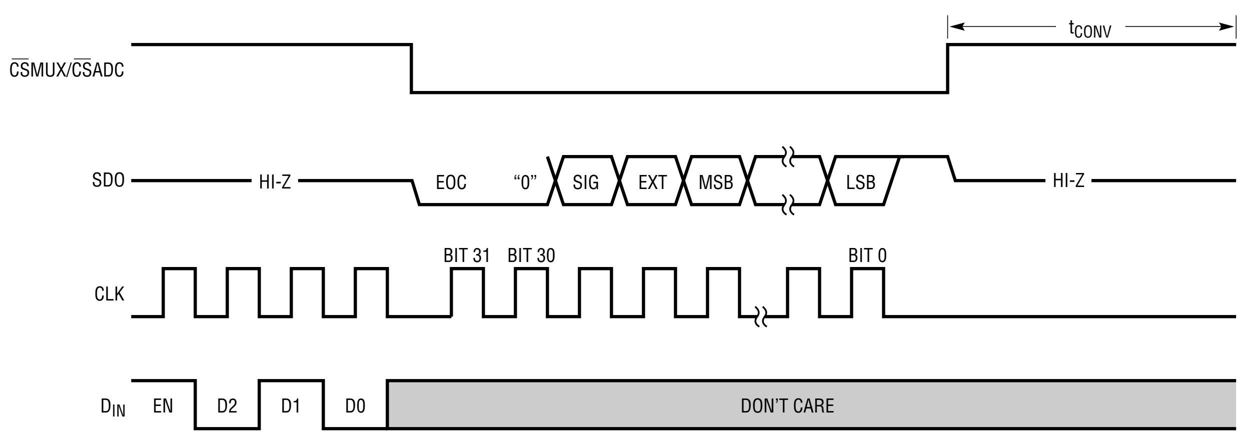


Figure 1. Typical Conversion Sequence

APPLICATIONS INFORMATION

An 8-Channel DC-to-Daylight Digitizer

The circuit in Figure 2 shows an example of the LTC2408's flexibility in digitizing a number of real-world physical phenomena—from DC voltages to ultraviolet light. All of the examples implement single-ended signal conditioning. Although differential signal conditioning is a preferred approach in applications where the sensor is a bridge-type, is located some distance from the ADC or operates in a high ambient noise environment, the LTC2408's low power dissipation allows circuit operation in close proximity to the sensor. As a result, conditioning the sensor output can be greatly simplified through the use of single-ended arrangements. In those applications where differential signal conditioning is required, chopper amplifier-based or self-contained instrumentation amplifiers (also available from LTC) can be used with the LTC2408.

With the resistor network connected to CH0, the LTC2408 is able to measure DC voltages from 1mV to 1kV in a single range without the need for autoranging. The 990k resistor should be a 1W resistor rated for high voltage operation. Alternatively, the 990k resistor can be replaced with a series connection of several lower cost, lower power metal film resistors.

The circuit connected to CH1 shows an LT1793 FET input operational amplifier used as an electrometer for high impedance, low frequency applications such as measuring pH. The circuit has been configured for a gain of 21; thus, the input signal range is $-15mV \leq V_{IN} \leq 250mV$. An amplifier circuit is necessary in these applications because high output impedance sensors cannot drive switched-capacitor ADCs directly. The LT1793 was chosen for its low input bias current (10pA, max) and low noise ($8nV/\sqrt{Hz}$) performance. As shown, the use of a driven guard (and Teflon™ standoffs) is recommended in high impedance sensor applications; otherwise, PC board surface leakage current effects can degrade results.

Teflon is a trademark of Dupont Company.

APPLICATIONS INFORMATION

The circuit connected to CH2 illustrates a precision half-wave rectifier that uses the LTC2408's internal $\Delta\Sigma$ ADC as an integrator. This circuit can be used to measure 60Hz, 120Hz or from 400Hz to 1kHz with good results. The LTC2408's internal $sinc^4$ filter effectively eliminates any frequency in this range. Above 1kHz, limited amplifier gain-bandwidth product and transient overshoot behavior can combine to degrade performance. The circuit's dynamic range is limited by operational amplifier input offset voltage and the system's overall noise floor. Using an LTC1050 chopper-stabilized operational amplifier with a V_{OS} of 5µV, the dynamic range of this application covers approximately 5 orders of magnitude. The circuit configuration is best implemented with a precision, 3-terminal, 2-resistor 10k network (for example, an IRC PFC-D network) for R6 and R7 to maintain gain and temperature stability. Alternatively, discrete resistors with 0.1% initial tolerance and 5ppm/°C temperature coefficient would also be adequate for most applications.

Two channels (CH3 and CH4) of the LTC2408 are used to accommodate a 3-wire 100Ω, Pt RTD in a unique circuit that allows true RMS/RF signal power measurement from audio to gigahertz (GHz) frequencies. The unique feature of this circuit is that the signal power dissipated in the 50Ω termination in the form of heat is measured by the 100Ω RTD. Two readings are required to compensate for the RTD's lead-wire resistance. The reading on CH4 is multiplied by 2 and subtracted from the reading on CH3 to determine the exact value of the RTD.

While the LTC2408 is capable of measuring signals over a range of six decades, the implementation (mechanical, electrical and thermal) of this technique ultimately determines the performance of the circuit. The thermal resistance of the assembly (the 50Ω/RTD mass to its enclosure) will determine the sensitivity of the circuit. The dynamic range of the circuit will be determined by the maximum temperature the assembly is rated to withstand, approximately 850°C. Details of the implementation are quite involved and are beyond the scope of this document. Please contact LTC directly for a more comprehensive treatment of this implementation.

APPLICATIONS INFORMATION

In the circuit connected to the LTC2408's CH5 input, a thermistor is configured in a half-bridge arrangement that could be used to measure the case temperature of the RTD-based thermal power measurement scheme described above. In general, thermistors yield very good resolution over a limited temperature range. Measurement resolution of 0.001°C is possible; however, thermistor self-heating effects, thermistor initial tolerance and circuit thermal construction can combine to limit achievable resolution. For the half-bridge arrangement shown, the LTC2408 can measure temperature changes over 5 orders of magnitude.

Connected to the LTC2408's CH6 input, an infrared thermocouple (Omega Engineering OS36-1) can be used in limited range, noncontact temperature measurement applications or applications where high levels of infrared light must be measured. Given the LTC2408's $0.3ppm_{RMS}$ noise performance, measurement resolution using infrared thermocouples is approximately 0.03°C—equivalent to the resolution of a conventional Type J thermocouple. These infrared thermocouples are self-contained: 1) they do not require external cold junction compensation; 2) they cannot use conventional open thermocouple detection schemes; and 3) their output impedances are high, approximately 3kΩ. Alternatively, conventional thermocouples can be connected directly to the LTC2408 (not shown) and cold junction compensation can be provided by an external temperature sensor connected to a different channel (see the thermistor circuit on CH5) or by using the LT1025, a monolithic cold-junction compensator IC.

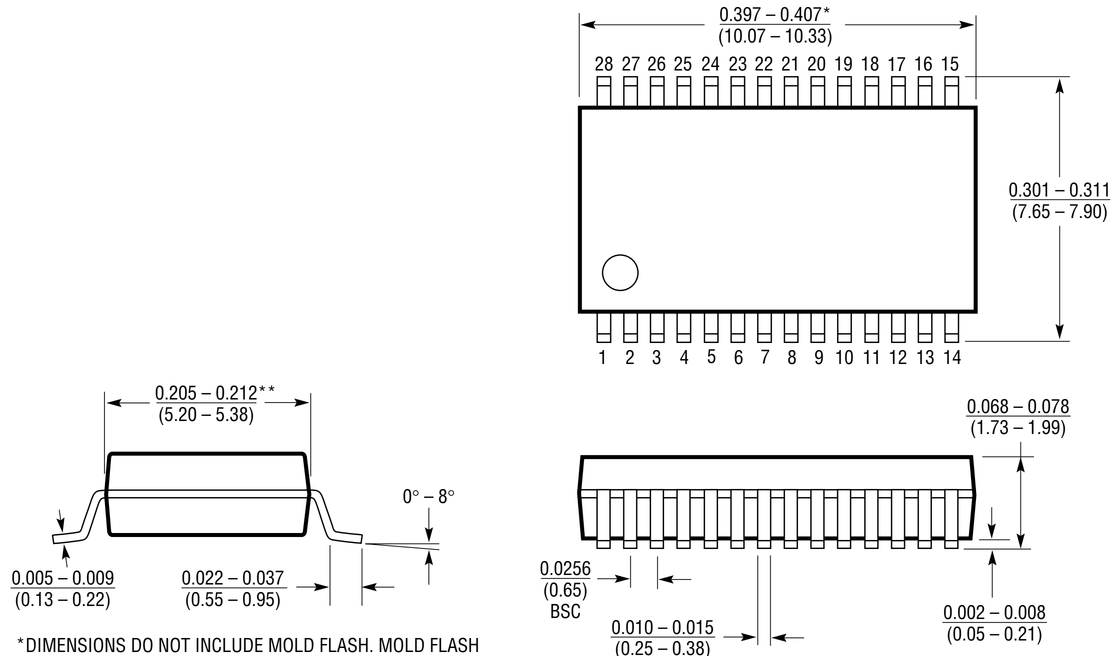
The components connected to CH7 are used to sense daylight or photodiode current with a resolution of 300pA. In the figure, the photodiode is biased in photoconductive mode; however, the LTC2408 can accommodate either photovoltaic or photoconductive configurations. The photodiode chosen (Hammatsu S1336-5BK) produces an output of 500mA per watt of optical illumination. The output of the photodiode is dependent on two factors: active detector area (2.4mm • 2.4mm) and illumination intensity. With the 5k resistor, optical intensities up to $368W/m^2$ at 960nM (direct sunlight is approximately $1000W/m^2$) can be measured by the LTC2408. With a resolution of 300pA, the optical dynamic range covers 6 orders of magnitude.

The application circuits shown connected to the LTC2408 demonstrate the mix-and-match capabilities of this multiplexed-input, high resolution ΔΣ ADC. Very low level signals and high level signals can be accommodated with a minimum of additional circuitry.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)

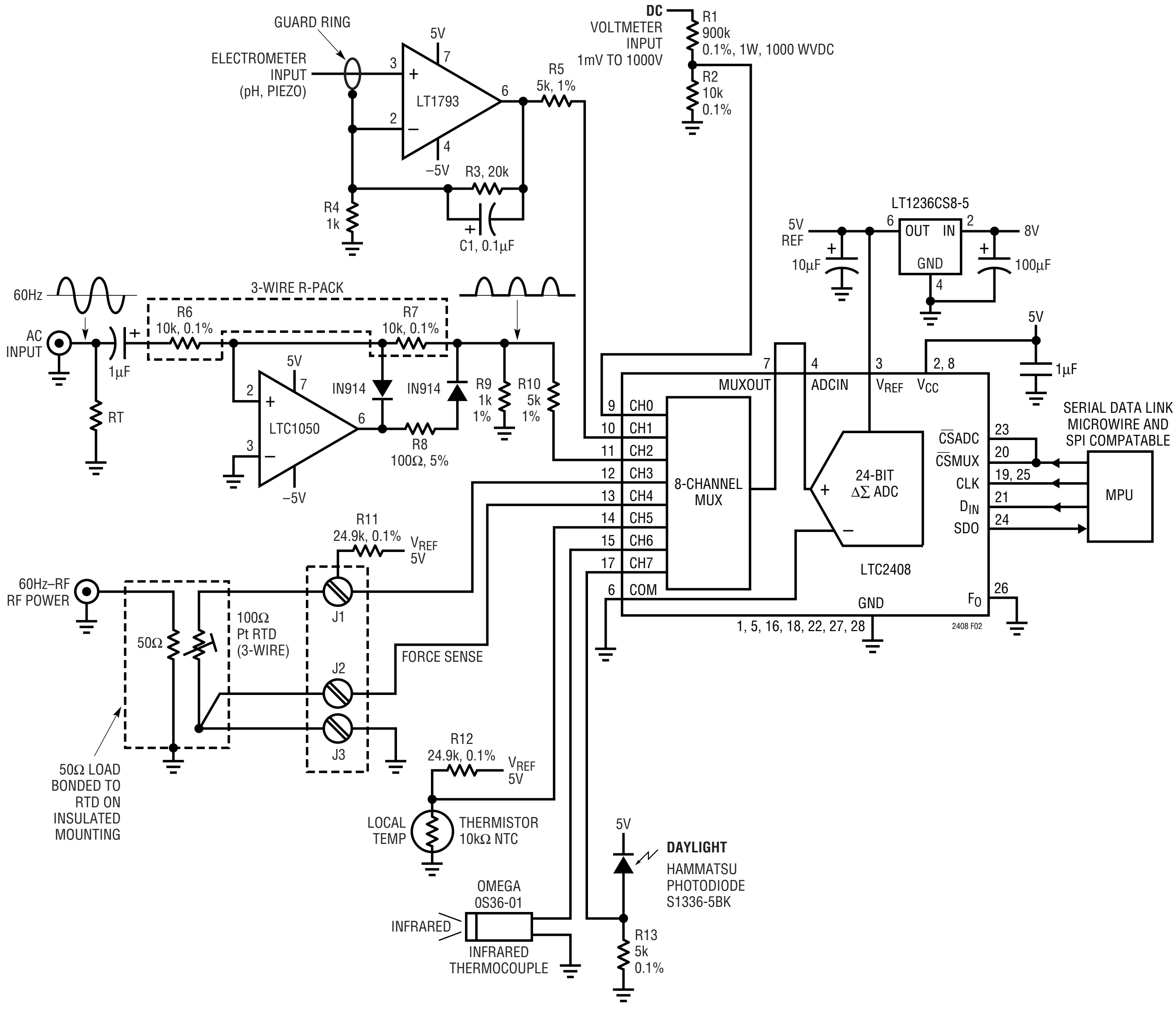


*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

G28 SSOP 0694

TYPICAL APPLICATION



Fiugre 2. Measure DC to Daylight Using the LTC2408

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1050	Precision Chopper Stabilized Op Amp	No External Components, 5µV Offset, 1.6µV_{P-P}
LTC1236	Precision Bandgap Reference	0.05% Max Initial Accuracy, 5ppm/°C Drift
LT1793	Low Noise JFET Input Op Amp	10pA Max Input Bias Current, Low Voltage Noise: 8nV
LTC2400	24-Bit Micropower ΔΣ ADC in SO-8	<1ppm INL, No Missing Codes, 4ppm Full Scale

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com
2408i LT/TP 0799 • PRINTED IN USA