LT1884

Dual Rail-to-Rail Output, Picoamp Input Precision Op Amp

January 2000

FEATURES

- **Offset Voltage: 80μV Maximum**
- **Input Bias Current: 900pA Maximum**
- **Offset Voltage Drift: 0.8μV/°C Maximum**
- Rail-to-Rail Output Swing
- Open-Loop Voltage Gain: 1 Million Minimum
- Operates with Single or Split Supplies
- 1mA Maximum Supply Current Per Amplifier
- Slew Rate: 1V/μs
- Standard Pinouts

APPLICATIONS

- Thermocouple Amplifiers
- Bridge Transducer Conditioners
- Instrumentation Amplifiers
- Battery-Powered Systems
- Photo Current Amplifiers

DESCRIPTION

The LT®1884 dual op amp brings high accuracy input performance to amplifiers with rail-to-rail output swing and faster response than other precision amplifiers. Input offset voltage is trimmed to less than 80μV and the low drift maintains this accuracy over the operating temperature range. Input bias currents are an ultralow 900pA maximum.

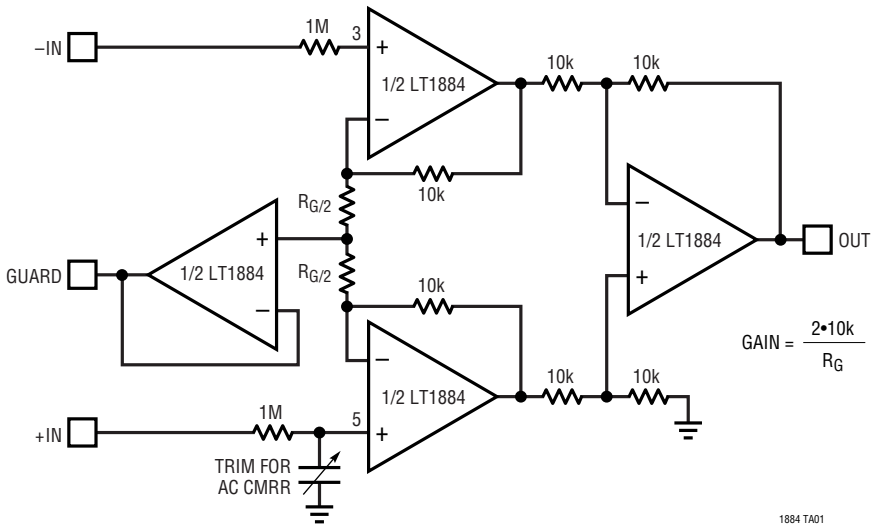
The amplifiers work on any total power supply voltage between 2.7V and 36V (fully specified from 5V to ±15V). Output voltage swings to within 40mV of the negative supply and 220mV of the positive supply make these amplifiers good choices for low voltage single supply operation.

Slew rates of 1V/μs with a supply current of less than 1mA per amplifier gives superior response and settling time performance in a low power precision amplifier.

The LT1884 is available with standard pinouts in SO-8 and DIP packages.

TYPICAL APPLICATION

Input Fault Protected Instrumentation Amplifier

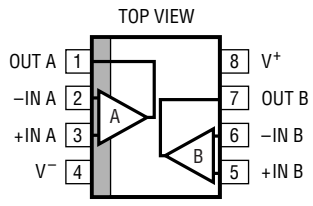


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V^+ to V^-) 40V
Differential Input Voltage (Note 2) ..... ±10V
Input Voltage ..... V^+ to V^-
Input Current (Note 2) ..... ±10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4) .. –40°C to 85°C
Specified Temperature Range (Note 5) ... –40°C to 85°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 190°C/W (S8)

ORDER PART NUMBER
LT1884CN8 LT1884IN8 LT1884CS8 LT1884IS8
S8 PART MARKING
1884 1884I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Single supply operation V_{EE} = 0, V_{CC} = 5V; V_{CM} = V_{CC}/2 unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage				30	80	µV
		0°C < T_A < 70°C	●			125	µV
		–40°C < T_A < 85°C	●			150	µV
	Input Offset Voltage Drift (Note 6)	0°C < T_A < 70°C	●		0.3	0.8	µV/°C
		–40°C < T_A < 85°C	●		0.3	0.8	µV/°C
I_{OS}	Input Offset Current				150	900	pA
		0°C < T_A < 70°C	●			1200	pA
		–40°C < T_A < 85°C	●			1400	pA
I_B	Input Bias Current				150	900	pA
		0°C < T_A < 70°C	●			1200	pA
		–40°C < T_A < 85°C	●			1400	pA
	Input Noise Voltage	0.1Hz to 10Hz			0.4		μV_{P-P}
e_n	Input Noise Voltage Density	f = 1kHz			9.5		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 1kHz			0.05		$pA/\sqrt{Hz}$
V_{CM}	Input Voltage Range			V_{EE} + 1.0		V_{CC} – 1.0	V
			●	V_{EE} + 1.2		V_{CC} – 1.2	V
CMRR	Common Mode Rejection Ratio	1V < V_{CM} < 4V		108	128		dB
		1.2V < V_{CM} < 3.8V	●	106			dB
PSRR	Power Supply Rejection Ratio	V_{EE} = 0, V_{CM} = 1.5V; 2.7V < V_{CC} < 36V	●	108	132		dB
	Minimum Operating Supply Voltage		●		2.4	2.7	V
A_{VOL}	Large-Signal Voltage Gain	R_L = 10k; 1V < V_{OUT} < 4V		500	1600		V/mV
			●	350			V/mV
		R_L = 2k; 1V < V_{OUT} < 4V		400	800		V/mV
			●	300			V/mV
		R_L = 1k; 1V < V_{OUT} < 4V		300	400		V/mV
			●	200			V/mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Single supply operation V_{EE} = 0, V_{CC} = 5V; V_{CM} = 2.5V unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Output Voltage Swing Low	No Load	●		20	40	mV
		I_{SINK} = 100µA	●		25	50	mV
		I_{SINK} = 1mA	●		70	150	mV
		I_{SINK} = 5mA	●		270	600	mV
V_{OH}	Output Voltage Swing High (Referred to V_{CC})	V_{CC} = 5V; No Load	●		120	220	mV
		V_{CC} = 5V; I_{SOURCE} = 100µA	●		130	230	mV
		V_{CC} = 5V; I_{SOURCE} = 1mA	●		180	300	mV
		V_{CC} = 5V; I_{SOURCE} = 5mA	●		360	600	mV
I_S	Supply Current Per Amplifier	V_{CC} = 3V			0.65	0.85	mA
			●			1.3	mA
		V_{CC} = 5V			0.65	0.9	mA
			●			1.4	mA
		V_{CC} = 12V			0.70	1.0	mA
			●			1.5	mA
I_{SC}	Short-Circuit Current	V_{OUT} Short to GND	●	15	30		mA
		V_{OUT} Short to V_{CC}	●	15	30		mA
GBW	Gain-Bandwidth Product	f = 20kHz		1.2	2		MHz
t_S	Settling Time	0.01%, V_{OUT} = 1.5V to 3.5V, A_V = –1, R_L = 2k			10		µs
SR^+	Slew Rate Positive	A_V = –1		0.45	0.7		V/µs
			●	0.36			V/µs
SR^-	Slew Rate Negative	A_V = –1		0.35	0.55		V/µs
			●	0.25			V/µs
ΔV_{OS}	Offset Voltage Match	(Note 6)			35	125	µV
		0°C < T_A < 70°C	●			195	µV
		–40°C < T_A < 85°C	●			235	µV
	Offset Voltage Match Drift	(Notes 6, 7)	●		0.4	1.2	µV/°C
ΔI_{B+}	Noninverting Bias Current Match	(Notes 7, 9)			250	1200	pA
		0°C < T_A < 70°C	●			1600	pA
		–40°C < T_A < 85°C	●			1900	pA
ΔCMRR	Common Mode Rejection Match	(Notes 7, 9)	●	104	125		dB
ΔPSRR	Positive Power Supply Rejection Match	V_{EE} = 0V, V_{CM} = 1.5V, 2.7V < V_{CC} < 36V, (Notes 7, 9)	●	104	126		dB

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Split supply operation V_S = ±15V, V_{CM} = 0V unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage				30	80	µV
		0°C < T_A < 70°C	●			125	µV
		–40°C < T_A < 85°C	●			150	µV
	Input Offset Voltage Drift (Note 4)	0°C < T_A < 70°C	●		0.3	0.8	µV/°C
		–40°C < T_A < 85°C	●		0.3	0.8	µV/°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Split supply operation V_S = ±15V, V_{CM} = 0V unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{OS}	Input Offset Current				150	900	pA
		0°C < T_A < 70°C	●			1200	pA
		–40°C < T_A < 85°C	●			1400	pA
I_B	Input Bias Current				150	900	pA
		0°C < T_A < 70°C	●			1200	pA
		–40°C < T_A < 85°C	●			1400	pA
	Input Noise Voltage	0.1Hz to 10Hz			0.4		μV_{P-P}
e_n	Input Noise Voltage Density	f = 1kHz			9.5		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 1kHz			0.05		$pA/\sqrt{Hz}$
V_{CM}	Input Voltage Range			V_{EE} + 1.0		V_{CC} – 1.0	V
			●	V_{EE} + 1.2		V_{CC} – 1.2	V
CMRR	Common Mode Rejection Ratio	–13.5V < V_{CM} < 13.5V	●	114	130		dB
+PSRR	Positive Power Supply Rejection Ratio	V_{EE} = –15, V_{CM} = 0; 1.5V < V_{CC} < 18V	●	114	132		dB
–PSRR	Negative Power Supply Rejection Ratio	V_{CC} = 15, V_{CM} = 0; –1.5V < V_{EE} < –18V	●	106	132		dB
	Minimum Operating Supply Voltage		●		±1.2	±1.35	V
A_{VOL}	Large-Signal Voltage Gain	R_L = 10k; –13.5V < V_{OUT} < 13.5V		1000	1600		V/mV
			●	700			V/mV
		R_L = 2k; –13.5V < V_{OUT} < 13.5V		250	420		V/mV
			●	175			V/mV
		R_L = 1k; –12V < V_{OUT} < 12V		100	230		V/mV
			●	75			V/mV
V_{OL}	Output Voltage Swing Low (Referred to V_{EE})	No Load	●		20	40	mV
		I_{SINK} = 100µA	●		25	50	mV
		I_{SINK} = 1mA	●		70	150	mV
		I_{SINK} = 5mA	●		270	600	mV
V_{OH}	Output Voltage Swing High (Referred to V_{CC})	No Load	●		160	220	mV
		I_{SOURCE} = 100µA	●		160	230	mV
		I_{SOURCE} = 1mA	●		180	300	mV
		I_{SOURCE} = 5mA	●		360	600	mV
I_S	Supply Current Per Amplifier	V_S = ±15V			0.85	1.1	mA
			●			1.6	mA
I_{SC}	Short-Circuit Current	V_{OUT} Short to V_{EE}	●	15	50		mA
		V_{OUT} Short to V_{CC}	●	15	30		mA
GBW	Gain-Bandwidth Product	f = 20kHz		1.5	2.2		MHz
t_S	Settling Time	0.01%, V_{OUT} = –5V to 5V, A_V = –1, R_L = 2k			17		µs
SR^+	Slew Rate Positive	A_V = –1		0.5	1		V/µs
			●	0.4			V/µs
SR^-	Slew Rate Negative	A_V = –1		0.4	0.7		V/µs
			●	0.32			V/µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Split supply operation V_S = ±15V, V_{CM} = 0V unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔV_{OS}	Offset Voltage Match	(Note 7)			35	125	µV
		0°C < T_A < 70°C	●			175	µV
		–40°C < T_A < 85°C	●			235	µV
	Offset Voltage Match Drift	(Notes 6, 7)	●		0.4	1.1	µV/°C
ΔI_{B+}	Noninverting Bias Current Match	(Notes 7, 8)			240	1200	pA
		0°C < T_A < 70°C	●			1600	pA
		–40°C < T_A < 85°C	●			1900	pA
ΔCMRR	Common Mode Rejection Match	(Notes 7, 9)	●	106	125		dB
Δ+PSRR	Positive Power Supply Rejection Match	V_{EE} = –15V, V_{CM} = 0V, 1.5V < V_{CC} < 18V, (Notes 7, 9)	●	108	124		dB
Δ–PSRR	Negative Power Supply Rejection Match	V_{CC} = 15V, V_{CM} = 0V, –1.5V < V_{EE} < –18V, (Notes 7, 9)	●	102	132		dB

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The inputs are protected by internal resistors and back-to-back diodes. If the differential input voltage exceeds ±0.7V, the input current should be limited externally to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum.

Note 4: The LT1884C and LT1884I are guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 5: The LT1884C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. LT1884I is guaranteed to meet specified performance from –40°C to 85°C.

Note 6: This parameter is not 100% tested.

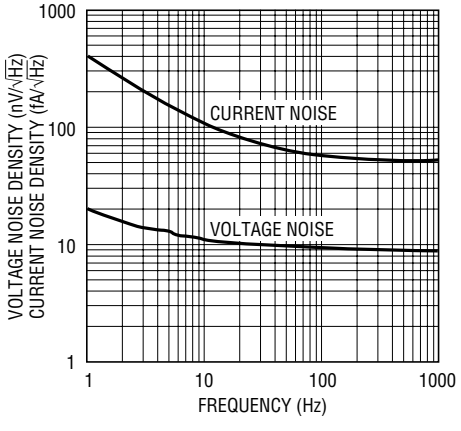
Note 7: Matching parameters are the difference between amplifiers A and B.

Note 8: This parameter is the difference between the two noninverting input bias currents.

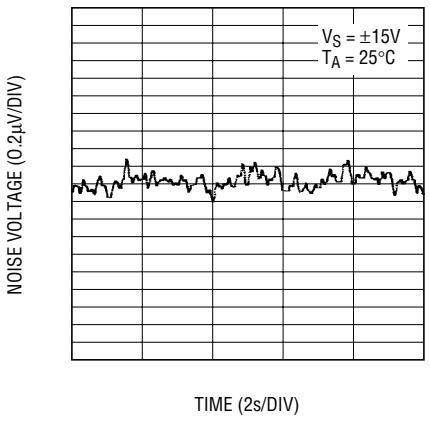
Note 9: ΔCMRR and ΔPSRR are defined as follows: CMRR and PSRR are measured in µV/V on each amplifier. The difference is calculated in µV/V and then converted to dB.

TYPICAL PERFORMANCE CHARACTERISTICS

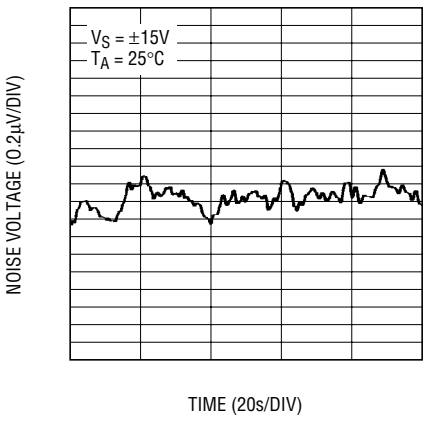
V_n, I_n vs Frequency



0.1Hz to 10Hz Noise

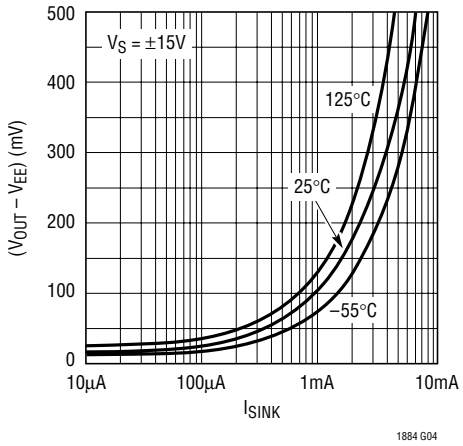


0.01Hz to 1Hz Noise

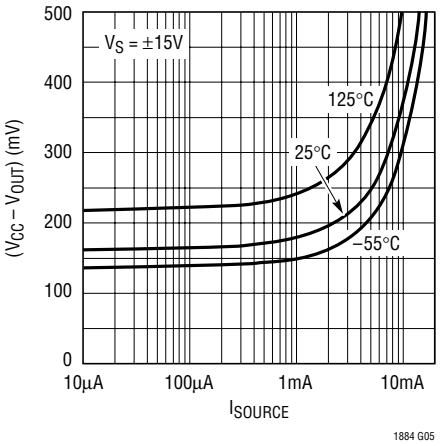


TYPICAL PERFORMANCE CHARACTERISTICS

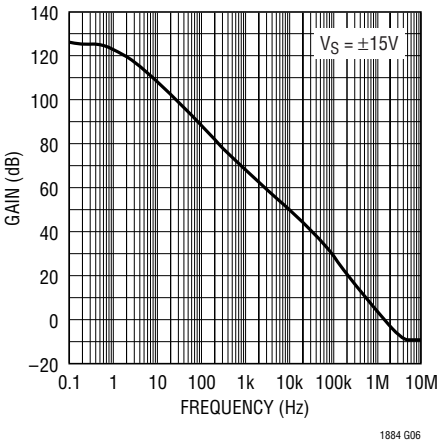
V_{OUT} vs I_{SINK}



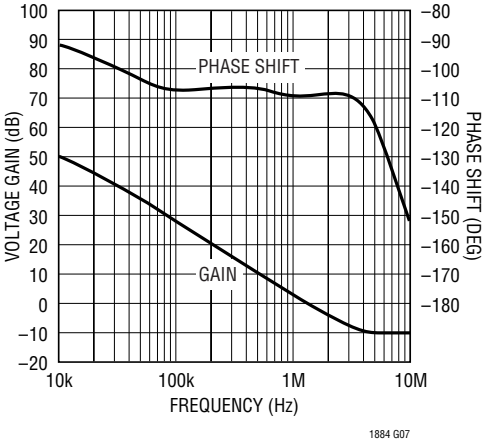
V_{OUT} vs I_{SOURCE}



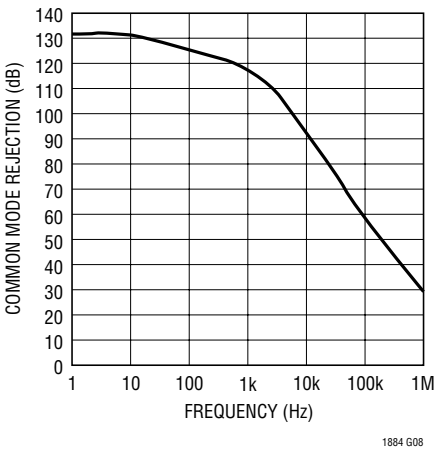
Gain vs Frequency



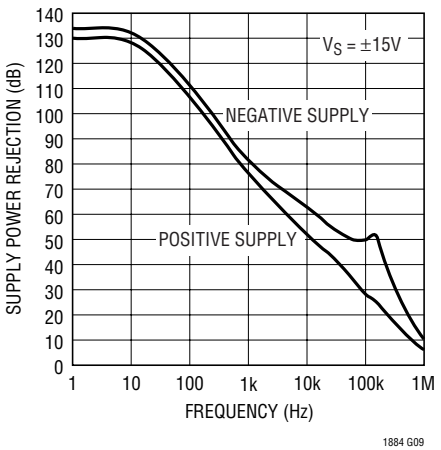
Gain, Phase Shift vs Frequency



CMRR vs Frequency



PSRR vs Frequency



APPLICATIONS INFORMATION

The LT1884 dual op amp features exceptional input precision with rail-to-rail output swing. Slew rate and small-signal bandwidth are superior to other amplifiers with comparable input precision. These characteristics make the LT1884 a convenient choice for precision low voltage systems and for improved AC performance in higher voltage precision systems. Obtaining beneficial advantage of the precision inherent in the amplifier depends upon proper applications circuit design and board layout.

Preserving Input Precision

Preserving the input voltage accuracy of the LT1884 requires that the applications circuit and PC board layout do not introduce errors comparable to or greater than the 30µV offset. Temperature differentials across the input connections can generate thermocouple voltages of 10's of microvolts. PC board layouts should keep connections to the amplifier's input pins close together and away from heat dissipating components. Air currents across the board can also generate temperature differentials.

The extremely low input bias currents, 60pA, allow high accuracy to be maintained with high impedance sources and feedback networks. The LT1884's low input bias currents are obtained by using a cancellation circuit on-chip. This causes the resulting $I_{BIAS}+$ and $I_{BIAS}-$ to be uncorrelated, as implied by the I_{OS} specification being comparable to the I_{BIAS}. The user should not try to balance the input resistances in each input lead, as is commonly

APPLICATIONS INFORMATION

recommended with most amplifiers. The impedance at either input should be kept as small as possible to minimize total circuit error.

PC board layout is important to insure that leakage currents do not corrupt the low I_{BIAS} of the amplifier. In high precision, high impedance circuits, the input pins should be surrounded by a guard ring of PC board interconnect, with the guard driven to the same common mode voltage as the amplifier inputs.

Input Common Mode Range

The LT1884 output is able to swing nearly to each power supply rail, but the input stage is limited to operating between V_{EE} + 0.8V and V_{CC} – 0.9V. Exceeding this common mode range will cause the gain to drop to zero; however, no gain reversal will occur.

Input Protection

The inverting and noninverting input pins of the LT1884 have limited on-chip protection. ESD protection is provided to prevent damage during handling. The input transistors have voltage clamping and limiting resistors to protect against input differentials up to 10V. Short transients above this level will also be tolerated. If the input pins can see a sustained differential voltage above 10V, external limiting resistors should be used to prevent damage to the amplifier. A 1k resistor in each input lead will provide protection against a 30V differential voltage.

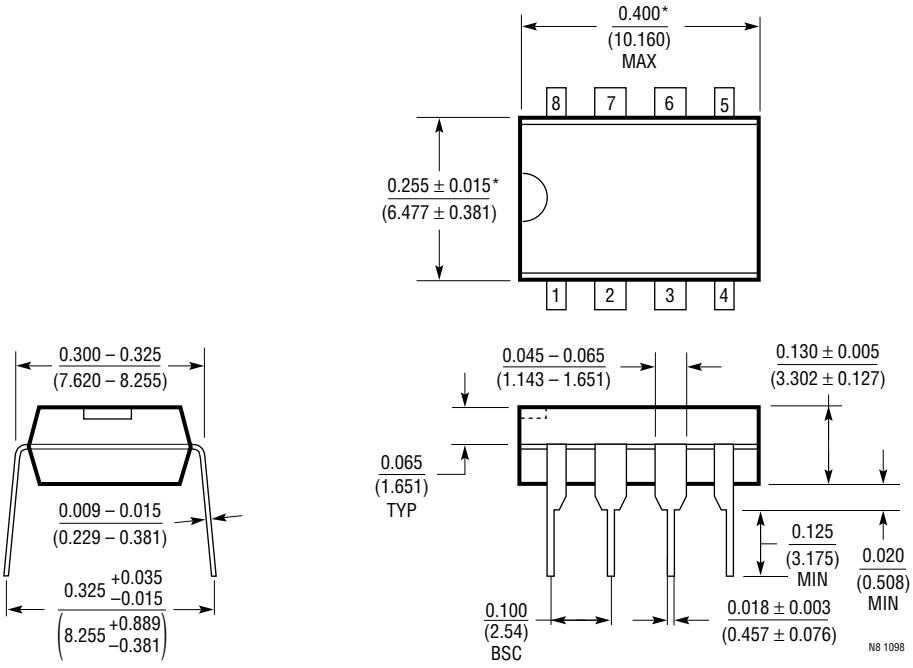
Capacitive Loads

The LT1884 can drive capacitive loads up to 300pF in unity-gain. The capacitive load driving increases as the amplifier is used in higher gain configurations. Capacitive load driving may be increased by decoupling the capacitance from the output with a small resistance.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

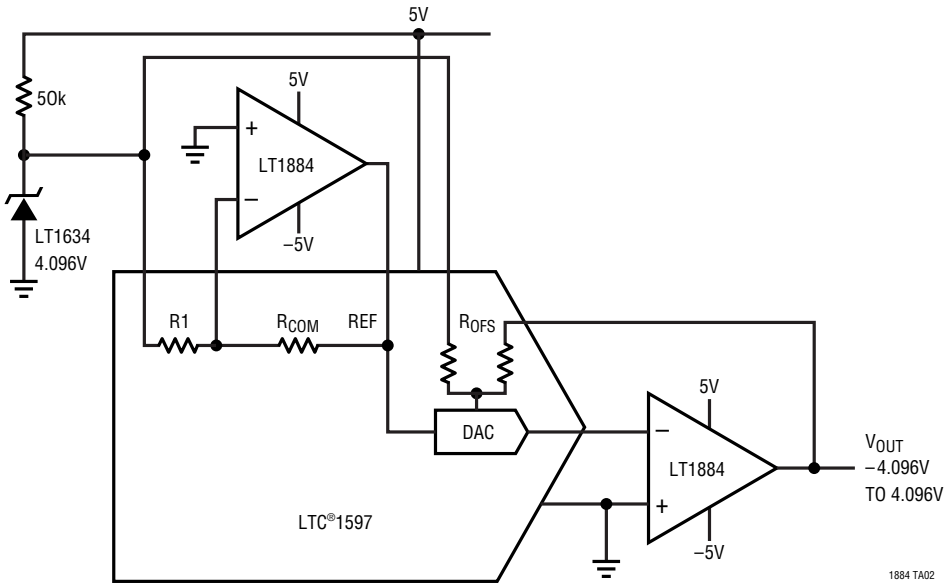
N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

TYPICAL APPLICATION

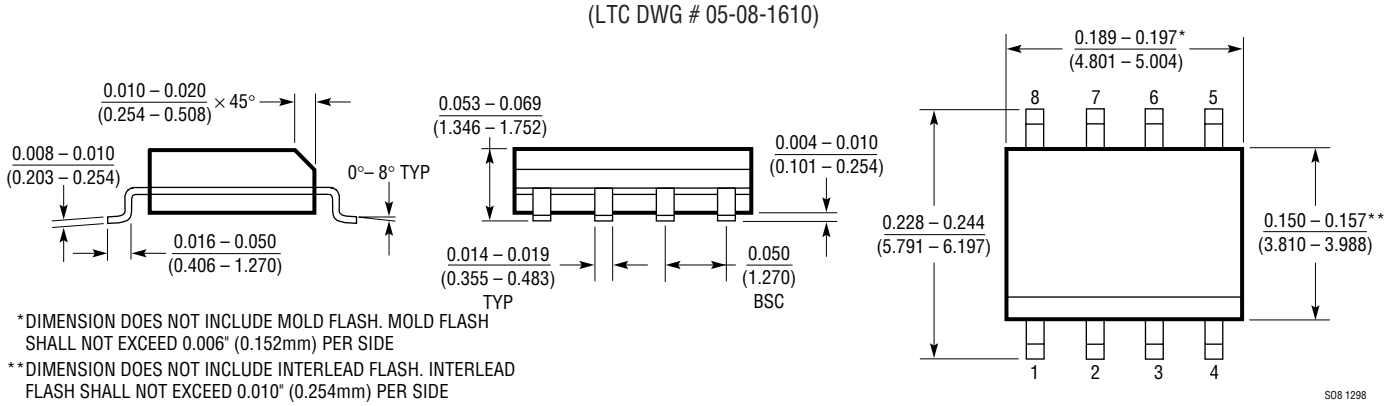
16-Bit Voltage Output DAC on ±5V Supply



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1112	Dual Picoamp Input Op Amp	V_{OS} = 60μV Max
LT1490	Micropower Rail-to-Rail Input and Output Op Amp	Over-The-Top™ Common Mode Range
LT1886	Dual 700MHz, 200mA Op Amp	Low Distortion –72dBc at 200kHz
LT1167	Gain Programmable Instrumentation Amp	Gain Error = 0.08% Max

Over-The-Top is a trademark of Linear Technology Corporation.

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