LTC1873

Dual 550kHz Synchronous 2-Phase Switching Regulator Controller with 5-Bit VID

September 1999

FEATURES

- Two Independent PWM Controllers in One Package
- **Side 1 Output Is Compliant with Intel Desktop VID Specifications (Includes 5-Bit DAC)**
- 1.3V to 3.5V Output Voltage with 50mV/100mV Steps
- **Two Sides Run Out-of-Phase to Minimize C_{IN}**
- All N-Channel External MOSFET Architecture
- No External Current Sense Resistors Required
- **Precison Internal 0.8V ±1% Reference**
- 550kHz Switching Frequency Minimizes External Component Size
- Very Fast Transient Response
- Up to 25A Output Current per Channel
- Low Shutdown Current: < 100µA
- Small 28-Pin SSOP Package

APPLICATIONS

- Microprocessor Core and I/O Supplies
- Multiple Logic Supply Generator
- High Efficiency Power Conversion

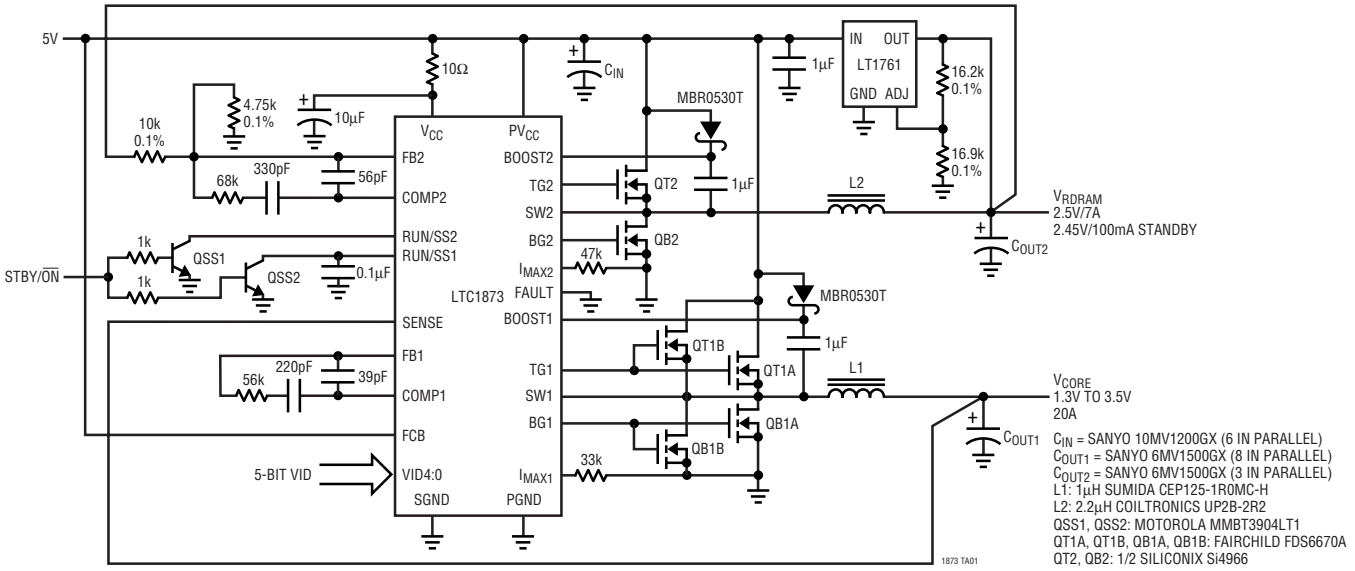
DESCRIPTION

The LTC®1873 is a dual switching regulator controller optimized for high efficiency with low input voltages. It includes two complete, on-chip, independent switching regulator controllers. Each is designed to drive a pair of external N-channel MOSFETs in a voltage mode feedback, synchronous buck configuration. The LTC1873 includes digital output voltage adjustment on side 1 that conforms to the Intel Desktop VID specification. A constant-frequency, true PWM design minimizes external component size and cost and optimizes load transient performance. The synchronous buck architecture automatically shifts to discontinuous and then to Burst Mode™ operation as the output load decreases, ensuring maximum efficiency over a wide range of load currents.

The LTC1873 features an onboard reference trimmed to 0.5% and delivers better than 1.5% regulation at the converter outputs over all combination of line, load and temperature. Each channel can be enabled independently; with both channels disabled, the LTC1873 shuts down and supply current drops below 100µA.

TYPICAL APPLICATION

Low Cost Desktop CPU Supply With RDRAM Keepalive



C_{IN} = SANYO 10MV1200GX (6 IN PARALLEL)
C_{OUT1} = SANYO 6MV1500GX (8 IN PARALLEL)
C_{OUT2} = SANYO 6MV1500GX (3 IN PARALLEL)
L1: 1µH SUMIDA CEP125-1R0MC-H
L2: 2.2µH COILTRONICS UP2B-2R2
QSS1, QSS2: MOTOROLA MMBT3904LT1
QT1A, QT1B, QB1A, QB1B: FAIRCHILD FDS6670A
QT2, QB2: 1/2 SILICONIX Si4966

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} 7V
- BOOST*n* 15V
- BOOST*n* – SW*n* 7V

Input Voltage
- SW*n* ..... –1V to 15V
- VID*n* ..... –0.3V to 7V
- All Other Inputs ..... –0.3V to V_{CC} + 0.3V

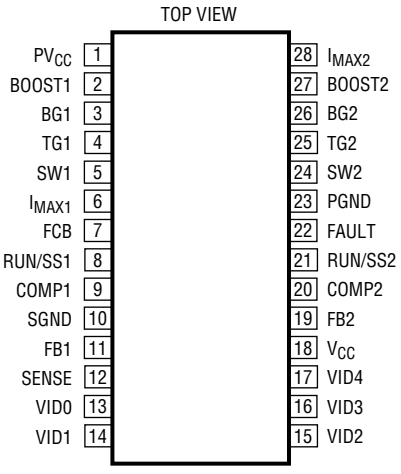
Peak Output Current < 10µs
- TG*n*, BG*n* 5A

Operating Temperature Range
- (Note 2) ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 55°C/W

ORDER PART NUMBER
LTC1873EG

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 5V unless otherwise specified. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
V_{CC}	V_{CC} Supply Voltage		●	3		7	V
PV_{CC}	PV_{CC} Supply Voltage	(Note 3)	●	3		7	V
BV_{CC}	BOOST Pin Voltage	V_{BOOST} – V_{SW} (Note 3)	●	2.7		7	V
I_{CC}	V_{CC} Supply Current	Test Circuit 1 RUN/SS1 = RUN/SS2 = 0V (Note 6)	● ●		4.5 30	8 100	mA µA
IPV_{CC}	PV_{CC} Supply Current	Test Circuit 1 (Note 5) RUN/SS1 = RUN/SS2 = 0V (Note 6)	● ●		2.5 6	6 100	mA µA
I_{BOOST}	BOOST Pin Current	Test Circuit 1 (Note 5) RUN/SS1 = RUN/SS2 = 0V	● ●		1.3 0.1	3 10	mA µA
V_{FB}	Feedback Voltage	Test Circuit 1	●	0.792	0.800	0.808	V
ΔV_{FB}	Feedback Voltage Line Regulation	V_{CC} = 3V to 7V	●		±0.005	±0.05	%/V
I_{FB}	Feedback Current	FB2 Only (Note 7)	●		±0.001	±1	µA
V_{FCB}	FCB Threshold		●	0.75	0.8	0.85	V
ΔV_{FCB}	FCB Feedback Hysteresis				20		mV
I_{FCB}	FCB Pin Current		●		±0.001	±1	µA
V_{RUN}	RUN/SS Pin RUN Threshold		●	0.45	0.55	0.65	V
I_{SS}	Soft Start Source Current	RUN/SS*n* = 0V		–1.5	–3.5	–5.5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 5V unless otherwise specified. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Characteristics							
f_{OSC}	Oscillator Frequency	Test Circuit 1	●	475	550	750	kHz
Φ_{OSC2}	Controller 2 Oscillator Phase	Relative to Controller 1			180		DEG
DC_{MIN1}	Minimum Duty Cycle	$V_{FB} < V_{MAX}$	●	7	10		%
DC_{MIN2}	Minimum Duty Cycle	$V_{FB} > V_{MAX}$	●	0			%
DC_{MAX}	Maximum Duty Cycle		●	87	90	93	%
t_{NOV}	Driver Nonoverlap	Test Circuit 1	●		25	100	ns
t_r, t_f	Driver Rise/Fall Time	Test Circuit 1 (Note 9)	●		15	80	ns
Feedback Amplifier							
A_{VFB}	FB DC Gain		●	74	85		dB
GBW	FB Gain Bandwidth				25		MHz
I_{ERR}	FB Sink/Source Current	$COMP_N$ Output	●	±3	±10		mA
V_{MIN}	MIN Comparator Threshold		●		760	785	mV
V_{MAX}	MAX Comparator Threshold		●	815	840		mV
Current Limit Loop							
A_{VILIM}	I_{LIM} Gain				40		dB
I_{IMAX}	I_{MAX} Source Current	I_{MAX} = 0V	●	–7	–10	–13	µA
Status Outputs							
V_{FAULT}	FAULT Trip Point	V_{FB} Relative to Regulated V_{OUT}	●	+10	+15	+20	%
V_{OLF}	FAULT Output Low Voltage	I_{FAULT} = 1mA	●		0.03	0.1	V
I_{FAULT}	FAULT Output Current	V_{FAULT} = 0V			–10		µA
t_{FAULT}	FAULT Delay Time	$V_{FB} > V_{FAULT}$ to FAULT ↓			25		µs
VID Inputs							
R1	Resistance Between SENSE and FB1	Side 1 Only			20		kΩ
V_{OUT} Error %	Output Voltage Accuracy	Programmed from 1.3V to 3.5V	●	–1.5		1.5	%
R_{PULLUP}	VID Input Pull-Up Resistance	V_{DIODE} = 0.6V (Note 8)			40		kΩ
VID_T	VID Input Voltage Threshold	V_{IL} (2.7V ≤ V_{CC} ≤ 5.5V) V_{IH} (2.7V ≤ V_{CC} ≤ 5.5V)		 1.6		0.4 	V V
$I_{VID-LEAK}$	VID Input Leakage Current	V_{CC} < VID < 7V (Note 8)			0.01	±1	µA
V_{PULLUP}	VID Pull-Up Voltage	V_{CC} = 3.3V V_{CC} = 5V			2.8 4.5		V V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC1873 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: PV_{CC} and BV_{CC} (V_{BOOST} – V_{SW}) must be greater than $V_{GS(ON)}$ of the external MOSFETs used to ensure proper operation.

Note 4: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 5: Supply current in normal operation is dominated by the current needed to charge and discharge the external MOSFET gates. This current will vary with supply voltage and the external MOSFETs used.

Note 6: Supply current in shutdown is dominated by external MOSFET leakage and may be significantly higher than the quiescent current drawn by the LTC1873, especially at elevated temperature.

Note 7: Feedback current at FB1 will be higher due to internal VID resistors.

Note 8: Each built-in pull-up resistor attached to the VID inputs also has a series diode connected to V_{CC} to allow input voltages higher than the V_{CC} supply without damage or clamping. (See Block Diagram.)

Note 9: Rise and fall times are measured at 20% to 80% levels.

PIN FUNCTIONS

PV_{CC} (Pin 1): Driver Power Supply Input. PV_{CC} provides power to the two BG*n* output drivers. PV_{CC} must be connected to a voltage high enough to fully turn on the external MOSFETs QB1 and QB2. PV_{CC} should generally be connected directly to V_{IN}. PV_{CC} requires at least a 1µF bypass capacitor directly to PGND.

BOOST1 (Pin 2): Controller 1 Top Gate Driver Supply. The BOOST1 pin supplies power to the floating TG1 driver. BOOST1 should be bypassed to SW1 with a 1µF capacitor. An additional Schottky diode from V_{IN} to BOOST1 pin will create a complete floating charge-pumped supply at BOOST1. No other external supplies are required.

BG1 (Pin 3): Controller 1 Bottom Gate Drive. The BG1 pin drives the gate of the bottom N-channel synchronous switch MOSFET, QB1. BG1 is designed to drive up to 10,000pF of gate capacitance directly. If RUN/SS1 goes low, BG1 will go low, turning off QB1. If FAULT mode is tripped, BG1 will go high and stay high, keeping QB1 on until the power is cycled.

TG1 (Pin 4): Controller 1 Top Gate Drive. The TG1 pin drives the gate of the top N-channel MOSFET, QT1. The TG1 driver draws power from the BOOST1 pin and returns to the SW1 pin, providing true floating drive to QT1. TG1 is designed to drive up to 10,000pF of gate capacitance directly. In shutdown or fault modes, TG1 will go low.

SW1 (Pin 5): Controller 1 Switching Node. SW1 should be connected to the switching node of converter 1. The TG1 driver ground returns to SW1, providing floating gate drive to the top N-channel MOSFET switch, QT1. The voltage at SW1 is compared to I_{MAX1} by the current limit comparator while the bottom MOSFET, QB1, is on.

I_{MAX1} (Pin 6): Controller 1 Current Limit Set. The I_{MAX1} pin sets the current limit comparator threshold for controller 1. If the voltage drop across the bottom MOSFET, QB1, exceeds the magnitude of the voltage at I_{MAX1}, controller 1 will go into current limit. The I_{MAX1} pin has an internal 10µA current source pull-up, allowing the current threshold to be set with a single external resistor to PGND. This current setting resistor should be Kelvin connected to the source of QB1. See the Current Limit Programming section for more information on choosing R_{IMAX}.

FCB (Pin 7): Force Continuous Bar. The FCB pin forces both converters to maintain continuous synchronous operation regardless of load when the voltage at FCB drops below 0.8V. FCB is normally tied to V_{CC}. To force continuous operation, tie FCB to SGND. FCB can also be connected to a feedback resistor divider from a secondary winding on one converter's inductor to generate a third regulated output voltage. Do not leave FCB floating.

RUN/SS1 (Pin 8): Controller 1 Run/Soft-Start. Pulling RUN/SS1 to SGND will disable controller 1 and turn off both of its external MOSFET switches. Pulling both RUN/SS pins down will shut down the entire LTC1873, dropping the quiescent supply current below 50µA. A capacitor from RUN/SS1 to SGND will control the turn-on time and rate of rise of the controller 1 output voltage at power-up. An internal 3.5µA current source pull-up at RUN/SS1 pin sets the turn-on time at approximately 50ms/µF.

COMP1 (Pin 9): Controller 1 Loop Compensation. The COMP1 pin is connected directly to the output of the first controller's error amplifier and the input to the PWM comparator. An RC network is used at the COMP1 pin to compensate the feedback loop for optimum transient response.

SGND (Pin 10): Signal Ground. All internal low power circuitry returns to the SGND pin. Connect to a low impedance ground, separated from the PGND node. All feedback, compensation and soft-start connections should return to SGND. SGND and PGND should connect only at a single point, near the PGND pin and the negative plate of the C_{IN} bypass capacitor.

FB1 (Pin 11): Controller 1 Feedback Input. The loop compensation network for controller 1 should be connected to FB1. FB1 is connected internally to the VID resistor network to set the output voltage at side 1.

SENSE (Pin 12): Output Sense. Connect to V_{OUT1}.

VID0 to VID4 (Pins 13 to 17): VID Programming Inputs. These are logic inputs that set the output voltage at side 1 to a preprogrammed value (see Table 1). VID4 is the MSB, VID0 is the LSB. The codes selected by the VID*n* inputs correspond to the Intel Desktop VID specification. Each

PIN FUNCTIONS

VID*n* pin includes an on-chip 40kΩ pull-up resistor in series with a diode (see Block Diagram).

V_{CC} (Pin 18): Power Supply Input. All internal circuits except the output drivers are powered from this pin. V_{CC} should be connected to a low noise power supply voltage between 3V and 7V and should be bypassed to SGND with at least a 1µF capacitor in close proximity to the LTC1873.

FB2 (Pin 19): Controller 2 Feedback Input. FB2 should be connected through a resistor divider network to V_{OUT2} to set the ouput voltage. The loop compensation network for controller 2 also connects to FB2.

COMP2 (Pin 20): Controller 2 Loop Compensation. See COMP1.

RUN/SS2 (Pin 21): Controller 2 Run/Soft-Start. See RUN/SS1.

FAULT (Pin 22): Output Overvoltage Fault (Latched). The FAULT pin is an open-drain output with an internal 10µA pull-up. If either regulated output voltage rises more than 15% above its programmed value for more than 25µs, the FAULT output will go high and the entire LTC1873 will be disabled. When FAULT is high, both BG pins will go high, turning on the bottom MOSFET switches and pulling down the high output voltage. The LTC1873 will remain latched in this state until the power is cycled. When FAULT mode is active, the FAULT pin will be pulled up with an internal 10µA current source. Tying FAULT directly to SGND will disable latched FAULT mode and will allow the LTC1873 to resume normal operation when the overvoltage fault is removed.

PGND (Pin 23): Power Ground. The BG*n* drivers return to this pin. Connect PGND to a high current ground node in close proximity to the sources of external MOSFETs, QB1 and QB2, and the V_{IN} and V_{OUT} bypass capacitors.

SW2 (Pin 24): Controller 2 Switching Node. See SW1.

TG2 (Pin 25): Controller 2 Top Gate Drive. See TG1.

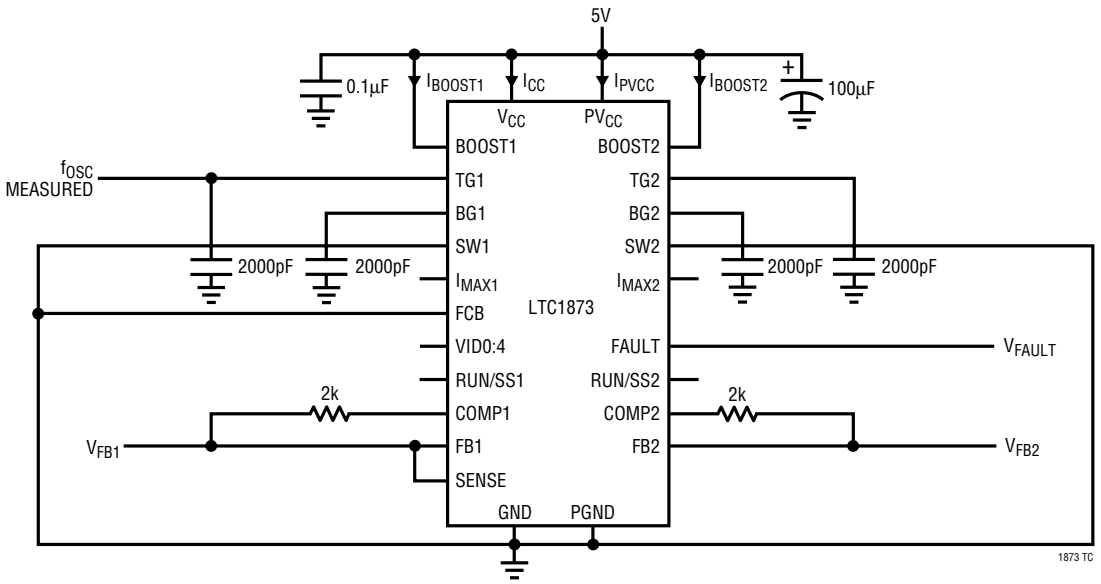
BG2 (Pin 26): Controller 2 Bottom Gate Drive. See BG1.

BOOST2 (Pin 27): Controller 2 Top Gate Driver Supply. See BOOST1.

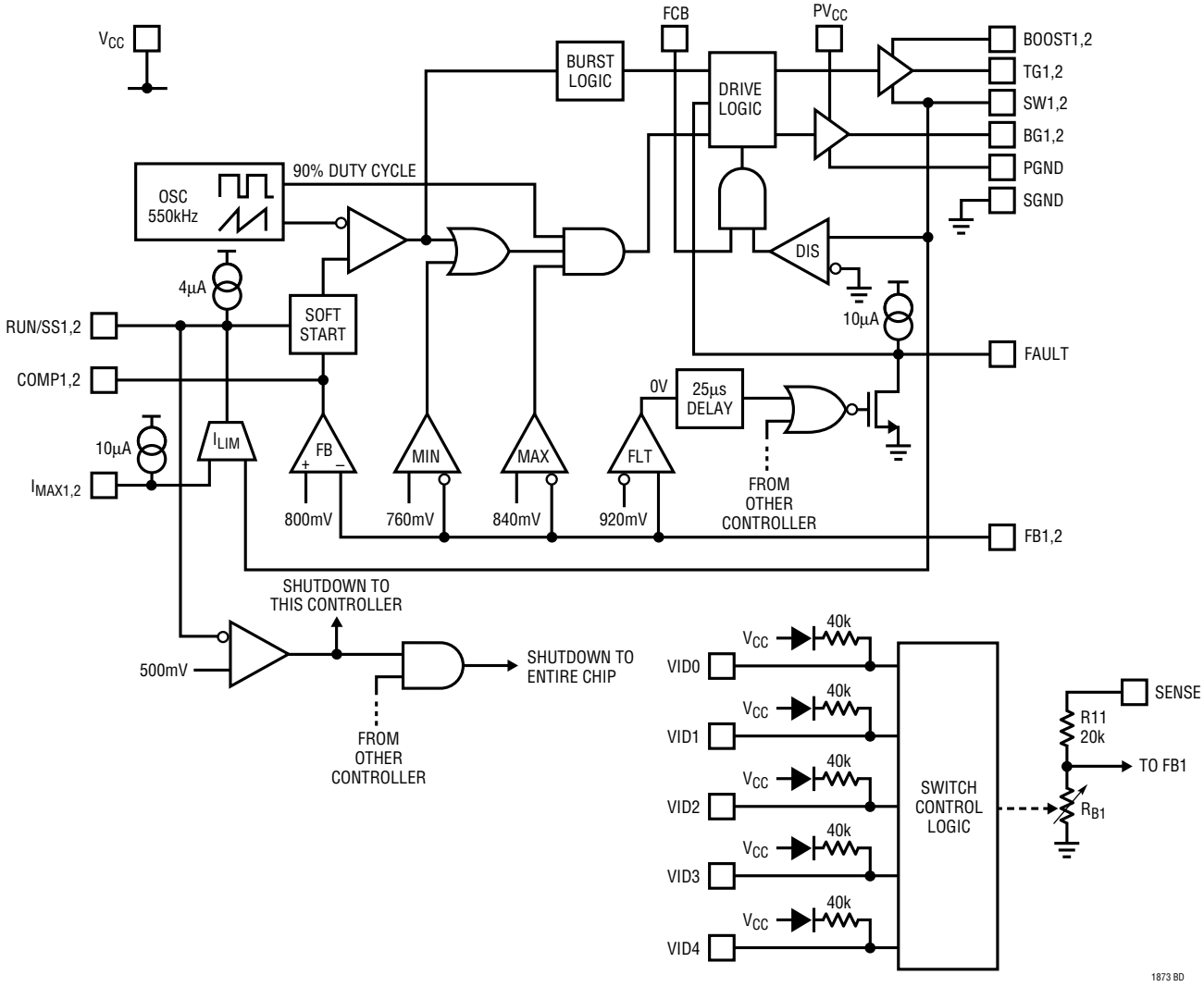
I_{MAX2} (Pin 28): Controller 2 Current Limit Set. See I_{MAX1}.

TEST CIRCUIT

Test Circuit 1



BLOCK DIAGRAM



APPLICATIONS INFORMATION

OVERVIEW

The LTC1873 is a dual, step-down (buck), voltage mode feedback switching regulator controller. It is designed to be used in a synchronous switching architecture with two external N-channel MOSFETs per channel. It is intended to operate from a low voltage input supply (7V maximum) and provide a high power, high efficiency, precisely regulated output voltage. Several features make it particularly suited for microprocessor supply regulation. Output regulation is extremely tight, with DC line and load regulation and initial accuracy better than 1.5%, and total regulation including transient response inside of 3.5% with a properly designed circuit. The 550kHz switching frequency allows the use of physically small, low value external components without compromising performance. An onboard DAC sets the output voltage at channel 1, consistent with the Intel desktop VID specification (Table 1).

The LTC1873's internal feedback amplifier is a 25MHz gain-bandwidth op amp, allowing the use of complex multipole/zero compensation networks. This allows the feedback loop to maintain acceptable phase margin at higher frequencies than traditional switching regulator controllers allow, improving stability and maximizing transient response. The 800mV internal reference at channel 2

APPLICATIONS INFORMATION

Table 1. VID Inputs and Corresponding Output Voltage for Channel 1

CODE	VID4	VID3	VID2	VID1	VID0	V_{OUT1}
00000	GND	GND	GND	GND	GND	2.05V
00001	GND	GND	GND	GND	Float	2.00V
00010	GND	GND	GND	Float	GND	1.95V
00011	GND	GND	GND	Float	Float	1.90V
00100	GND	GND	Float	GND	GND	1.85V
00101	GND	GND	Float	GND	Float	1.80V
00110	GND	GND	Float	Float	GND	1.75V
00111	GND	GND	Float	GND	GND	1.70V
01000	GND	Float	GND	GND	GND	1.65V
01001	GND	Float	GND	GND	Float	1.60V
01010	GND	Float	GND	Float	GND	1.55V
01011	GND	Float	GND	Float	Float	1.50V
01100	GND	Float	Float	GND	GND	1.45V
01101	GND	Float	Float	GND	Float	1.40V
01110	GND	Float	Float	Float	GND	1.35V
01111	GND	Float	Float	Float	Float	1.30V
10000	Float	GND	GND	GND	GND	3.50V
10001	Float	GND	GND	GND	Float	3.40V
10010	Float	GND	GND	Float	GND	3.30V
10011	Float	GND	GND	Float	Float	3.20V
10100	Float	GND	Float	GND	GND	3.10V
10101	Float	GND	Float	GND	Float	3.00V
10110	Float	GND	Float	Float	GND	2.90V
10111	Float	GND	Float	GND	GND	2.80V
11000	Float	Float	GND	GND	GND	2.70V
11001	Float	Float	GND	GND	Float	2.60V
11010	Float	Float	GND	Float	GND	2.50V
11011	Float	Float	GND	Float	Float	2.40V
11100	Float	Float	Float	GND	GND	2.30V
11101	Float	Float	Float	GND	Float	2.20V
11110	Float	Float	Float	Float	GND	2.10V
11111*	Float	Float	Float	Float	Float	2.00V

* 11111 is defined by Intel to signify “no CPU.” The LTC1873 will generate the output voltage shown when this codes is selected.

allows regulated output voltages as low as 800mV without external level shifting amplifiers.

The LTC1873’s synchronous switching logic transitions automatically into Burst Mode operation, maximizing efficiency with light loads. An onboard overvoltage (OV) fault flag indicates when an OV fault has occurred. The OV flag can be set to latch the device off when an OV fault has occurred, or to automatically resume operation when the fault is removed.

2-Phase Operation

The LTC1873 dual switching regulator controller offers considerable benefits using 2-phase operation. Circuit benefits include lower input filtering requirements, reduced electromagnetic interference (EMI) and increased efficiency associated with 2-phase operation.

Why the need for 2-phase operation? Until recently, constant-frequency dual switching regulators operated both channels in phase (i.e., single-phase operation). This means that both topside MOSFETs turned on at the same time, causing current pulses of up to twice the amplitude of those for one regulator to be drawn from the input capacitor. These large amplitude current pulses increased the total RMS current flowing from the input capacitor, requiring the use of more expensive input capacitors and increasing both EMI and losses in the input capacitor and input power supply.

With 2-phase operation, the two channels of the LTC1873 are operated 180 degrees out of phase. This effectively interleaves the current pulses coming from the switches, greatly reducing the overlap time where they add together. The result is a significant reduction in total RMS input current, which in turn allows less expensive input capacitors to be used, reduces shielding requirements for EMI and improves real world operating efficiency.

Figure 7 shows example waveforms for a single switching regulator channel versus a 2-phase LTC1873 system with both sides switching. A single-phase dual regulator with both sides operating would exhibit double the single side numbers. In this example, 2-phase operation reduced the RMS input current from $9.3A_{RMS}$ ($2 \times 4.66A_{RMS}$) to $4.8A_{RMS}$. While this is an impressive reduction in itself, remember that the power losses are proportional to I_{RMS}^2, meaning that the actual power wasted is reduced by a

APPLICATIONS INFORMATION

factor of 3.75. The reduced input ripple voltage also means less power is lost in the input power path, which could include batteries, switches, trace/connector resistances and protection circuitry. Improvements in both conducted and radiated EMI also directly accrue as a result of the reduced RMS input current and voltage.

Small Footprint

The LTC1873 operates at a 550kHz switching frequency, allowing it to use low value inductors without generating excessive ripple currents. Because the inductor stores less energy per cycle, the physical size of the inductor can be reduced without risking core saturation, saving PCB board space. The high operating frequency also means less energy is stored in the output capacitors between cycles, minimizing their required value and size. The remaining components, including the SSOP-28 LTC1873, are tiny, allowing an entire dual-output LTC1873 circuit to be constructed in $1.5in^2$ of PCB space. Further, this space is generally located right next to the microprocessor or in some similarly congested area, where PCB real estate is at a premium.

Fast Transient Response

The LTC1873 uses a fast 25MHz GBW op amp as an error amplifier. This allows the compensation network to be designed with several poles and zeros in a more flexible configuration than with a typical g_m feedback amplifier. The high bandwidth of the amplifier, coupled with the high switching frequency and the low values of the external inductor and output capacitor, allow very high loop crossover frequencies. The low inductor value is the other half of the equation—with a typical value on the order of 1μH, the inductor allows very fast di/dt slew rates. The result is superior transient response compared with conventional solutions.

High Efficiency

The LTC1873 uses a synchronous step-down (buck) architecture, with two external N-channel MOSFETs per output. A floating topside driver and a simple external charge pump provide full gate drive to the upper MOSFET. The voltage mode feedback loop and MOSFET V_{DS} current limit sensing remove the need for an external current sense resistor, eliminating an external component and a source of power loss in the high current path. Properly designed circuits using low gate charge MOSFETs are capable of efficiencies exceeding 90% over a wide range of output voltages.

VID Programming

The LTC1873 includes an onboard feedback network that programs the output voltage at side 1 in accordance with the Intel Desktop VID specification (Table 1). The network includes a 20k resistor (R1) connected from SENSE to FB1, and a variable value resistor (R_B) from FB1 to SGND, with the value set by the digital code present at the VID0:4 pins. SENSE should be connected to V_{OUT1} to allow the network to monitor the output voltage. No additional feedback components are required to set the output voltage at controller 1, although loop compensation components are still required. Each VID*n* pin includes an internal 40k pull-up resistor, allowing it to float high if left unconnected. The pull-up resistors are connected to V_{CC} through diodes (see Block Diagram), allowing the VID*n* pins to be pulled above V_{CC} without damage.

Note that code 11111, defined by Intel to indicate "no CPU present," does generate an output voltage at V_{OUT1} (2.00V). Note also that controller 2 on the LTC1873 is not connected to the VID circuitry, and works independently from controller 1.

ARCHITECTURE DETAILS

The LTC1873 dual switching regulator controller includes two independent regulator channels. The two sides of the chip and their corresponding external components act independently of each other with the exception of the common input bypass capacitor, the VID circuitry at side 1, and the FCB and FAULT pins, which affect both channels. In the following discussions, when a pin is referred to without mentioning which side is involved, that discussion applies equally to both sides.

APPLICATIONS INFORMATION

Switching Architecture

Each half of the LTC1873 is designed to operate as a synchronous buck converter (Figure 1). Each channel includes two high power MOSFET gate drivers to control external N-channel MOSFETs QT and QB. These drivers have 0.5Ω output impedances and can carry well over an amp of continuous current with peak currents up to 5A to slew large MOSFET gates quickly. The external MOSFETs are connected with the drain of QT attached to the input supply and the source of QT at the switching node SW. QB is the synchronous rectifier with its drain at SW and its source at PGND. SW is connected to one end of the inductor, with the other end connected to V_{OUT}. The output capacitor is connected from V_{OUT} to PGND.

When a switching cycle begins, QB is turned off and QT is turned on. SW rises almost immediately to V_{IN} and the inductor current begins to increase. When the PWM pulse finishes, QT turns off and one nonoverlap interval later, QB turns on. Now SW drops to PGND and the inductor current decreases. The cycle repeats with the next tick of the master clock. The percentage of time spent in each mode is controlled by the duty cycle of the PWM signal, which in turn is controlled by the feedback amplifier. The master clock runs at a 550kHz rate and turns QT once every 1.8μs. In a typical application with a 5V input and a 1.5V output, the duty cycle will be set at 1.5/5 × 100% or 30% by the feedback loop. This will give roughly a 540ns on-time for QT and a 1.26μs on-time for QB.

This constant frequency operation brings with it a couple of benefits. Inductor and capacitor values can be chosen with a precise operating frequency in mind and the feedback loop components can be similarly tightly specified. Noise generated by the circuit will always be in a known frequency band with the 550kHz frequency designed to leave the 455kHz IF band free of interference. Subharmonic oscillation and slope compensation, common headaches with constant frequency current mode switchers, are absent in voltage mode designs like the LTC1873.

During the time that QT is on, its source (the SW pin) is at V_{IN}. V_{IN} is also the power supply for the LTC1873. However, QT requires V_{IN} + $V_{GS(ON)}$ at its gate to achieve minimum R_{ON}. This presents a problem for the LTC1873—it needs to generate a gate drive signal at TG higher than its highest supply voltage. To accomplish this, the TG driver runs from floating supplies, with its negative supply attached to SW and its power supply at BOOST. This allows it to slew up and down with the source of QT. In combination with a simple external charge pump (Figure 2), this allows the LTC1873 to completely enhance the gate of QT without requiring an additional, higher supply voltage.

The two channels of the LTC1873 run from a common clock, with the phasing chosen to be 180° from side 1 to side 2. This has the effect of doubling the frequency of the switching pulses seen by the input bypass capacitor, significantly lowering the RMS current seen by the capacitor and reducing the value required (see the 2-Phase section).

Feedback Amplifier

Each side of the LTC1873 senses the output voltage at V_{OUT} with an internal feedback op amp (see Block Diagram). This is a real op amp with a low impedance output, 85dB open-loop gain and 25MHz gain-bandwidth product. The positive input is connected internally to an 800mV reference, while the negative input is connected to the FB

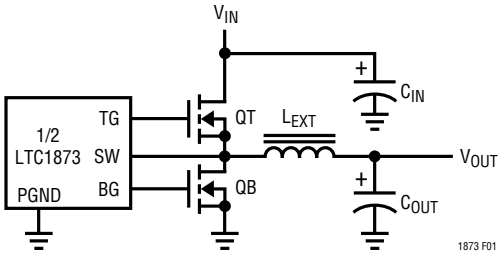


Figure 1. Synchronous Buck Architecture

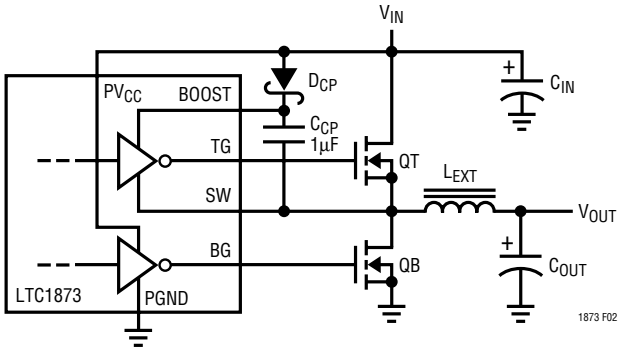


Figure 2. Floating TG Driver Supply

APPLICATIONS INFORMATION

pin. The output is connected to COMP, which is in turn connected to the soft-start circuitry and from there to the PWM generator.

Unlike many regulators that use a resistor divider connected to a high impedance feedback input, the LTC1873 is designed to use an inverting summing amplifier topology with the FB pin configured as a virtual ground. This allows flexibility in choosing pole and zero locations not available with simple g_m configurations. In particular, it allows the use of "type 3" compensation, which provides a phase boost at the LC pole frequency and significantly improves loop phase margin (see Figure 3). Appendix A contains a detailed explanation of type 3 feedback loops. Note that side 1 of the LTC1873 includes R1 and R_B internally as part of the VID DAC circuitry.

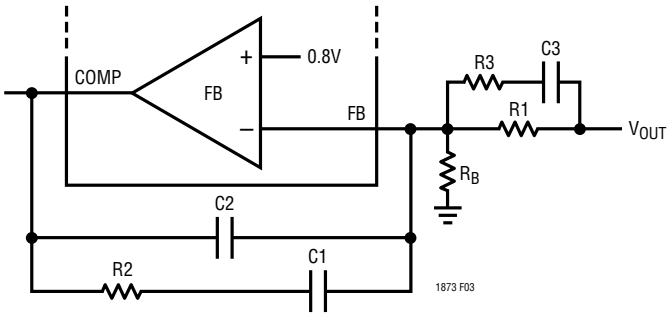


Figure 3. "Type 3" Feedback Loop (Side 2 Shown)

MIN/MAX COMPARATORS

Two additional feedback loops keep an eye on the primary feedback amplifier and step in if the feedback node moves ±5% from its nominal 800mV value. The MAX comparator (see Block Diagram) activates whenever FB rises more than 5% above 800mV. It immediately turns the top MOSFET (QT) off and the bottom MOSFET (QB) on and keeps them that way until FB falls back within 5% of its nominal value. This pulls the output down as fast as possible, preventing damage to the (often expensive) load. If FB rises because the output is shorted to a higher supply, QB will stay on until the short goes away, the higher supply current limits or QB dies trying to save the load. This behavior provides maximum protection against overvoltage faults at the output, while allowing the circuit to resume normal operation when the fault is removed. The overvoltage protection circuit can optionally be set to latch the output off permanently (see the Overvoltage Fault section).

The MIN comparator (see Block Diagram) trips whenever FB is more than 5% below 800mV and immediately forces the switch duty cycle to 90% to bring the output voltage back into range. It releases when FB is within the 5% window. MIN is disabled when the soft-start or current limit circuits are active—the only two times that the output should legitimately be below its regulated value.

Notice that the FB pin is the virtual ground node of the feedback amplifier. A typical compensation network does not include local DC feedback around the amplifier, so that the DC level at FB will be an accurate replica of the output voltage, divided down by R1 and R_B (Figure 3). However, the compensation capacitors will tend to attenuate AC signals at FB, especially with low bandwidth type 1 feedback loops. This creates a situation where the MIN and MAX comparators do not respond immediately to shifts in the output voltage, since they monitor the output at FB. Maximizing feedback loop bandwidth will minimize these delays and allow MIN and MAX to operate properly. See the Feedback Loop/Compensation section.

SHUTDOWN/SOFT-START

Each half of the LTC1873 has a RUN/SS pin. The RUN/SS pins perform two functions: when pulled to ground, each shuts down its half of the LTC1873, and each acts as a conventional soft-start pin, enforcing a maximum duty cycle limit proportional to the voltage at RUN/SS. An internal 3.5μA current source pull-up is connected to each RUN/SS pin, allowing a soft-start ramp to be generated with a single external capacitor to ground. The 3.5μA current sources are active even when the LTC1873 is shut down, ensuring the device will start when any external pull-down at RUN/SS is released. Either side can be shut down without affecting the operation of the other side. If both sides are shut down at the same time, the LTC1873 goes into a micropower sleep mode, and quiescent current drops typically below 50μA. Entering sleep mode also resets the FAULT latch, if it was set.

APPLICATIONS INFORMATION

Each RUN/SS pin shuts down its half of the LTC1873 when it falls below about 0.5V (Figure 4). Between 0.5V and about 1V, that half is active, but the maximum duty cycle is limited to 10%. The maximum duty cycle limit increases linearly between 1V and 2.5V, reaching its final value of 90% when RUN/SS is above 2.5V. Somewhere before this point, the feedback amplifier will assume control of the loop and the output will come into regulation. When RUN/SS rises to 0.5V below V_{CC}, the MIN feedback comparator is enabled, and the LTC1873 is in full operation.

CURRENT LIMIT

The LTC1873 includes an onboard current limit circuit that limits the maximum output current to a user-programmed level. It works by sensing the voltage drop across QB during the time that QB is on and comparing that voltage to a user-programmed voltage at I_{MAX}. Since QB looks like a low value resistor during its on-time, the voltage drop across it is proportional to the current flowing in it. In a buck converter, the average current in the inductor is equal to the output current. This current also flows through QB during its on-time. Thus, by watching the voltage across QB, the LTC1873 can monitor the output current.

Any time QB is on and the current flowing to the output is reasonably large, the SW node at the drain of QB will be somewhat negative with respect to PGND. The LTC1873 senses this voltage and inverts it to allow it to compare the sensed voltage with a positive voltage at the I_{MAX} pin. The I_{MAX} pin includes a trimmed 10µA pull-up, enabling the user to set the voltage at I_{MAX} with a single resistor, R_{IMAX}, to ground. The LTC1873 compares the two inputs and begins limiting the output current when the magnitude of the negative voltage at the SW pin is greater than the voltage at I_{MAX}.

The current limit detector is connected to an internal g_m amplifier that pulls a current from the RUN/SS pin proportional to the difference in voltage magnitudes between the SW and I_{MAX} pins. This current begins to discharge the soft-start capacitor at RUN/SS, reducing the duty cycle and controlling the output voltage until the current drops below the limit. The soft-start capacitor needs to move a fair amount before it has any effect on the duty cycle, adding a delay until the current limit takes effect (Figure 4). This allows the LTC1873 to experience brief overload conditions without affecting the output voltage regulation. The delay also acts as a pole in the current limit loop to

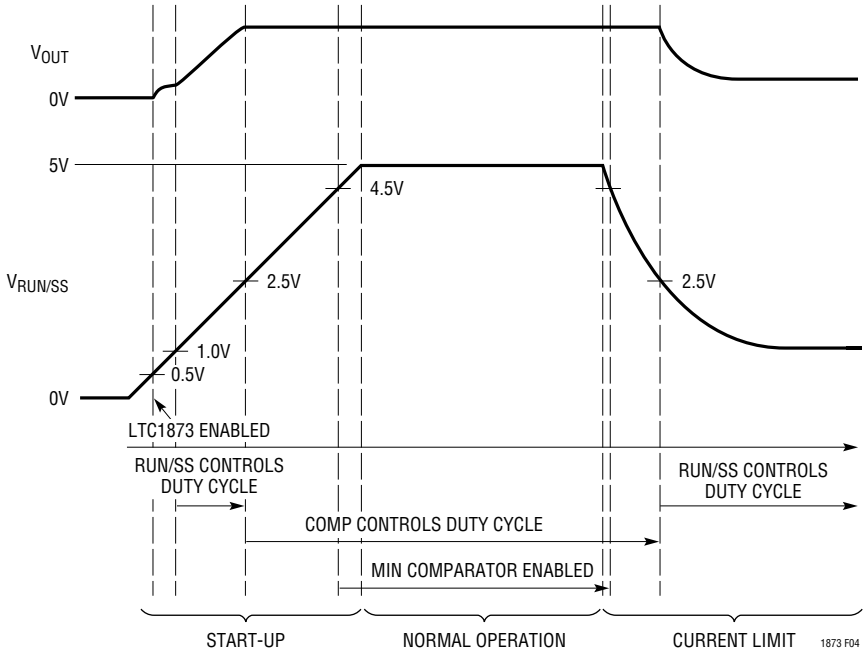


Figure 4. Soft-Start Operation in Start-Up and Current Limit

APPLICATIONS INFORMATION

enhance loop stability. Larger overloads cause the soft-start capacitor to pull down quickly, protecting the output components from damage. The current limit g_m amplifier includes a clamp to prevent it from pulling RUN/SS below 0.5V and shutting off the device.

Power MOSFET $R_{DS(ON)}$ varies from MOSFET to MOSFET, limiting the accuracy obtainable from the LTC1873 current limit loop. Additionally, ringing on the SW node due to parasitics can add to the apparent current, causing the loop to engage early. The LTC1873 current limit is designed primarily as a disaster prevention, "no blow up" circuit, and is not useful as a precision current regulator. It should typically be set around 50% above the maximum expected normal output current to prevent component tolerances from encroaching on the normal current range. See the Current Limit Programming section for advice on choosing a valve for R_{IMAX}.

DISCONTINUOUS/Burst Mode OPERATION

Theory of operation

The LTC1873 switching logic has three modes of operation. Under heavy loads, it operates as a fully synchronous, continuous conduction switching regulator. In this mode of operation ("continuous" mode), the current in the inductor flows in the positive direction (toward the output) during the entire switching cycle, constantly supplying current to the load. In this mode, the synchronous switch (QB) is on whenever QT is off, so the current always flows through a low impedance switch, minimizing voltage drop and power loss. This is the most efficient mode of operation at heavy loads, where the resistive losses in the power devices are the dominant loss term.

Continuous mode works efficiently when the load current is greater than half of the ripple current in the inductor. In a buck converter like the LTC1873, the average current in the inductor (averaged over one switching cycle) is equal to the load current. The ripple current is the difference between the maximum and the minimum current during a switching cycle (see Figure 5a). The ripple current depends on inductor value, clock frequency and output voltage, but is constant regardless of load as long as the LTC1873 remains in continuous mode. See the Inductor Selection section for a detailed description of ripple current.

As the output load current decreases in continuous mode, the average current in the inductor will reach a point where it drops below half the ripple current. At this point, the current in the inductor will reverse during a portion of the switching cycle, or begin to flow from the output back to the input. This does not adversely affect regulation, but does cause additional losses as a portion of the inductor current flows back and forth through the resistive power switches, giving away a little more power each time and lowering the efficiency. There are some benefits to allowing this reverse current flow: the circuit will maintain regulation even if the load current drops below zero (the load supplies current to the LTC1873) and the output ripple voltage and frequency remain constant at all loads, easing filtering requirements. Circuits that take advantage of this behavior can force the LTC1873 to operate in continuous mode at all loads by tying the FCB (Force Continuous Bar) pin to ground.

Discontinuous Mode

To minimize the efficiency loss due to reverse current flow at light loads, the LTC1873 switches to a second mode of operation: discontinuous mode (Figure 5b). In discontinuous mode, the LTC1873 detects when the inductor current approaches zero and turns off QB for the remainder of the switch cycle. During this time, the voltage at the SW pin will float about V_{OUT}, the voltage across the inductor will be zero, and the inductor current remains zero until the next switching cycle begins and QT turns on again. This prevents current from flowing backwards in QB, eliminating that power loss term. It also reduces the ripple current in the inductor as the output current approaches zero.

The LTC1873 detects that the inductor current has reached zero by monitoring the voltage at the SW pin while QB is on. Since QB acts like a resistor, SW should ideally be right at 0V when the inductor current reaches zero. In reality, the SW node will ring to some degree immediately after it is switched to ground by QB, causing some uncertainty as to the actual moment the average current in QB goes to zero. The LTC1873 minimizes this effect by ignoring the SW node for a fixed 50ns after QB turns on when the ringing

APPLICATIONS INFORMATION

is most severe, and by including a few millivolts offset in the comparator that monitors the SW node. Despite these precautions, some combinations of inductor and layout parasitics can cause the LTC1873 to enter discontinuous mode erratically. In many cases, the time that QB turns off will correspond to a peak in the ringing waveform at the SW pin (Figure 6). This erratic operation isn't pretty, but retains much of the efficiency benefit of discontinuous mode and maintains regulation at all times.

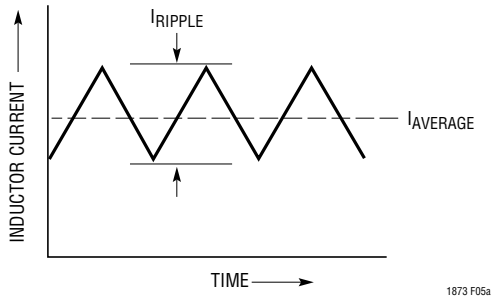


Figure 5a. Continuous Mode

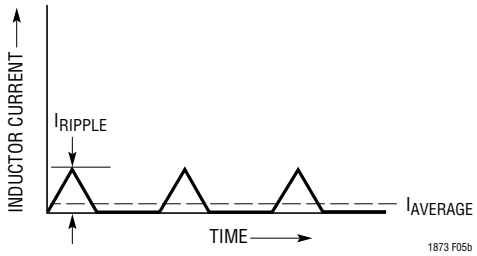


Figure 5b. Discontinuous Mode

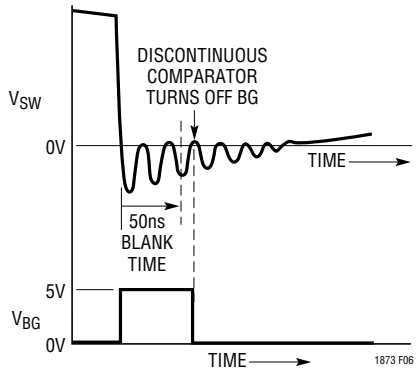


Figure 6. Ringing at SW Causes Discontinuous Comparator to Trip Early

Burst Mode Operation

Discontinuous mode removes a loss term due to resistive drop in QB, but the LTC1873 is still switching QT and QB on and off once a cycle. Each time an external MOSFET is turned on, the internal driver must charge its gate to V_{CC}. Each time it is turned off, that charge is lost to ground. At the high switching frequencies that the LTC1873 operates at, the charge lost to the gates can add up to tens of milliamps from V_{CC}. As the load current continues to drop, this quickly become the dominant power loss term, reducing efficiency once again.

Once again, the LTC1873 switches to a new mode to minimize efficiency loss: Burst Mode operation. As the circuit goes deeper and deeper into discontinuous mode, the total time QT and QB are on reduces. However, the ratio of the time that QT is on to the time that QB is on must remain constant for the output to stay in regulation. An internal timer circuit forces QT to stay on for at least 10% of a normal switching cycle. When the load drops to the point that the output requires less than 10% on-time at QT, the output voltage will begin to rise. The LTC1873 senses this rise and shuts both QT and QB off completely, skipping several switching cycles until the output falls back into range. It then resumes switching in discontinuous mode with QT at 10% duty cycle and the burst sequence repeats. The total deviation from the regulated output is within the 1.5% regulation tolerance of the LTC1873.

In Burst Mode operation, both resistive loss and switching loss are minimized while keeping the output in regulation. The ripple current will be set by the 10% QT on-time and the input supply voltage and is the lowest of all three operating modes. As the load current falls to zero in Burst Mode operation, the most significant loss term becomes the 3mA quiescent current drawn by each side of the LTC1873—usually much less than the minimum load current in a typical low voltage logic system. Burst Mode operation maximizes efficiency at low load currents, but can cause low frequency ripple in the output voltage as the cycle-skipping circuitry switches on and off.

APPLICATIONS INFORMATION

FCB Pin

In some circumstances, it is desirable to control or disable discontinuous and Burst Mode operations. The FCB (Force Continuous Bar) pin allows the user to do this. When the FCB pin is high, the LTC1873 is allowed to enter discontinuous and Burst Mode operations at either side as required. If FCB is taken low, discontinuous and Burst Mode operations are disabled and both sides of the LTC1873 run in continuous mode regardless of load. This does not affect output regulation but does reduce efficiency at low output currents. The FCB pin threshold is specified at 0.8V ±50mV, and includes 20mV of hysteresis, allowing it to be used as a precision small-signal comparator.

Paralleling Outputs

Synchronous regulators (like the LTC1873) are known for their bullheadedness when their outputs are paralleled with other regulators. In particular, a synchronous regulator paralleled with another regulator whose output is slightly higher (perhaps just by millivolts) will happily sink amps of current attempting to pull its own output back down to what it thinks is the right value.

The LTC1873 discontinuous mode allows it to be paralleled with another regulator without fighting. A typical system might use the LTC1873 as a primary regulator and a small LDO as a backup regulator to keep SRAM alive when the main power is off. When the LTC1873 is shut down (by pulling RUN/SS to ground), both QT and QB turn off and the output goes into a high impedance state, allowing the smaller regulator to support the output voltage. However, if the LTC1873 is powered back up in continuous mode, it will begin a soft-start cycle with a low duty cycle, pulling the output down and corrupting the data stored in SRAM. The solution is to tie FCB high, allowing the device to start in discontinuous mode. Any reverse current flow in QB will trip the discontinuous mode circuitry, preventing the LTC1873 from pulling down the output.

OVERVOLTAGE FAULT

The LTC1873 includes a single overvoltage fault flag for both channels: FAULT. FAULT is an open-drain output with an internal 10μA pull-up. If either FB pin rises more than 15% above the nominal 800mV value for more than 25μs, the overvoltage comparator will trip, setting an internal latch. This latch releases the pull-down at FAULT, allowing the 10μA pull-up to take it high. When FAULT goes high, the LTC1873 stops all switching, turns both QB (bottom synchronous) MOSFETs on continuously and remains in this state until both RUN/SS pins are pulled low simultaneously, the power supply is recycled, or the FAULT pin is pulled low externally. This behavior is intended to protect a potentially expensive load from overvoltage damage at all costs. Under some conditions, this behavior can cause the output voltage to undershoot below ground. If latched FAULT mode is used, a Schottky diode should be added with its cathode at the output and its anode at ground to clamp the negative voltage to a safe level and prevent possible damage to the load and the output capacitors.

Note that in overvoltage conditions, the MAX comparator will kick in at just +5%, turning QB on continuously long before the output reaches +15%. Under most fault conditions, this is adequate to bring the output back down without firing the fault latch. Additionally, if MAX successfully keeps the output below +15%, the LTC1873 will resume normal regulation as soon as the output overvoltage fault is resolved.

In some circuits, the OV latch can be a liability. Consider a circuit where the output voltage at one channel may be changed on the fly by changing the VID code or switching in different feedback resistors. A downward adjustment of greater than 15% will fire the fault latch, disabling both sides of the LTC1873 until the power is recycled. In circuits such as this, the fault latch can be disabled by grounding the FAULT pin. The internal latch will still be set the first time the output exceeds +15%, but the 10μA current source pull-up will not be able to pull FAULT high, and the LTC1873 will ignore the latch and continue normal operation. The MAX comparator will act as usual, turning on QB

APPLICATIONS INFORMATION

until output is within range and then allowing the loop to resume normal operation. FAULT can also be pulled down with external open-collector logic to restart a fault-latched LTC1873 as an alternative to recycling the power. Note that this will not reset the internal latch; if the external pull-down is released, the LTC1873 will reenter FAULT mode. To reset the latch, pull both RUN/SS pins low simultaneously or cycle the power.

VID Considerations

Some applications change the VID codes at channel 1 on the fly. This is possible with the LTC1873, but care must be taken to avoid tripping the overvoltage fault circuit. Stepping the voltage upwards abruptly is safe, but stepping down quickly by more than 15% can leave the system in a state where the output voltage is still at the old higher level, but the feedback node is set to expect a new, substantially lower voltage. If this condition persists for more than 25μs, the overvoltage fault circuitry will activate and latch off the LTC1873.

The simplest solution is to disable the fault circuit by grounding the FAULT pin. Systems that must keep the fault circuit active should ensure that the output voltage is never programmed to step down by more than 15% in any single step. A safe strategy is to step the output down by 10% or less at a time and wait for the output to settle to the new value before taking subsequent steps. Regardless of the state of the FAULT pin, the load is always protected against overvoltage faults by the +5% MAX comparator.

EXTERNAL COMPONENT SELECTION

POWER MOSFETs

Getting peak efficiency out of the LTC1873 depends strongly on the external MOSFETs used. The LTC1873 requires at least two external MOSFETs per side—more if one or more of the MOSFETs are paralleled to lower on-resistance. To work efficiently, these MOSFETs must exhibit low $R_{DS(ON)}$ at 5V V_{GS} (3.3V V_{GS} if the PV_{CC} input supply is 3.3V) to minimize resistive power loss while they are conducting current. They must also have low gate charge to minimize transition losses during switching. On the other hand, voltage breakdown requirements in a typical LTC1873 circuit are pretty tame: the 7V maximum input voltage limits the V_{DS} and V_{GS} the MOSFETs can see to safe levels for most devices.

Low $R_{DS(ON)}$

$R_{DS(ON)}$ calculations are pretty straightforward. $R_{DS(ON)}$ is the resistance from the drain to the source of the MOSFET when the gate is fully on. Many MOSFETs have $R_{DS(ON)}$ specified at 4.5V gate drive—this is the right number to use in LTC1873 circuits running from a 5V supply. As current flows through this resistance while the MOSFET is on, it generates I^2R watts of heat, where I is the current flowing (usually equal to the output current) and R is the MOSFET $R_{DS(ON)}$. This heat is only generated when the MOSFET is on. When it is off, the current is zero and the power lost is also zero (and the other MOSFET is busy losing power).

This lost power does two things: it subtracts from the power available at the output, costing efficiency, and it makes the MOSFET hotter—both bad things. The effect is worst at maximum load when the current in the MOSFETs and thus the power lost are at a maximum. Lowering $R_{DS(ON)}$ improves heavy load efficiency at the expense of additional gate charge (usually) and more cost (usually). Proper choice of MOSFET $R_{DS(ON)}$ becomes a trade-off between tolerable efficiency loss, power dissipation and cost. Note that while the lost power has a significant effect on system efficiency, it only adds up to a watt or two in a typical LTC1873 circuit, allowing the use of small, surface mount MOSFETs without heat sinks.

Gate Charge

Gate charge is amount of charge (essentially, the number of electrons) that the LTC1873 needs to put into the gate of an external MOSFET to turn it on. The easiest way to visualize gate charge is to think of it as a capacitance from the gate pin of the MOSFET to SW (for QT) or to PGND (for QB). This capacitance is composed of MOSFET channel charge, actual parasitic drain-source capacitance and Miller-multiplied gate-drain capacitance, but can be approximated as a single capacitance from gate to source. Regardless of where the charge is going, the fact remains

APPLICATIONS INFORMATION

that it all has to come out of V_{CC} to turn the MOSFET gate on, and when the MOSFET is turned back off, that charge all ends up at ground. In the meanwhile, it travels through the LTC1873's gate drivers, heating them up. More power lost!

In this case, the power is lost in little bite-sized chunks, one chunk per switch per cycle, with the size of the chunk set by the gate charge of the MOSFET. Every time the MOSFET switches, another chunk is lost. Clearly, the faster the clock runs, the more important gate charge becomes as a loss term. Old-fashioned switchers that ran at 20kHz could pretty much ignore gate charge as a loss term; in the 550kHz LTC1873, gate charge loss can be a significant efficiency penalty. Gate charge loss can be the dominant loss term at medium load currents, especially with large MOSFETs. Gate charge loss is also the primary cause of power dissipation in the LTC1873 itself.

TG Charge Pump

There's another nuance of MOSFET drive that the LTC1873 needs to get around. The LTC1873 is designed to use N-channel MOSFETs for both QT and QB, primarily because N-channel MOSFETs generally cost less and have lower $R_{DS(ON)}$ than similar P-channel MOSFETs. Turning QB on is no big deal since the source of QB is attached to PGND; the LTC1873 just switches the BG pin between PGND and V_{CC}. Driving QT is another matter. The source of QT is connected to SW which rises to V_{CC} when QT is on. To keep QT on, the LTC1873 must get TG one MOSFET $V_{GS(ON)}$ above V_{CC}. It does this by utilizing a floating driver with the negative lead of the driver attached to SW (the source of QT) and the V_{CC} lead of the driver coming out separately at BOOST. An external 1µF capacitor (C_{CP}) connected between SW and BOOST (Figure 2) supplies power to BOOST when SW is high, and recharges itself through D_{CP} when SW is low. This simple charge pump keeps the TG driver alive even as it swings well above V_{CC}. The value of the bootstrap capacitor C_{CP} needs to be at least 100 times that of the total input capacitance of the topside MOSFET(s). For very large external MOSFETs (or multiple MOSFETs in parallel), C_{CP} may need to be increased beyond the 1µF value.

INPUT SUPPLY

The BiCMOS process that allows the LTC1873 to include large MOSFET drivers on-chip also limits the maximum input voltage to 7V. This limits the practical maximum input supply to a loosely regulated 5V or 6V rail. The LTC1873 will operate properly with input supplies down to about 3V, so a typical 3.3V supply can also be used if the external MOSFETs are chosen appropriately (see the Power MOSFETs section).

At the same time, the input supply needs to supply several amps of current without excessive voltage drop. The input supply must have regulation adequate to prevent sudden load changes from causing the LTC1873 input voltage to dip. In most typical applications where the LTC1873 is generating a secondary low voltage logic supply, all of these input conditions are met by the main system logic supply when fortified with an input bypass capacitor.

INPUT BYPASS CAPACITOR

A typical LTC1873 circuit running from a 5V logic supply might provide 1.6V at 10A at one of its outputs. 5V to 1.6V implies a duty cycle of 32%, which means QT is on 32% of each switching cycle. During QT's on-time, the current drawn from the input equals the load current and during the rest of the cycle, the current drawn from the input is near zero. This 0A to 10A, 32% duty cycle pulse train adds up to $4.7A_{RMS}$ at the input. At 550kHz, switching cycles last about 1.8µs—most system logic supplies have no hope of regulating output current with that kind of speed. A local input bypass capacitor is required to make up the difference and prevent the input supply from dropping drastically when QT kicks on. This capacitor is usually chosen for RMS ripple current capability and ESR as well as value.

The input bypass capacitor in an LTC1873 circuit is common to both channels. Consider our 10A example case with the other side of the LTC1873 disabled. The input bypass capacitor gets exercised in three ways: its ESR must be low enough to keep the initial drop as QT turns on within reason (100mV or so); its RMS current capability must be adequate to withstand the $4.7A_{RMS}$ ripple current at the input and the capacitance must be large enough to maintain the input voltage until the input supply can make

APPLICATIONS INFORMATION

up the difference. Generally, a capacitor that meets the first two parameters will have far more capacitance than is required to keep capacitance-based droop under control. In our example, we need 0.01Ω ESR to keep the input drop under 100mV with a 10A current step and $4.7A_{RMS}$ ripple current capacity to avoid overheating the capacitor. These requirements can be met with multiple low ESR tantalum or electrolytic capacitors in parallel, or with a large monolithic ceramic capacitor.

The two sides of the LTC1873 run off a single master clock and are wired 180° out of phase with each other to significantly reduce the total capacitance/ESR needed at the input. Assuming 100mV of ripple and 10A output current, we needed an ESR of 0.01Ω and 4.7A ripple current capability for one side. Now, assume both sides are running simultaneously with identical loading. If the two sides switched in phase, all the loading conditions would double and we'd need enough capacitance for $9.4A_{RMS}$ and 0.005Ω ESR. With the two sides out of phase, the input current is $4.8A_{RMS}$—barely larger than the single case (Figure 7)! The peak current deltas are still only 10A, requiring the same 0.01Ω ESR rating. As long as the capacitor we chose for the single side application can support the slightly higher $4.8A_{RMS}$ current, we can add the second channel without changing the input capacitor at all. As a general rule, an input bypass capacitor capable of supporting the larger output current channel can support both channels running simultaneously (see the 2-Phase Operation section for more information). Details on how to calculate the maximum RMS input current can be found in Application Note 77.

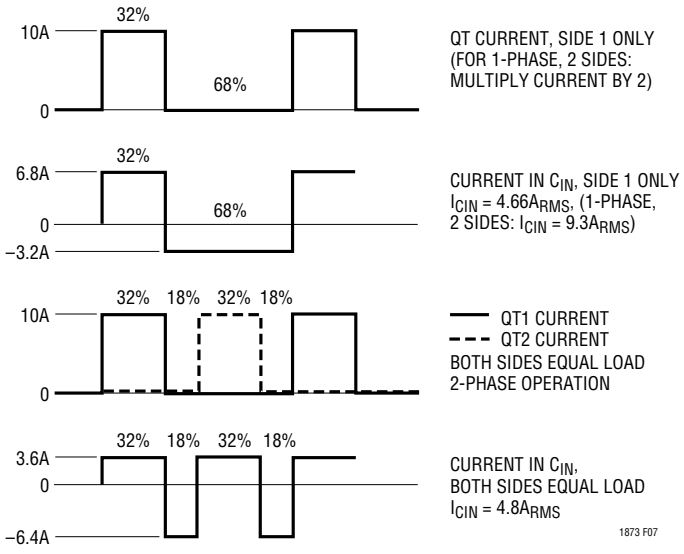


Figure 7. Current Waveforms

Tantalum capacitors are a popular choice as input capacitors for LTC1873 applications, but they deserve a special caution here. Generic tantalum capacitors have a destructive failure mechanism when they are subjected to large RMS currents (like those seen at the input of a LTC1873). At some random time after they are turned on, they can blow up for no apparent reason. The capacitor manufacturers are aware of this and sell special "surge tested" tantalum capacitors specifically designed for use with switching regulators. When choosing a tantalum input capacitor, make sure that it is rated to carry the RMS current that the LTC1873 will draw. If the data sheet doesn't give an RMS current rating, chances are the capacitor isn't surge tested. Don't use it!

OUTPUT BYPASS CAPACITOR

The output bypass capacitor has quite different requirements from the input capacitor. The ripple current at the output of a buck regulator like the LTC1873 is much lower than at the input, due to the fact that the inductor current is constantly flowing at the output whenever the LTC1873 is operating in continuous mode. The primary concern at the output is capacitor ESR. Fast load current transitions at the output will appear as voltage across the ESR of the output bypass capacitor until the feedback loop in the LTC1873 can change the inductor current to match the new load current value. This ESR step at the output is often the single largest budget item in the load regulation calculation. As an example, our hypothetical 1.6V, 10A switcher with a 0.01Ω ESR output capacitor would experience a 100mV step at the output with a 0 to 10A load step—a 6.3% output change!

Usually the solution is to parallel several capacitors at the output. For example, to keep the transient response inside of 3% with the previous design, we'd need an output ESR better than 0.0048Ω. This can be met with three 0.014Ω, 470μF tantalum capacitors in parallel.

APPLICATIONS INFORMATION

INDUCTOR

The inductor in a typical LTC1873 circuit is chosen primarily for value and saturation current. The inductor value sets the ripple current, which is commonly chosen at around 30% of the anticipated full load current. Ripple current is set by:

$$I_{RIPPLE} = \frac{t_{ON(QB)}(V_{OUT})}{L}$$

In our hypothetical 1.6V, 10A example, we'd set the ripple current to 30% of 10A or 3A, and the inductor value would be:

$$L = \frac{t_{ON(QB)}(V_{OUT})}{I_{RIPPLE}} = \frac{(1.2\mu s)(1.6V)}{4A} = 0.5\mu H$$

$$\text{with } t_{ON(QB)} = \left(1 - \frac{1.6V}{5V}\right) / 550kHz = 1.2\mu s$$

The inductor must not saturate at the expected peak current. In this case, if the current limit was set to 15A, the inductor should be rated to withstand 15A + 1/2 I_{RIPPLE}, or 16.5A without saturating.

FEEDBACK LOOP/COMPENSATION

Type 3 Loops

In a typical LTC1873 circuit, the feedback loop consists of the modulator, the external inductor and output capacitor, and the feedback amplifier and its compensation network. All of these components affect loop behavior and need to be accounted for in the loop compensation. The modulator consists of the internal PWM generator, the output MOSFET drivers and the external MOSFETs themselves. From a feedback loop point of view, it looks like a linear voltage transfer function from COMP to SW and has a gain roughly equal to the input voltage. It has fairly benign AC behavior at typical loop compensation frequencies with significant phase shift appearing at half the switching frequency.

The external inductor/output capacitor combination makes a more significant contribution to loop behavior. These components cause a second order LC roll-off at the output, with the attendant 180° phase shift. This roll-off is what filters the PWM waveform, resulting in the desired DC output voltage, but the phase shift complicates the loop compensation if the gain is still higher than unity at the pole frequency. Eventually (usually well above the LC pole frequency), the reactance of the output capacitor will approach its ESR, and the roll-off due to the capacitor will stop, leaving 6dB/octave and 90° of phase shift. See Appendix A, Figure A3. Note that Figure A4 does not apply.

So far, the AC response of the loop is pretty well out of the user's control. The modulator is a fundamental piece of the LTC1873 design, and the external L and C are usually chosen based on the regulation and load current requirements without considering the AC loop response. The feedback amplifier, on the other hand, gives us a handle with which to adjust the AC response. The goal is to have 180° phase shift at DC (so the loop regulates) and something less than 360° phase shift at the point that the loop gain falls to 0dB. The simplest strategy is to set up the feedback amplifier as an inverting integrator, with the 0dB frequency lower than the LC pole (Appendix A, Figure A5). This "type 1" configuration is stable but slow and transient response will be less than exceptional. Also, this circuit configuration cannot count on the MIN and MAX comparators to assist with transient recovery, since they monitor the output at the FB pin which is moving no faster than the integrator pole frequency.

Appendix A, Figure A6 shows an improved "type 2" circuit that uses an additional pole-zero pair to temporarily remove 90° of phase shift. This allows the loop to remain stable with 90° more phase shift in the LC section, provided the loop reaches 0dB gain near the center of the phase "bump." Type 2 loops work well in systems where the ESR zero in the LC roll-off happens close to the LC pole, limiting the total phase shift due to the LC. The additional phase compensation in the feedback amplifier allows the 0dB point to be at or above the LC pole frequency, improving loop bandwidth substantially over a simple type 1 loop. It still has limited ability to compensate for LC combinations where low capacitor ESR keeps the phase shift near 180° for an extended frequency range. Many LTC1873 circuits exhibit this behavior—they require type 3 compensation.

Type 3 loops (Appendix A, Figure A7) use two poles and two zeros to obtain a 180° phase boost in the middle of the frequency band. A properly designed type 3 circuit can

APPLICATIONS INFORMATION

maintain acceptable loop stability even when low output capacitor ESR causes the LC section to approach 180° phase shift well above the initial LC roll-off. As with a type 2 circuit, the loop should cross through 0dB in the middle of the phase bump to maximize phase margin. Because most LTC1873 circuits use low ESR output capacitors, type 3 compensation is usually needed to obtain acceptable phase margin with a high bandwidth feedback loop.

Feedback Component Selection

Selecting the R and C values for a typical type 3 loop is a nontrivial task. The applications shown in this data sheet show typical values, optimized for the power components shown. They should give acceptable performance with similar power components, but will be way off if even one major power component is changed significantly. The only way to ensure proper dynamic behavior and maximize transient response is to recalculate the values specifically for the circuit in question. Appendix A explains feedback component selection in detail. The 25MHz internal op amp in the LTC1873 can generally close a type 3 loop as high as 50kHz before it runs out of bandwidth. Note that channel 1 includes R1 and R_B internally as part of the VID DAC circuitry. R1 is fixed at 20kΩ and R_B varies depending on the VID code selected.

CURRENT LIMIT PROGRAMMING

Programming the current limit on the LTC1873 is straightforward. The I_{MAX} pin sets the current limit by setting the maximum allowable voltage drop across QB (the bottom MOSFET) before the current limit circuit engages. The voltage across QB is set by its on-resistance and the current flowing in the inductor, which is the same as the output current. The LTC1873 current limit circuit inverts the voltage at I_{MAX} before comparing it with the negative voltage across QB, allowing the current limit to be set with a positive voltage.

To set the current limit, calculate the expected voltage drop across QB at the maximum desired current:

$$V_{PROG} = (I_{ILIM})(R_{DS(ON)}) + 100mV$$

I_{LIM} should be chosen to be quite a bit higher than the expected operating current, to allow for MOSFET $R_{DS(ON)}$ changes with temperature. Setting I_{LIM} to 150% of the maximum normal operating current is usually safe and will adequately protect the power components if they are chosen properly. The 100mV term is an approximate factor that corrects for errors caused by ringing on the switch node (illustrated in Figure 6). This factor will change depending on the layout and the components used, but 100mV is usually a good starting point. V_{DROP} is then programmed at the I_{MAX} pin using the internal 10µA pull-up and an external resistor:

$$R_{ILIM} = V_{PROG}/10\mu A$$

The resulting value of R_{ILIM} should be checked in an actual circuit to ensure that the I_{LIM} circuit kicks in as expected. MOSFET $R_{DS(ON)}$ specs are like horsepower ratings in automobiles, and should be taken with a grain of salt. Circuits that use very low values for R_{IMAX} (<20k) should be checked carefully, since small changes in R_{IMAX} can cause large I_{LIM} changes when the 100mV correction factor makes up a large percentage of the total V_{PROG} value. If V_{PROG} is set too low, the LTC1873 may fail to start up.

Accuracy Trade-Offs

The V_{DS} sensing scheme used in the LTC1873 is not particularly accurate, primarily due to uncertainty in the $R_{DS(ON)}$ from MOSFET to MOSFET. A second error term arises from the ringing present at the SW pin, which causes the V_{DS} to look larger than $(I_{LOAD})(R_{DS(ON)})$ at the beginning of QB's on-time. These inaccuracies do not prevent the LTC1873 current limit circuit from protecting itself and the load from damaging overcurrent conditions, but they do prevent the user from setting the current limit to a tight tolerance if more than one copy of the circuit is being built. The 50% factor in the current setting equation above reflects the margin necessary to ensure that the circuit will stay out of current limit at the maximum normal load, even with a hot MOSFET that is running quite a bit higher than its $R_{DS(ON)}$ spec.

APPLICATIONS INFORMATION

FCB OPERATION/SECONDARY WINDINGS

The FCB pin can be used in conjunction with a secondary winding on one side of the LTC1873 to generate a third regulated voltage output. This output can be directly regulated at the FCB pin. In theory, a fourth output could be added, either unregulated or with additional external circuitry at the FCB pin.

The extra auxiliary output is taken from a second winding on the core of the inductor on one channel, converting it into a transformer (Figure 8). The auxiliary output voltage is set by the main output voltage and the turns ratio of the extra winding to the primary winding. Load regulation at the auxiliary output will be relatively good as long as the main output is running in continuous mode. As the load on the main channel drops and the LTC1873 switches to discontinuous or Burst Mode operation, the auxiliary output will not be able to maintain regulation, especially if the load at the auxiliary output remains heavy.

To avoid this, the auxiliary output voltage is divided down with a conventional feedback resistor string with the divided auxiliary output voltage fed back to the FCB pin (Figure 8). The FCB pin threshold is trimmed to 800mV with 20mV of hysteresis, allowing fairly precise control of the auxiliary voltage. If the LTC1873 is in discontinuous or Burst Mode operation and the auxiliary output voltage drops, the FCB pin will trip and the LTC1873 will resume continuous operation regardless of the load on the main output. The FCB pin removes the requirement that power must be drawn from the inductor primary in order to extract power from the auxiliary windings. With the loop in continuous mode, the auxiliary outputs may be loaded without regard to the primary load. Note that if the LTC1873 is already running in continuous mode and the auxiliary output drops due to excessive loading, no additional action can be taken by the LTC1873 to regulate the auxiliary output.

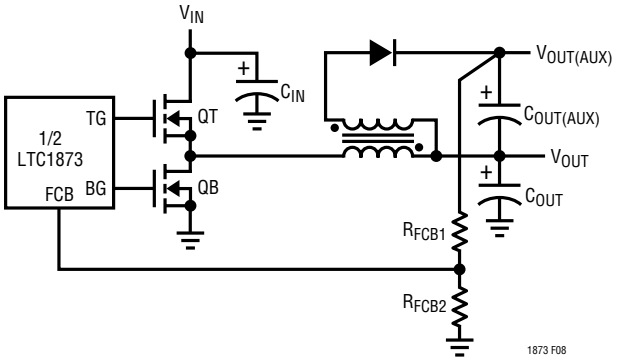


Figure 8. Regulating an Auxiliary Output with the FCB Pin

FAULT FLAG

The FAULT pin is an open-drain output that indicates if one or both of the outputs has exceeded 15% of its programmed output voltage. FAULT includes an internal 10μA pull-up to V_{CC} and does not require an external pull-up to interface to standard logic. FAULT pulls low in normal operation, and releases when a overvoltage fault is detected.

When an overvoltage fault occurs, an internal latch sets and FAULT goes high, disabling the LTC1873 until the latch is cleared by recycling the power or pulling both RUN/SS pins low simultaneously. Alternately, the FAULT pin can be pulled back low externally with an open-collector/open-drain device or an N-channel MOSFET or NPN, which will allow the LTC1873 to resume normal operation, but will not reset the latch. If the pull-down is later removed, the LTC1873 will latch off again unless the latch is reset by cycling the power or RUN/SS pins.

OPTIMIZING PERFORMANCE

Maximizing High Load Current Efficiency

Efficiency at high load currents (when the LTC1873 is operating in continuous mode) is primarily controlled by the resistance of the components in the power path (QT, QB, L_{EXT}) and power lost in the gate drive circuits due to MOSFET gate charge. Maximizing efficiency in this region of operation is as simple as minimizing these terms.

The behavior of the load over time affects the efficiency strategy. Parasitic resistances in the MOSFETs and the inductor set the maximum output current the circuit can supply without burning up. A typical efficiency curve (Figure 9) shows that peak efficiency occurs near 30% of this maximum current. If the load current will vary around the efficiency peak and will spend relatively little time at the

APPLICATIONS INFORMATION

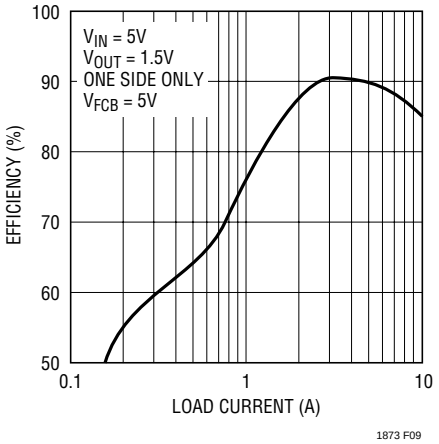


Figure 9. LTC1873 Efficiency Curve for a Typical 10A Circuit

maximum load, choosing components so that the average load is at the efficiency peak is a good idea. This puts the maximum load well beyond the efficiency peak, but usually gives the greatest system efficiency over time, which translates to the longest run time in a battery-powered system. If the load is expected to be relatively constant at the maximum level, the components should be chosen so that this load lands at the peak efficiency point, well below the maximum possible output of the converter.

Maximizing Low Load Current Efficiency

Low load current efficiency depends strongly on proper operation in discontinuous and Burst Mode operations. In an ideally optimized system, discontinuous mode reduces conduction losses but not switching losses, since each power MOSFET still switches on and off once per cycle. In a typical system, there is additional loss in discontinuous mode due to a small amount of residual current left in the inductor when QB turns off. This current gets dissipated across the body diode of either QT or QB. Some LTC1873 systems lose as much to body diode conduction as they save in MOSFET conduction. The real efficiency benefit of discontinuous mode happens when Burst Mode operation is invoked. At typical power levels, when Burst Mode operation is activated, gate drive is the dominant loss term. Burst Mode operation turns off all output switching for several clock cycles in a row, significantly cutting gate drive losses. As the load current in Burst Mode operation falls toward zero, the current drawn by the circuit falls to the LTC1873's background quiescent level—about 3mA per channel.

To maximize low load efficiency, make sure the LTC1873 is allowed to enter discontinuous and Burst Mode operation as cleanly as possible. FCB must be above its 0.8V threshold. Minimize ringing at the SW node so that the discontinuous comparator leaves as little residual current in the inductor as possible when QB turns off. It helps to connect the SW pin of the LTC1873 as close to the drain of QB as possible. An RC snubber network can also be added from SW to PGND.

REGULATION OVER COMPONENT TOLERANCE/ TEMPERATURE

DC Regulation Accuracy

The LTC1873 initial DC output accuracy depends mainly on internal reference accuracy, op amp offset and external resistor accuracy (side 2 only). Two LTC1873 specs come into play: feedback voltage and feedback voltage line regulation. The feedback voltage spec is 800mV ±8mV over the full temperature range, and is specified at the FB pin, which encompasses both reference accuracy and any op amp offset. This accounts for 1% error at the output with a 5V input supply. The feedback voltage line regulation spec adds an additional 0.05%/V term that accounts for change in reference output with change in input supply voltage. With a 5V supply, the errors contributed by the LTC1873 itself typically add up to less than 1% DC error at the output.

At side 2, the output voltage setting resistors (R1 and R_B in Figure 3) are the other major contributor to DC error. At a typical 1.xV output voltage, the resistors are of roughly the same value, which tends to halve their error terms, improving accuracy. Still, using 1% resistors for R1 and R_B will add 1% to the total output error budget, equal to that of all errors due to the LTC1873 combined. Using 0.1% resistors in just those two positions can nearly halve the DC output error for very little additional cost. Side 1 uses the internal VID network to set the output voltage, and is specified to be within ±1.5% of the values shown in Table 1.

APPLICATIONS INFORMATION

Load Regulation

Load regulation is affected by feedback voltage, feedback amplifier gain and external ground drops in the feedback path. Feedback voltage is covered above and is within 1% over temperature. A full-range load step might require a 10% duty cycle change to keep the output constant, requiring the COMP pin to move about 100mV. With amplifier gain at 85dB, this adds up to only a 10μV shift at FB, negligible compared to the reference accuracy terms.

External ground drops aren't so negligible. The LTC1873 can sense the positive end of the output voltage by attaching the feedback resistor directly at the load, but it cannot do the same with the ground lead. Just 0.001Ω of resistance in the ground lead at 10A load will cause a 10mV error in the output voltage—as much as all the other DC errors put together. Proper layout becomes essential to achieving optimum load regulation from the LTC1873. See the Layout/Troubleshooting section for more information. A properly laid out LTC1873 circuit should move less than a millivolt at the output from zero to full load.

TRANSIENT RESPONSE

Transient response is the other half of the regulation equation. The LTC1873 can keep the DC output voltage constant to within 1% when averaged over hundreds of cycles. Over just a few cycles, however, the external components conspire to limit the speed that the output can move. Consider our typical 5V to 1.5V circuit, subjected to a 1A to 5A load transient. Initially, the loop is in regulation and the DC current in the output capacitor is zero. Suddenly, an extra 4A start flowing out of the output capacitor while the inductor is still supplying only 1A. This sudden change will generate a $(4A)(C_{ESR})$voltage step at the output; with a typical 0.015Ω output capacitor ESR, this is a 60mV step at the output, or 4% (for a 1.5V output voltage).

Very quickly, the feedback loop will realize that something has changed and will move at the bandwidth allowed by the external compensation network towards a new duty cycle. If the bandwidth is set to 50kHz, the COMP pin will get to 60% of the way to 90% duty cycle in 3μs. Now the inductor is seeing 3.5V across itself for a large portion of the cycle, and its current will increase from 1A at a rate set by di/dt = V/L. If the inductor value is 0.5μH, the di/dt will be 3.5V/0.5μH or 7A/μs. Sometime in the next few microseconds after the switch cycle begins, the inductor current will have risen to the 5A level of the load current and the output capacitor will stop losing charge.

Note that the output voltage will stop dropping before the inductor current reaches this new output current level. Recall that any practical output capacitor looks like a pure capacitance in series with some amount of ESR. When a load transient hits, virtually all of the initial voltage drop at the output is due to IR drop across the ESR. The output capacitance begins to discharge at the same time and continues until the inductor current rises to match the new output current level.

The output voltage, however, will turn around and start heading the right way before this happens. The next time the top MOSFET turns on, the inductor current will begin increasing linearly. This increasing current flows almost entirely into the capacitor, going through the ESR as it does so (Figure 10). Positive di/dt in the inductor causes positive dv/dt in the ESR, regardless of what the "pure" capacitance is doing. The output voltage will turn around when the positive dv/dt across the ESR exceeds the negative dv/dt across the pure capacitance. If the expected load step (ΔI) is known, an optimum inductor value can be chosen:

$$L \le \left(V_{IN} - V_{OUT}\right) \bullet C \bullet \frac{ESR}{\Delta I}$$

Making L smaller than this optimum value yields little or no improvement in transient response. As the output voltage recovers, the inductor current will briefly rise above the level of the output current to replenish the charge lost from the output capacitor. With a properly compensated loop, the entire recovery time will be inside of 10μs.

Most loads care only about the maximum deviation from ideal, which occurs somewhere in the first two cycles after the load step hits. During this time, the output capacitor does all the work until the inductor and control loop regain control. The initial drop (or rise if the load steps down) is entirely controlled by the ESR of the capacitor and amounts

APPLICATIONS INFORMATION

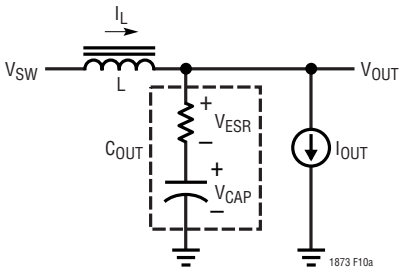


Figure 10a. Capacitor Parasitics Affecting Transient Recovery

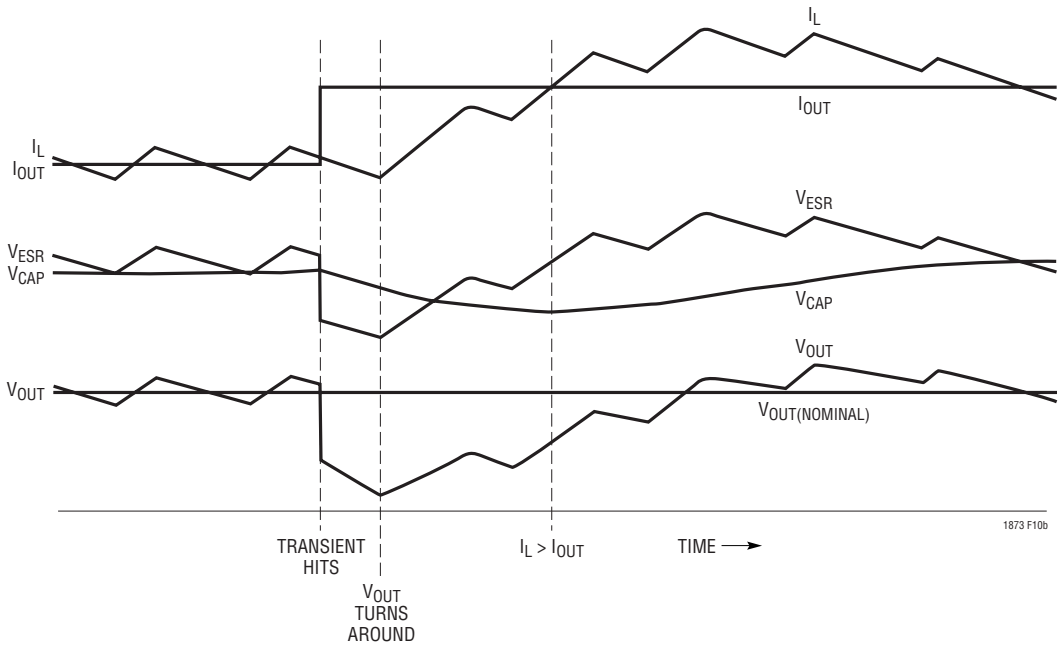


Figure 10b. Transient Recovery Curves

to most of the total voltage drop. To minimize this drop, reduce the ESR as much as possible by choosing low ESR capacitors and/or paralleling multiple capacitors at the output. The capacitance value accounts for the rest of the voltage drop until the inductor current rises. With most output capacitors, several devices paralleled to get the ESR down will have so much capacitance that this drop term is negligible. Ceramic capacitors are an exception; a small ceramic capacitor can have suitably low ESR with relatively small values of capacitance, making this second drop term significant.

Optimizing Loop Compensation

Loop compensation has a fundamental impact on transient recovery time, the time it takes the LTC1873 to recover after the output voltage has dropped due to output capacitor ESR. Optimizing loop compensation entails maintaining the highest possible loop bandwidth while ensuring loop stability. Appendix A describes in detail the techniques used to design an optimized type 3 feedback loop, appropriate for most LTC1873 systems.

APPLICATIONS INFORMATION

Measurement Techniques

Measuring transient response presents a challenge in two respects: obtaining an accurate measurement and generating a suitable transient to use to test the circuit. Output measurements should be taken with a scope probe directly across the output capacitor. Proper high frequency probing techniques should be used. In particular, don't use the 6" ground lead that comes with the probe! Use an adapter that fits on the tip of the probe and has a short ground clip to ensure that inductance in the ground path doesn't cause a bigger spike than the transient signal being measured. Conveniently, the typical probe tip ground clip is spaced just right to span the leads of a typical output capacitor.

Now that we know how to measure the signal, we need to have something to measure. The ideal situation is to use the actual load for the test, and switch it on and off while watching the output. If this isn't convenient, a current step generator is needed. This generator needs to be able to turn on and off in nanoseconds to simulate a typical switching logic load, so stray inductance and long clip leads between the LTC1873 and the transient generator must be minimized.

Figure 11 shows an example of a simple transient generator. Be sure to use a noninductive resistor as the load element—many power resistors use an inductive spiral pattern and are not suitable for use here. A simple solution is to take ten 1/4W film resistors and wire them in parallel to get the desired value. Surface mount resistors are best. This gives a noninductive resistive load which can dissipate 2.5W continuously or 50W if pulsed with a 5% duty cycle, enough for most LTC1873 circuits. Solder the MOSFET and the resistor(s) as close to the output of the LTC1873 circuit as possible and set up the signal generator to pulse at a 100Hz rate with a 5% duty cycle. This pulses the LTC1873 with 500µs transients 10ms apart, adequate for viewing the entire transient recovery time for both positive and negative transitions while keeping the load resistor cool.

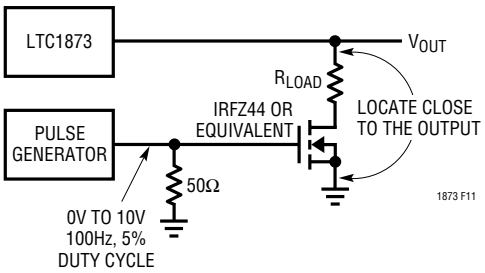


Figure 11. Transient Load Generator

APPENDIX A

THE K FACTOR: A NEW MATHEMATICAL TOOL FOR STABILITY ANALYSIS AND SYNTHESIS

H. Dean Venable
Venable Industries, Inc.
2120 W. Braker Lane, Suite M
Austin, TX 78758
info@venableind.com
http://www.venableind.com

Abstract

Analysis of the stability of feedback loops has always been a subject that was shrouded in mystery and confusion. Recent efforts to clear away some of these problems have helped, but even with computer-aided design, a certain amount of trial-and-error remained. This paper presents a new mathematical concept that is simple but powerful. The techniques described allow synthesis of a feedback amplifier with a few algebraic equations to obtain any desired crossover frequency and phase margin (within reason) on the first try.

1. INTRODUCTION

Stability analysis of feedback loops has historically required a certain amount of trial-and-error. Computer modeling and computer-aided design allowed one to evaluate results of a particular design with relative ease, but it was still difficult to start with a designed result and then determine the exact circuit values required to obtain that result. This paper presents three standardized feedback amplifiers which cover the requirements for every known loop. These amplifiers, together with a new mathematical concept called the K Factor, allow the circuit designer to choose a desired result, i.e., a particular loop cross-over frequency and phase margin, and then determine the necessary component values to achieve these results from a few straight-forward algebraic equations.

Venable Industries, Inc. specializes in the sale and support of computer-controlled Frequency Response Analyzer test systems designed for the power supply industry. Written in 1983, the *K Factor* paper is a mathematical convention that led us to our current product capabilities. Today, Venable's software instantly designs all of the compensation values for this circuit topology and others, automatically calculating values based on test or model data. This feature saves valuable design time. It enables engineers to quickly and accurately measure the frequency response of components and analog circuits as well as test impedance across the frequency domain. Most importantly, the Venable Frequency Response Analyzer system allows engineers to optimally stabilize feedback loops.

2. THE NATURE OF LOOPS

A typical loop is shown in Figure A1. The loop consists of a power-processing block called a MODULATOR in series with an error-detecting block called an AMPLIFIER.

The modulator can be as simple as the buck regulator shown, or it could have been a complex hydraulic servo system or an aircraft attitude control system. No matter how complicated the modulator, the principle is the same: a portion of the output is compared to a reference in an error amplifier, and the difference is amplified and inverted and used as a control input for the modulator to keep the controlled variable constant. Even in multiple-loop systems, there is still one main loop that performs this function.

APPENDIX A

3. WHAT STABILITY MEANS

3.1 The Nature of Stability

There is no problem with a control loop at DC. It is obvious that negative feedback tends to make the controlled output more constant. The problem comes at some higher frequency. Reactive components and time delays cause phase shifts which tend to increase the phase shift around the loop. There is a 180 degree phase shift at DC. At some frequency, the additional phase shift from reactive components and time delays is equal to 180 degrees also, so that an error signal at this frequency will be shifted a total of 360 degrees as it progresses around the loop, and comes back in phase with the original signal. If the net of all the amplitude gains and losses around the loop is one or greater at this frequency, then the error signal is self-perpetuating and the circuit becomes an oscillator. The object of stability analysis is to find a way to keep the total phase shift from reaching 360 degrees before the loop gain falls below unity (0 dB). This is shown graphically in Figure A2. The difference between the actual total phase shift and 360 degrees when the gain is unity is called PHASE MARGIN. The amount the gain is below unity when the total phase shift reaches 360 degrees is called GAIN MARGIN.

3.2 The Importance of Phase

It is possible to stabilize a loop just by reducing the gain of the amplifier until loop cross-over occurs at a frequency well below that where phase shifts from reactive components start to become significant. The problem with this approach is that the response time of the loop to a transient disturbance is slowed down to the point where it is usually unacceptable. In any high-performance loop, the object is to cross over at as high a frequency as possible, while maintaining good phase margin. This is accomplished by tailoring the frequency response of the error amplifier to compensate for some of the modulator phase shift in the region of gain cross-over. A principle objective of this paper is to examine the nature of this "tailoring," and to derive equations that allow loop performance to be predicted without iterative "trial-and-error" procedures.

4. THE NATURE OF MODULATORS

The modulator, or power-processing portion of a circuit, can take many forms. Because of the general nature of modulators, each one has to be analyzed individually. In switching power supplies, however, the transfer function of the modulator usually takes one of two forms: either buck-derived or boost-derived.

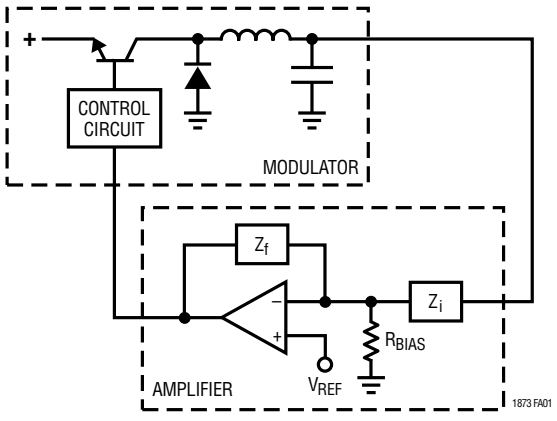


Figure A1. Closed Loop Circuit

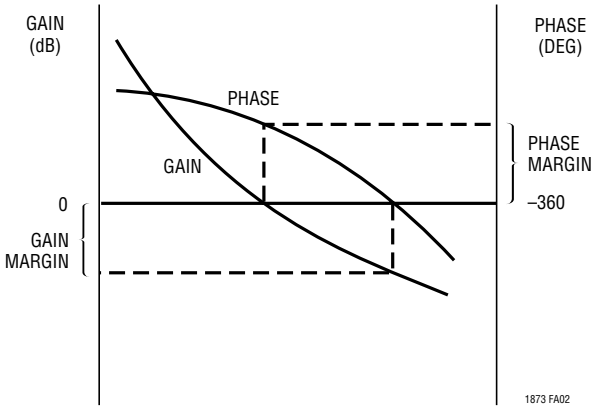


Figure A2. Stability Criteria

APPENDIX A

4.1 Buck-Derived Modulators

Figure A3 shows a typical transfer function of a buck-derived modulator. An electrical transfer function of a circuit is the output voltage divided by the input voltage, with both the magnitude and phase angle of this ratio plotted as a function of frequency. In buck-derived switching regulators with L-C filters, the transfer function usually has some fixed value, A_V, at low frequency, associated with minimal phase shift. At the resonance of the L-C filter, the transfer function breaks to a –2 slope (a –1 slope falls 20 dB/decade, a –2 slope falls 40 dB/decade, etc.). A –2 slope is associated with –180 degrees of phase shift. At some frequency (usually, but not always, higher than the frequency of the L-C corner) the internal resistance of the filter capacitor (ESR) becomes higher than the capacitive reactance, and the slope of the transfer function curve changes to –1 as the filter changes from an L-C filter to an L-R filter. The phase shift associated with a –1 slope is –90 degrees, provided the response is determined by real components.

4.2 Boost-Derived Modulators

Figure A4 shows the transfer function of a boost-derived modulator. The gain portion of a boost-derived modulator looks very much like the gain portion of a buck-derived modulator. There are some major differences in the gain portion, however, and the phase portion is obviously different. Most boost-derived modulators also have a region of fixed gain at low frequency, again associated with a minimal phase shift; however the value of gain in this region is usually a non-linear function of operating point. There is a point in frequency where the transfer function breaks to a –2 slope, as in the buck-derived case, but this frequency is also a function of operating point because the effective value of inductance changes with duty cycle. The phase shift associated with the –2 slope region is the same in either case, –180 degrees. The major problem in boost-derived modulators is caused by a right-half plane zero, a mathematical entity that nevertheless causes real problems. The frequency at which the right-half plane zero occurs is related to the effective value of the filter inductance and the load resistance, and usually occurs at a low enough frequency (typically several kilohertz) that the effect of it must be considered when trying to optimize loop performance. A right-half plane zero causes the gain curve to break from a –2 to a –1 slope, the same as a left-half plane zero, but the phase shifts 90 degrees negative instead of positive. No practical amplifier offers enough phase boost to compensate for this phenomenon, so modulators with boost-derived transfer functions are restricted to cross-over frequencies below the frequency of the right-half plane zero. Recently, Dr. Fred Lee and others have proposed techniques generally referred to as "multiple-loop feedback" methods, wherein

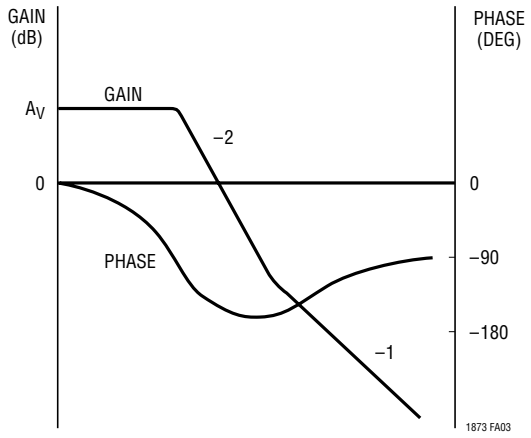


Figure A3. Transfer Function of Buck Modulator

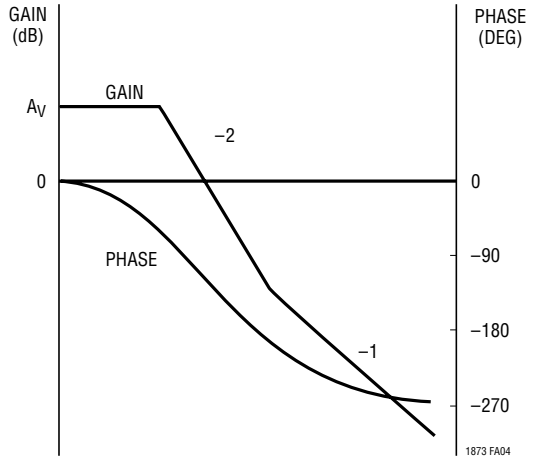


Figure A4. Transfer Function of Boost Modulator

APPENDIX A

a signal from the energy storage inductor is fed into the pulse width modulator circuit to change the basic transfer function of the modulator, eliminating the right-half plane zero, and even reducing the –2 slope portion of the modulator to a –1 slope by using current feedback. These modifications are very helpful in obtaining good performance from boost-derived modulators by changing the basic nature of their transfer functions, but do not change the basic techniques described herein for stabilizing loops. No matter what type of modulator is used, or what modifications are incorporated to change the modulator transfer function, the techniques for stabilization of the loop are exactly the same. One of the three basic amplifiers described below will still suffice to stabilize any loop.

5. THE THREE BASIC AMPLIFIERS

5.1 Fundamental Assumptions

In all cases, it is assumed that a real op-amp is used and that the system is configured so that negative feedback (inversion) is required in the amplifier. It is possible to stabilize loops using the internal error amplifier provided in most PWM chips, but it is difficult to optimize performance since the transfer function is generally based on internal component values which are poorly specified and therefore unpredictable. It is also possible, although difficult, to stabilize loops using an error amplifier in the non-inverting mode. The trouble with this mode is that the gain is restricted to values greater than one, and this is not always compatible with the desired transfer function of the amplifier. For best performance, the internal amplifier of the PWM chip should be wired as an inverting or non-inverting buffer, whichever allows the external error amplifier to be inverting. For the SG1524 family of chips, for example, the internal amplifier should be wired as a non-inverting buffer for positive output voltages and as an inverting buffer for negative output voltages. For the TL494 family of chips, which have the opposite internal sense, the internal amplifier should be wired as an inverting buffer for positive output voltages, and as a non-inverting buffer for negative output voltages.

5.2 Type 1 Amplifier

Figure A5 shows a Type 1 amplifier and its transfer function. The Type 1 amplifier has a single pole at the origin and the gain rolls off at a –1 slope forever, crossing unity gain at the frequency where the reactance of C1 is equal in magnitude to the resistance of R1. This type of amplifier has –270 degrees of phase shift throughout the –1 slope region, and is used to compensate loops where the phase shift of the modulator is minimal, for example, below the L-C filter corner.

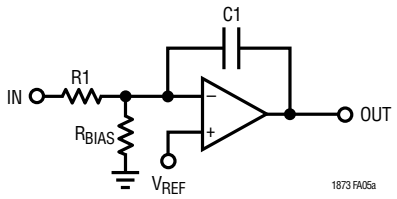


Figure A5a. Type 1 Amplifier Schematic Diagram

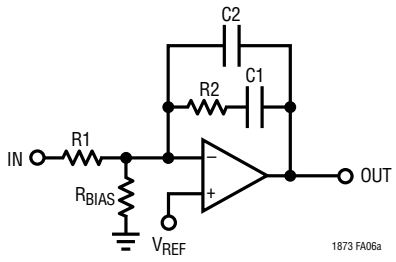


Figure A6a. Type 2 Amplifier Schematic Diagram

5.3 Type 2 Amplifier

Figure A6 shows a Type 2 amplifier and its transfer function. The Type 2 amplifier also has a pole at the origin, but has a zero-pole pair in addition. This zero-pole pair causes a region of zero gain slope and a corresponding phase "bump", or region of reduced phase shift. Whereas the phase shift is –270 degrees throughout the –1 slope regions of the amplifier transfer function, in the zero slope region the phase shift tends toward –180 degrees. The amount of phase shift reduction (size of the "bump") is related to the width of the zero slope region and has a maximum value of 90 degrees. The frequency at which the

APPENDIX A

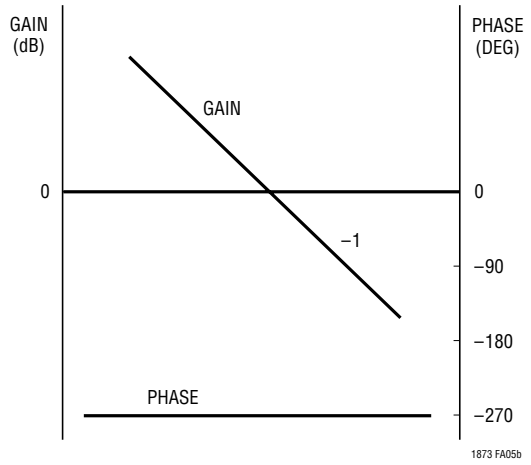


Figure A5b. Type 1 Amplifier Transfer Function

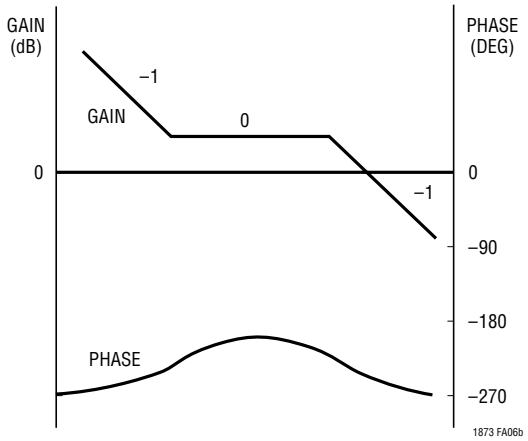


Figure A6b. Type 2 Amplifier Transfer Function

zero occurs is approximately that where R2 takes out C1, that is, where the reactance of C1 is equal in magnitude to the resistance of R2. The frequency at which the pole occurs is approximately that where C2 takes out R2, that is, where the reactance of C2 is equal in magnitude to the resistance of R2. Type 2 amplifiers are used to compensate loops where the phase shift of the modulator portion is approximately –90 degrees. The transfer function of the amplifier is designed so that overall loop cross-over occurs in the center of the zero gain slope region. The zero-pole pair is frequently referred to as a "lead" network. Notice that the output of an amplifier can never lead the input, and that a "lead" network can be more accurately described as a "reduction in lag" network.

5.4 Type 3 Amplifier

Figure A7 shows a Type 3 amplifier and its transfer function. A Type 3 amplifier also has a pole at the origin, but in addition has two zero-pole pair. The two zeros are coincident and the two poles are coincident, resulting in a region of +1 gain slope and a corresponding phase "bump", or region of reduced phase shift. Whereas the phase shift is –270 degrees throughout the –1 slope regions of the amplifier transfer function, in the +1 slope region the phase shift tends toward –90 degrees. The amount of phase shift reduction (size of the "bump") is related to the width of the +1 slope region, and has a maximum value of 180 degrees. The frequency where the two zeros occur is approximately where R2 takes out C1 and C3 takes out R1,

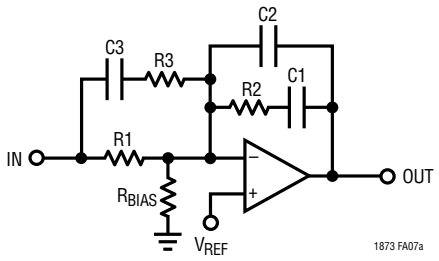


Figure A7a. Type 3 Amplifier Schematic Diagram

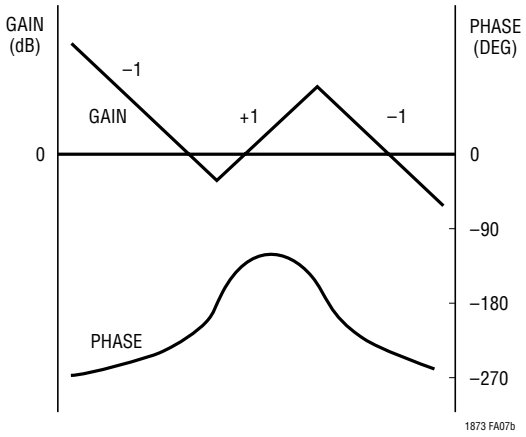


Figure A7b. Type 3 Amplifier Transfer Function

APPENDIX A

and the frequency where the two poles occur is approximately where C2 takes out R2 and R3 takes out C3, where "takes out" means the capacitive reactance is equal in magnitude to the resistance. Type 3 amplifiers are used to compensate loops where the phase shift of the modulator portion is approximately -180 degrees at the frequency of desired loop gain cross-over. The transfer function of the amplifier is designed so that overall loop cross-over occurs in the center of the +1 slope region. Type 3 amplifiers have the most phase boost of any practical amplifier configuration. It is not practical to compensate for more than 180 degrees of phase lag in the modulator portion. If the phase shift of the modulator at the chosen cross-over frequency is greater than 180 degrees, steps should be taken to cross the loop over at a lower frequency (frequency with less phase lag), or modify the modulator circuit to reduce the amount of phase lag at the desired cross-over frequency.

6. THE K FACTOR

6.1 Introduction to the K Factor

The K Factor was originally conceived of as an aid in the synthesis of amplifiers. It is defined as the square root of the ratio of the pole frequency to the zero frequency for Type 2 amplifiers, or the ratio of the double pole frequency to the double zero frequency for Type 3 amplifiers. Figure A8 shows the relationship between the loop cross-over frequency, f, and location of the zeros and poles of the amplifier transfer function. Type 1 amplifiers always have a K of 1. A Type 2 amplifier has a zero at f/K and a pole at Kf, therefore f is the geometric mean of the zero frequency and the pole frequency. The peak phase boost from the zero-pole pair occurs at frequency f, and it is assumed that the amplifier is designed so that overall loop cross-over occurs at frequency f also. For a Type 3 amplifier, the frequency of the double zero is f divided by the square root of K and the frequency of the double pole is f times the square root of K. Frequency f is then the geometric mean between the frequency of the double zero and the frequency of the double pole. The peak of the phase boost from the two zero-pole pair occurs at frequency f, and it assumed that the amplifier is designed such that the overall loop cross-over occurs at frequency f also. In each case, the larger the K, the larger the phase boost.

6.2 Tradeoffs of K Factor Value

There is a penalty associated with using zero-pole pair to increase phase margin that is evident from looking at Figure A8. No matter what type of amplifier is chosen, the K factor is a direct measure of the reduced gain at low frequency and increased gain at high frequency which result from the zero-pole pair, both undesirable side effects of the quest for more phase margin. The K factor can then be thought of the gain penalty that is paid for increased phase margin.

6.3 f/K as a Figure of Merit

To improve overall loop performance, one's first thought is to increase the loop cross-over frequency. If this increase happens to coincide with a frequency range where the modulator phase lag is increasing rapidly, K may have to be increased faster than f to maintain the same phase margin, in which case the low frequency gain will actually suffer from the increased cross-over frequency. The expression f/K can therefore be thought of as a Figure of Merit for a particular amount of phase margin.

7. DERIVATION OF THE K FACTOR

The Type 1 amplifier always has a K of 1, so deriving the K factor for it is not a problem. Also, the mathematics for determining the amount of boost from given locations of amplifier zeros and poles is well understood. The problem that had not been solved was to derive equations that expressed the location of the zeros and poles as a function of phase boost.

7.1 Derivation of K for Type 2 Amplifiers

The expression for the amount of phase boost from a zero-pole pair is well known and has been presented before. The phase shift due to a zero or pole is given by the inverse tangent of ratio of the measurement frequency to the frequency at which the zero or pole is located. The principle of superposition applies, that is, the total amount of phase shift can be determined by summing the individual

APPENDIX A

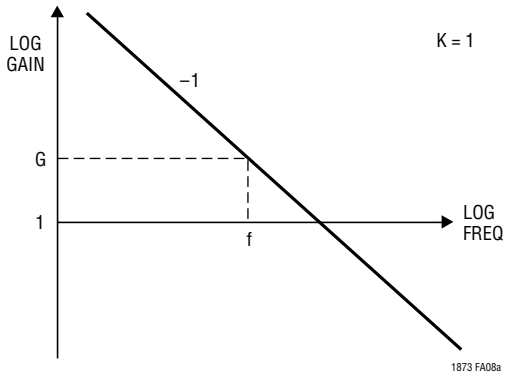


Figure A8a. Type 1 Amplifier

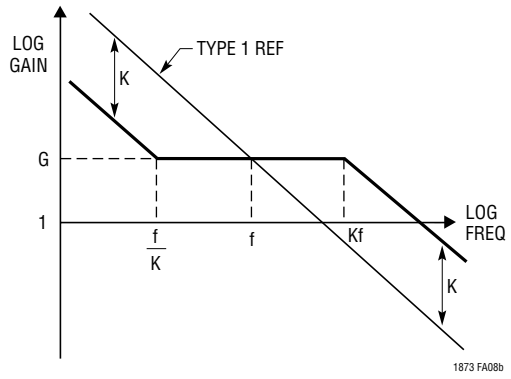


Figure A8b. Type 2 Amplifier

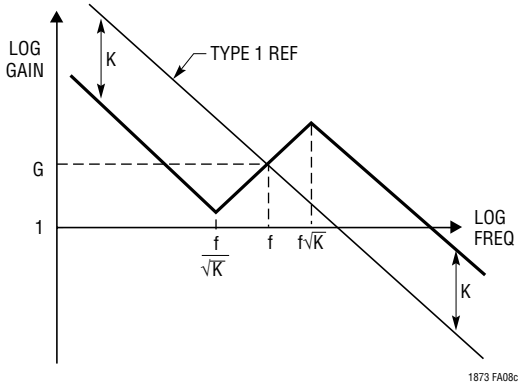


Figure A8c. Type 3 Amplifier

phase shifts of each zero and pole taken individually. The boost at frequency f from a zero at frequency f/K and a pole at frequency Kf is given by the equation:

$$\text{Boost} = \text{Tan}^{-1}(K) - \text{Tan}^{-1}(1/K) \quad (1)$$

From the trigonometric identity,

$$\text{Tan}^{-1}(X) + \text{Tan}^{-1}(1/X) = 90 \text{ degrees} \quad (2)$$

the amount of boost can be determined by substituting (2) in (1):

$$\text{Boost} = \text{Tan}^{-1}(K) + \text{Tan}^{-1}(K) - 90$$
$$= 2\,\text{Tan}^{-1}(K) - 90 \quad (3)$$

From equation (3),

$$\text{Tan}^{-1}(K) = (\text{Boost} + 90)/2$$
$$= (\text{Boost}/2) + 45 \quad (4)$$

Therefore:

$$K = \text{Tan}[(\text{Boost}/2) + 45] \quad (5)$$

Equation (5) is the equation that relates the K factor to the amount of phase boost required from Type 2 amplifiers to achieve the desired phase margin. From this, the exact location of the zeros and poles is established, and the loop cross-over frequency and phase margin may be calculated without trial-and-error.

7.2 Derivation K for Type 3 Amplifiers

Type 3 amplifiers have a double zero at a frequency f divided by the square root of K and a double pole at a frequency f times the square root of K. The phase boost from a single zero-pole pair at these frequencies is given by the equation:

$$\text{Boost} = \text{Tan}^{-1}\sqrt{K} - \text{Tan}^{-1}(1/\sqrt{K}) \quad (6)$$

For 2 zero-pole pairs, where the zeros are coincident and the poles are coincident, there is twice the boost that results from only 1 zero-pole pair, therefore the boost that results from a Type 3 amplifier is:

$$\text{Boost} = 2[\text{Tan}^{-1}\sqrt{K} - \text{Tan}^{-1}(1/\sqrt{K})] \quad (7)$$

APPENDIX A

Incorporating the trigonometric identity given in (2) into (7),

$$\text{Boost} = 2(\text{Tan}^{-1}\sqrt{K} + \text{Tan}^{-1}\sqrt{K} - 90)$$
$$= 2[2(\text{Tan}^{-1}\sqrt{K}) - 90]$$
$$= 4(\text{Tan}^{-1}\sqrt{K}) - 180 \quad (8)$$

Equation (8) can now be rearranged to solve for K:

$$\text{Tan}^{-1}\sqrt{K} = (\text{Boost} + 180)/4$$
$$= (\text{Boost}/4) + 45 \quad (9)$$
$$\sqrt{K} = \text{Tan}\,[(\text{Boost}/4) + 45 \quad (10)$$
$$K = \{\text{Tan}[(\text{Boost}/4) + 45]\}^2 \quad (11)$$

Equation (11) is the final equation expressing the K factor as a function of desired phase boost for a Type 3 amplifier. The location of the double zero and double pole is then established.

8. USING THE K FACTOR

8.1 Preliminary Steps

When using the K factor to synthesize an amplifier to stabilize a feedback loop, certain preliminary steps apply regardless of the type of amplifier chosen. These steps are as follows:

8.1.1 Make Bode Plots of the Modulator

This can be done by analysis or measurement, but preferably by measurement since it is difficult by analysis alone to include all the parasitic effects. Instruments to perform this measurement are called Frequency Response Analyzers. A number of companies manufacture this type of equipment. For switching regulators and similar applications where there is a significant amount of electrical noise present along with the signal, Fourier Integral Analysis machines are far superior to Fast Fourier Transform machines. Venable Industries offers several different complete Frequency Response Analysis Systems, all based on Fourier Integral Analysis machines.

8.1.2 Choose a Cross-over Frequency

The second step in the process is to choose the frequency at which you would like the overall loop gain to be unity. This is f, the cross-over frequency. This is normally chosen to be as high as possible, since higher cross-over frequency normally means faster transient response, and "as high as possible" means where the modulator phase shift is still less than 180 degrees. If the circuit has to be built in volume, where there may be significant differences in component values from unit to unit, or if it will be subjected to wide extremes of line, load, and temperature, it is best not to push the loop to extremes.

8.1.3 Choose the Desired Phase Margin

Pick the amount of phase margin you would like to have at unity gain. A phase margin of 90 degrees means your system is stable as a rock. Phase margin of 60 degrees is a good compromise between fast transient response and stability. Phase margins of 30 degrees or less cause the system to have substantial ringing when subjected to transients, and little tolerance for component or environmental variations.

8.1.4 Determine Required Amplifier Gain

The fourth step is to determine the required amplifier gain at cross-over. The amplifier gain at cross-over must equal the modulator loss, therefore the amplifier gain = 1/modulator gain. If the gain is expressed in dB, then the amplifier gain is simply the negative of the modulator gain.

8.1.5 Calculate Required Phase Boost

Calculate the amount of phase boost required from the zero-pole pair in the amplifier from the formula:

$$\text{Boost} = M - P - 90 \quad (12)$$

where M = Desired Phase Margin (degrees)
and P = Modulator Phase Shift (degrees)

8.1.6 Choose an Amplifier Type

Once the amount of boost required is determined, you can choose what type of amplifier to use.

Type 1 amplifier. The Type 1 amplifier is used where no boost is required. This is the case where a loop is crossed over before the frequency of the L-C corner, for example. This is the simplest type of amplifier and requires the fewest parts.

APPENDIX A

Type 2 amplifier. The Type 2 amplifier is used where the required boost is less than 90 degrees, and is most practical when the required boost is less than about 70 degrees, since a very large K factor is required as the boost approaches 90 degrees. It is used for loops where the modulator gain curve is falling off at about a –1 slope, and the phase shift is about –90 degrees. This is the case in current regulators, or in voltage regulators above the frequency of the ESR zero of the main filter capacitor.

Type 3 amplifier. The Type 3 amplifier is used where the required phase boost is less than 180 degrees. It offers the most boost for a given K factor of any of the amplifier types, but has the highest parts count also. A loop with a Type 3 amplifier will always perform better than one with a Type 1 or Type 2, where "better" is defined as more low frequency gain and less high frequency gain for a given cross-over frequency and amount of phase margin.

8.1.7 Choose a Value for R1

The final preliminary step is to choose a value for R1, the input resistor to the amplifier. This is normally based on how much current you want to draw from the modulator output. If the modulator is a low power, high voltage supply, R1 would typically be very large. If the modulator is a high power, low voltage supply, R1 can usually be selected arbitrarily. The current through R1 should be much larger than the input and bias currents of the operational amplifier used as an error amplifier. Care should be taken not to make the value of R1 too small, however, since all of the other compensation components scale in direct proportion to R1, and a low value for R1 means large values for the compensation capacitors. Large compensation capacitors, in addition to costing more, require more current to drive as a network, and may overload the output of the operational amplifier. A bias resistor, R_{BIAS}, is connected from the inverting input of the error amplifier to ground. This resistor is used to set the DC operating point of the loop, but has no effect on the ac operation, and does not enter into the calculations for cross-over frequency and phase margin.

8.2 Subsequent Steps

After the seven initial steps, the subsequent steps vary, depending on which type of amplifier you chose. In each case, the following notes and definitions apply:

(1) Resistors are in ohms, capacitors are in farads, phase is in degrees, frequency is in hertz, gain is a dimensionless ratio (not dB), and K is a dimensionless ratio.

(2) f = chosen cross-over frequency

(3) G = Amplifier gain at cross-over

(4) K = K factor

(5) R and C values refer to components in the three basic amplifier schematics shown in Figures 5, 6, and 7.

8.2.1 Subsequent Steps - Type 1

The following equations apply to Type 1 amplifiers only:

$$K = 1 \quad (13)$$

$$C1 = 1/(2\pi f G R1) \quad (14)$$

A Type 1 amplifier is somewhat different from the others, in that there is no phase boost. For this reason, the phase margin of the overall loop with a Type 1 amplifier is 90 degrees, less whatever phase lag the modulator has at the chosen cross-over frequency.

8.2.2 Subsequent Steps - Type 2

The following equations apply to Type 2 amplifiers only:

$$K = \mathrm{Tan}[(\mathrm{Boost}/2) + 45] \quad (15)$$

$$C2 = 1/(2\pi f G K R1) \quad (16)$$

$$C1 = C2 (K^2 - 1) \quad (17)$$

$$R2 = K/(2\pi f C1) \quad (18)$$

This completes the synthesis of the Type 2 feedback amplifier. With these component values, the overall loop gain will be unity at frequency f, and the phase margin will be as specified, provided the required boost was between 0 and 90 degrees. It is worthwhile to verify that required amplifier gain at all frequencies is less than the open loop gain of the amplifier, since op amps are not truly ideal devices. Reactance-frequency graph paper is an excellent medium to use for this, since the verification can be done

APPENDIX A

in a few moments and the results provide a better "feel" for the design.

8.2.3 Subsequent Steps - Type 3

The following equations apply to Type 3 amplifiers only:

$$K = \{Tan[(Boost/4) + 45]\}^2 \quad (19)$$

$$C2 = 1/(2\pi f G R1) \quad (20)$$

$$C1 = C2(K - 1) \quad (21)$$

$$R2 = \sqrt{K}/(2\pi f C1) \quad (22)$$

$$R3 = R1/(K - 1) \quad (23)$$

$$C3 = 1/(2\pi f \sqrt{K} R3) \quad (24)$$

This completes the synthesis of a Type 3 feedback amplifier. With these component values, the overall loop gain will be unity at frequency f, and the phase margin will be as specified, provided the required boost is between 0 and 180 degrees. It is worthwhile to verify that the required amplifier gain at all frequencies is less than the open loop gain of the amplifier, since op amps are not truly ideal devices. As with the Type 2 amplifier, reactance-frequency graph paper is an excellent medium to use for this.

8.3 Optimization

It is obvious that there is nothing that can be done to optimize a Type 1 amplifier, other than to choose the proper gain at a particular frequency. There is nothing that can be done to optimize a Type 2 amplifier either, although this may not be so obvious. With the K factor, the gain as well as the location of the zero and pole are determined for a particular operating point, and there is nothing you can do about the performance at other operating points other than live with what you get. It is the Type 3 amplifier that is intriguing, since the K factor assumptions are that the zeros and poles are coincident. What if the zeros and poles are not coincident? What if the zeros or poles or both are spread apart somewhat? Look at Figure 8c. For the same K factor, that is, the same penalty in low frequency gain, spreading the zeros or poles means flattening the sharp corners, moving one zero or pole toward cross-over frequency f, and the other zero or pole away. The net effect of this is to broaden and flatten the phase "bump", so that the phase margin at cross-over is reduced. Optimum performance, that is, the most phase margin for the smallest K factor, is obtained when the zeros and poles are coincident. It may be the case, however, that a particular circuit may have wide excursions of line, load, and temperature, which lead to wide variations in the modulator transfer function. In special cases such as this, it may be advantageous to sacrifice optimum performance at a particular point, in order to gain satisfactory performance over a wide operating range.

9. SUMMARY

Three basic amplifiers were developed which can be used to stabilize any known feedback loop. A new mathematical tool, the K Factor, was developed, and a set of design equations were presented based on the K factor. These design equations allow the precise determination of loop performance without the iterative process normally associated with stability analysis. These techniques have been extensively tested at Venable Industries, and allow even a relatively unskilled person to stabilize a loop with remarkable accuracy and speed.

REFERENCES

(1) Venable, H. Dean, "Practical Techniques for Analyzing, Measuring, and Stabilizing Feedback Control Loops in Switching Regulators and Converters", Proceedings of the Seventh National Power Conversion Conference, POWERCON 7, pp. I2-1 to I2-17, March, 1980.

(2) Venable, H. Dean, "Stability Analysis Made Simple", Rancho Palos Verdes, CA, Venable Industries, 1982.

(3) Middlebrook, R. D., and Cuk, Slobodan, "Advances in Switched-Mode Power Conversion, Volume I", Pasadena, CA TESLAco, 1981.

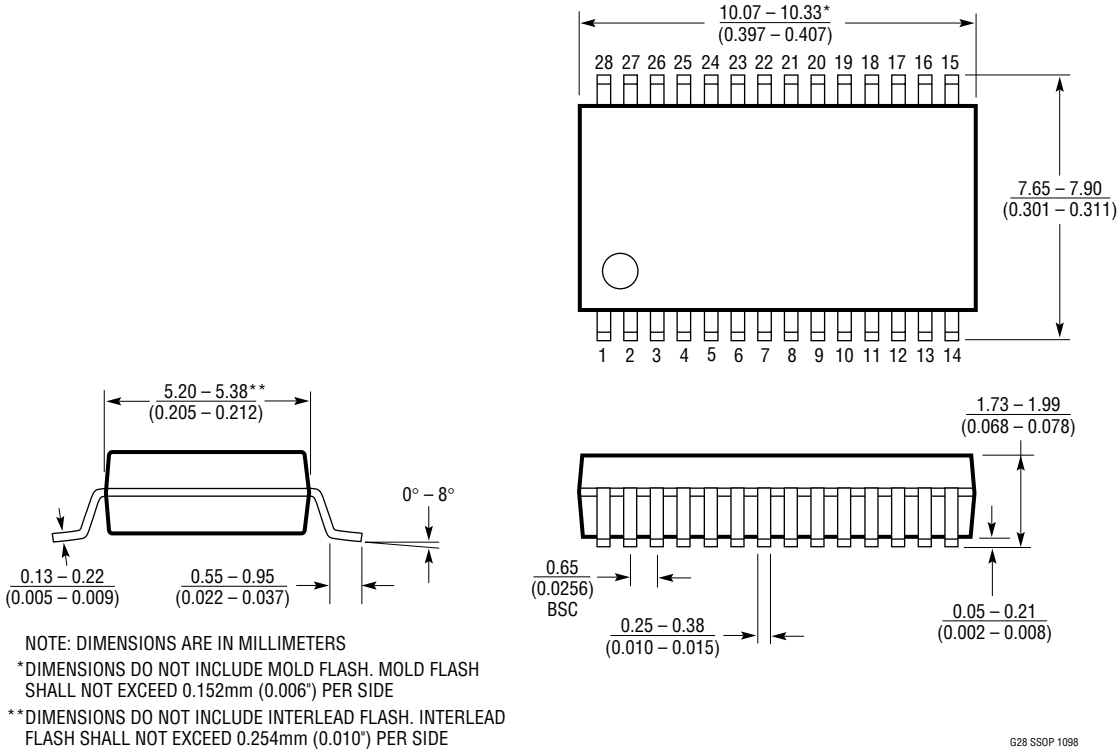
(4) Cuk, Slobodan, and Middlebrook, R. D., "Advances in Switched-Mode Power Conversion, Volume II", Pasadena, CA, TESLAco, 1981.

(5) Lee, F. C., and Yu, Y., "Application Handbook for a Standardized Control Module for DC-DC Converters", NASA Report Volume I and II, NAS3-20102, 1980.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



NOTE: DIMENSIONS ARE IN MILLIMETERS

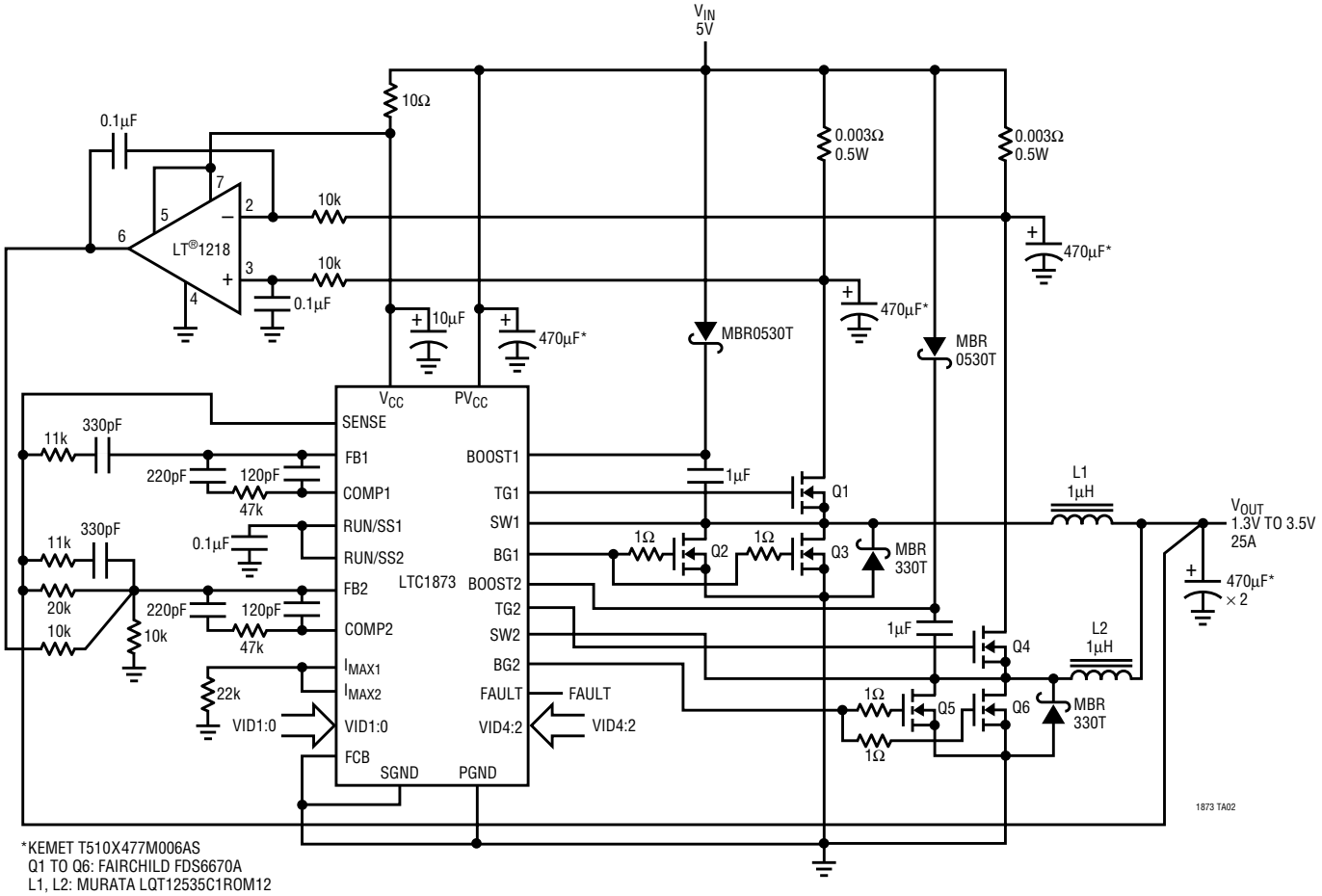
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

G28 SSOP 1098

TYPICAL APPLICATIONS

Single Output, 2-Phase, 25A VID Converter
(V_{IN} = 5V, V_{OUT} = 1.3V to 3.5V)



*KEMET T510X477M006AS
Q1 TO Q6: FAIRCHILD FDS6670A
L1, L2: MURATA LQT12535C1ROM12

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1530	High Power Synchronous Step-Down Controller	SO-8 with Current Limit. No R_{SENSE} Required
LTC1628	Dual High Efficiency 2-Phase Synchronous Step-Down Controller	Constant Frequency, Standby 5V and 3.3V LDOs, 3.5V ≤ V_{IN} ≤ 36V
LTC1702	Dual High Efficiency 2-Phase Synchronous Step-Down Controller	550kHz, 25MHz GBW Voltage Mode, V_{IN} ≤ 7V
LTC1703	Dual 550kHz Synchronous 2-Phase Switching Regulator Controller with Mobile VID	LTC1702 with Mobile VID for Portable Systems
LTC1706-19	VID Voltage Programmer	Adds 4-Bit Mobile VID to All1.19V Referenced Switching Regulators
LTC1706-81	Desktop VID Voltage Programmer	Adds 5-Bit Desktop VID to All 0.8V Referenced Regulators
LTC1709	2-Phase, 5-Bit VID Synchronous Step-Down Controller	Current Mode, V_{IN} to 36V, I_{OUT} Up to 30A
LTC1736	Synchronous Step-Down Controller with 5-Bit VID Control	Fault Protection, PowerGood, 3.5V to 36V Input, Current Mode
LTC1753	5-Bit Programmable Synchronous Switching Rregulator	1.3V to 3.5V Programmable Output Using Internal 5-Bit DAC
LTC1929	2-Phase, Synchronous High Efficiency Converter	Current Mode Ensures Accurate Current Sensing, V_{IN} Up to 36V, I_{OUT} Up to 30A

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com
1873is, sn1873 LT/TP 0999 4K • PRINTED IN USA