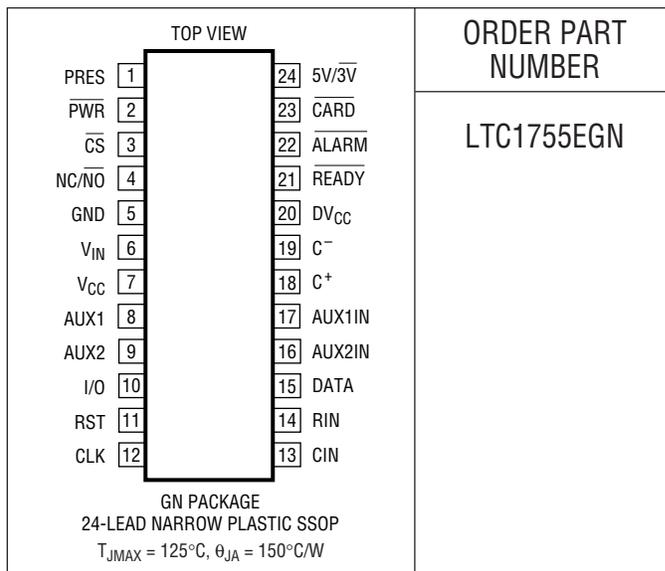


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} to GND	-0.3V to 6.5V
DV_{CC} , V_{CC} to GND	-0.3V to 5.5V
Digital Inputs to GND	-0.3V to ($DV_{CC} + 0.3V$)
CLK, RST, I/O, AUX1, AUX2 to GND	-0.3V to $V_{CC} + 0.3V$
V_{CC} Short-Circuit Duration	Indefinite
Operating Temperature Range (Note 2) ..	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LTC1755EGN

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full specified temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 2.7V$ to $6V$, $DV_{CC} = 2V$ to $5.5V$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply					
V_{IN} Operating Voltage		● 2.7		6	V
DV_{CC} Operating Voltage		● 2.0		5.5	V
I_{VIN} Operating Current	ACTIVE State, $I_{VCC} = 0$	●	50	100	μA
I_{DVCC} Operating Current	ACTIVE State, $DV_{CC} = 3V$	●	10	20	μA
I_{VIN} Shutdown Current	IDLE State, $DV_{CC} = 0V$, $V_{IN} \leq 3.6V$	●		1	μA
	IDLE State, $DV_{CC} = 0V$, $3.6V < V_{IN} \leq 6V$	●		10	μA
	IDLE State, $DV_{CC} = 5.5V$, $V_{IN} \leq 6V$	●		20	μA
V_{CC} Output Voltage	$5V/3V = DV_{CC}$	● 4.75	5.00	5.25	V
	$5V/3V = 0V$	● 2.80	3.00	3.20	V
I_{VCC} Output Current	$5V/3V = 0V$	●			mA
	$3V \leq V_{IN} \leq 6.0V$	● 55			mA
	$5V/3V = DV_{CC}$	● 65			mA
	$3V \leq V_{IN} \leq 6.0V$	●			mA
V_{CC} Turn-On Time	$5V/3V = 0V$	●			mA
	$5V/3V = DV_{CC}$	●			mA
V_{CC} Turn-On Time	$C_{OUT} = 10\mu\text{F}$	●	2.7	12	ms
V_{CC} Discharge Time to 0.4V	$I_{VCC} = 0\text{mA}$, $V_{CC} = 5V$, $C_{OUT} = 10\mu\text{F}$	●	100	250	μs
Controller Inputs/Outputs DATA, AUX1IN, AUX2IN, $DV_{CC} = 3V$					
High Input Voltage Threshold (V_{IH})		● $DV_{CC} - 0.6$	$0.5 \cdot DV_{CC}$		V
Low Input Voltage Threshold (V_{IL})		●	$0.5 \cdot DV_{CC}$	0.3	V
High Level Output Voltage (V_{OH})	Source Current = $20\mu\text{A}$	●	$0.7 \cdot DV_{CC}$		V
Low Level Output Voltage (V_{OL})	Sink Current = $-500\mu\text{A}$ (Note 3)	●		0.3	V
Output Rise/Fall Time	Loaded with 30pF	●		0.5	μs
Input Current (I_{IH}/I_{IL})	$\overline{CS} = DV_{CC}$	●	-1	1	μA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full specified temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 2.7\text{V to }6\text{V}$, $DV_{CC} = 2\text{V to }5.5\text{V}$, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RIN, CIN, PWR, CS, 5V/3V, NC/N0						
High Input Voltage Threshold (V_{IH})		●	$0.7 \cdot DV_{CC}$	$0.5 \cdot DV_{CC}$		V
Low Input Voltage Threshold (V_{IL})		●		$0.5 \cdot DV_{CC}$	$0.2 \cdot DV_{CC}$	V
Input Current (I_{IH}/I_{IL})		●	-1		1	μA
READY, ALARM, CARD						
Pull-Up Current (I_{OH})		●	250			nA
Low Level Output Voltage (V_{OL})	Sink Current = $-20\mu\text{A}$	●			0.3	V
Smart Card Inputs/Outputs I/O, AUX1, AUX2, $V_{CC} = 3\text{V or }5\text{V}$						
High Input Voltage Threshold (V_{IH})	$I_{IH(\text{MAX})} = \pm 20\mu\text{A}$	●	$0.6 \cdot V_{CC}$	$0.5 \cdot V_{CC}$		V
Low Input Voltage Threshold (V_{IL})	$I_{IL(\text{MAX})} = 1\text{mA}$	●		$0.5 \cdot V_{CC}$	0.8	V
High Level Output Voltage (V_{OH})	Source Current = $20\mu\text{A}$ DATA, AUX1IN, AUX2IN = DV_{CC}	●	$0.8 \cdot V_{CC}$			V
Low Level Output Voltage (V_{OL})	Sink Current = -1mA DATA, AUX1IN, AUX2IN = 0V (Note 3)	●			0.3	V
Rise/ Fall Time	Loaded with 30pF	●			0.5	μs
Short-Circuit Current	Shorted to V_{CC}	●		3.5	5	mA
CLK						
High Level Output Voltage (V_{OH})	Source Current = $100\mu\text{A}$	●	$V_{CC} - 0.5$			V
Low Level Output Voltage (V_{OL})	Sink Current = $-200\mu\text{A}$	●			0.3	V
CLK Rise/Fall Time	CLK Loaded with 30pF	●			16	ns
CLK Frequency	CLK Loaded with 30pF	●			5	MHz
RST						
High Level Output Voltage (V_{OH})	Source Current = $200\mu\text{A}$	●	$0.8 \cdot V_{CC}$			V
Low Level Output Voltage (V_{OL})	Sink Current = $-200\mu\text{A}$	●			0.3	V
RST Rise/Fall Time	Loaded with 30pF	●			0.5	μs
PRES						
High Input Voltage Threshold (V_{IH})		●	$0.7 \cdot DV_{CC}$	$0.5 \cdot DV_{CC}$		V
Low Input Voltage Threshold (V_{IL})		●		$0.5 \cdot DV_{CC}$	$0.2 \cdot DV_{CC}$	V
PRES Pull-Up Current		●	0.5	1		μA
PRES Debounce Time	Proportional to the $0.68\mu\text{F}$ Charge Pump Capacitor	●	40	80		ms

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC1755 is guaranteed to meet performance specifications from 0°C to 70°C . Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The DATA, AUX1IN, AUX2IN, AUX1, AUX2 and I/O pull-down drivers must sink up to $250\mu\text{A}$ sourced by the internal current sources.

PIN FUNCTIONS

PRES (Pin 1): (Input) Connects to the Smart Card acceptor's PRESENT indicator switch to detect if a card is inserted. This pin has a pull-up current source so that a grounded switch can be detected with no external components. The pull-up current source is nonlinear, delivering higher current when the PRES pin is above 1V but very little current below 1V. This helps resist false card indications due to leakage current. The activation state of the PRES pin can be set by the NC/NO pin so that both normally open (NO) and normally closed (NC) switches are easily recognized (see NC/NO pin description).

DV_{CC} sets the logic reference level for the PRES pin.

PWR (Pin 2): (Input) A low on the PWR pin places the LTC1755 in the ACTIVE state enabling the charge pump. The READY pin indicates when the card supply voltage (V_{CC}) has reached its final value and communication with the Smart Card is possible. The reset and clock channels are enabled after READY goes low. The three I/O channels are also enabled only after READY goes low, however they may be disabled separately via the CS pin.

The falling edge of PWR latches the state of the 5V/3V pin. After PWR is low, changes on the 5V/3V pin are ignored.

CS (Pin 3): (Input) The CS pin enables the three bidirectional I/O channels of the LTC1755. When the I/O channels are disabled the Smart Card pins (I/O, AUX1, AUX2) are forced to logic one and the controller pins (DATA, AUX2IN, AUX1IN) are high impedance. CS can be brought low along with PWR when the device is first enabled, however communication with the Smart Card is inhibited until V_{CC} reaches its final value as indicated by a low on the READY pin.

DV_{CC} sets the logic reference level for the CS pin.

NC/NO (Pin 4): (Input) This pin controls the activation level of the PRES pin. When it is high (DV_{CC}) the PRES pin is active high. When it is low (GND) the PRES pin is active low. In either case the presence of a Smart Card is indicated by a low on the CARD output. When a ground side normally open (NO) switch is used the NC/NO pin should be grounded. When a ground side normally closed (NC) switch is used the NC/NO pin should be connected to DV_{CC} .

Note: If a normally closed switch is used, a small current (several microamperes) will flow through the switch whenever a Smart Card is not present. For ultralow power consumption in shutdown, a normally open switch is optimum.

DV_{CC} sets the logic reference level for the NC/NO pin.

GND (Pin 5): Ground Reference for the IC. This pin should be connected to a low impedance ground plane. Bypass capacitors for V_{IN} and V_{CC} should be in close proximity to the GND pin.

V_{IN} (Pin 6): Supply Voltage for the Charge Pump. May be between 2.7V and 6V. A 10 μ F low ESR ceramic bypass capacitor is required on this pin for optimum performance.

V_{CC} (Pin 7): Regulated Smart Card Supply Voltage. This pin should be connected to the Smart Card V_{CC} contact. The 5V/3V pin determines the V_{CC} output voltage.

The V_{CC} pin is protected against short circuits by comparing the actual output voltage with an internal reference voltage. If V_{CC} is below its correct level (for as little as 5 μ s) the LTC1755 switches to the Alarm state (see the State Diagram). The V_{CC} pin requires a 10 μ F charge storage capacitor to ground. For optimum performance a low ESR ceramic capacitor should be used.

During the Idle and Alarm states the V_{CC} pin is rapidly discharged to ground to comply with the deactivation requirements of the EMV and ISO-7816 specifications.

AUX1 (Pin 8): (Input/Output) Smart Card Side Auxiliary I/O Pin. This pin is used for auxiliary bidirectional data transfer between the microcontroller and the Smart Card. It has the same characteristics as the I/O pin.

AUX2 (Pin 9): (Input/Output) Smart Card Side Auxiliary I/O Pin. This pin is used for auxiliary bidirectional data transfer between the microcontroller and the Smart Card. It has the same characteristics as the I/O pin.

I/O (Pin 10): (Input/Output) Smart Card Side Data I/O Pin. This pin is used for bidirectional data transfer between the microcontroller and the Smart Card. It should be connected to the Smart Card I/O contact. The Smart Card I/O pin must be able to sink up to 250 μ A when driving the I/O pin low

PIN FUNCTIONS

due to the pull-up current source. The I/O pin becomes a low impedance to ground during the Idle state. It does not become active until $\overline{\text{READY}}$ goes low indicating that V_{CC} is stable.

Once $\overline{\text{READY}}$ is low the I/O pin is protected against short circuits to V_{CC} by current limiting to 5mA maximum.

The DATA-I/O channel is bidirectional for half-duplex transmissions. Its idle state is H-H. Once an L is detected on one side of the channel the direction of transmission is established. Specifically, the side which received an L first is now the input, and the opposite side is the output. Transmission from the output side back to the input side is inhibited, thereby preventing a latch condition. Once the input side releases its L, both sides return to H, and the channel is now ready for a new L to be transmitted in either direction. If an L is forced externally on the output side, and it persists until after the L on the input side is released, this illegal input will not be transmitted to the input side because the transmission direction will not have changed. The direction of transmission can only be established from the idle (H-H) state and is determined by the first receipt of an L on either side.

RST (Pin 11): (Output) Level-Shifted Reset Output Pin. This pin should be connected to the Smart Card RST contact. The RST pin becomes a low impedance to ground during the Idle state (see the State Diagram). The reset channel does not become active until the $\overline{\text{READY}}$ signal goes low indicating that V_{CC} is stable.

Short-circuit protection is provided on the RST pin by comparing RST with R_{IN} . If these signals differ for several microseconds then the LTC1755 switches to the Alarm state. This fault checking is only performed after the V_{CC} pin has reached its final value (as indicated by the $\overline{\text{READY}}$ pin).

CLK (Pin 12): (Output) Level-Shifted Clock Output Pin. This pin should be connected to the Smart Card CLK contact. The CLK pin becomes a low impedance to ground during the Idle state (see the State Diagram). The clock channel does not become active until the $\overline{\text{READY}}$ signal goes low indicating that V_{CC} is stable.

Short-circuit protection is provided on the CLK pin by comparing CLK with C_{IN} . If these signals differ for several microseconds then the LTC1755 switches to the Alarm state. This fault checking is only performed after the V_{CC} pin has reached its final value (as indicated by the $\overline{\text{READY}}$ pin).

The clock channel is optimized for signal integrity in order to meet the stringent duty cycle requirements of the EMV specification. Therefore, to reduce power in low power applications, clock stop mode is recommended when data is not being exchanged.

CIN (Pin 13): (Input) Clock Input Pin from the Microcontroller. During the Active state this signal appears on the CLK pin after being level-shifted and buffered.

DV_{CC} sets the logic reference level for the C_{IN} pin.

RIN (Pin 14): (Input) Reset Input Pin from the Microcontroller. During the Active state this signal appears on the RST pin after being level-shifted and buffered.

DV_{CC} sets the logic reference level for the R_{IN} pin.

DATA (Pin 15): (Input/Output) Microcontroller Side Data I/O Pin. This pin is used for bidirectional data transfer between the microcontroller and the Smart Card. The microcontroller data pin must be open drain and must be able to sink up to 250 μA when driving the DATA pin low due to the pull-up current source. The DATA pin becomes high impedance during the Idle state or when CS is high (see the State Diagram). It does not become active until the $\overline{\text{READY}}$ signal goes low indicating that V_{CC} is stable.

AUX2IN (Pin 16): (Input/Output) Microcontroller Side Auxiliary I/O pin. This pin is used for bidirectional auxiliary data transfer between the microcontroller and the Smart Card. It has the same characteristics as the DATA pin.

AUX1IN (Pin 17): (Input/Output) Microcontroller Side Auxiliary I/O Pin. This pin is used for bidirectional auxiliary data transfer between the microcontroller and the Smart Card. It has the same characteristics as the DATA pin.

C⁺, C⁻ (Pins 18, 19): Charge Pump Flying Capacitor Terminals. Optimum values for the flying capacitor range from 0.68 μF to 1 μF . Best performance is achieved with a low ESR X7R ceramic capacitor.

PIN FUNCTIONS

DV_{CC} (Pin 20): Supply Voltage for the Microcontroller Side Digital Input and Input/Output Pins (Typically 3V). If the charge pump input pin (V_{IN}) is powered from the same source as the microcontroller, then DV_{CC} should be connected directly to V_{IN} . In this case only one (10 μ F) input bypass capacitor is needed for the LTC1755. If the DV_{CC} pin is powered separately then it should be bypassed separately with a 0.1 μ F capacitor. The DV_{CC} pin may be between 2V and 5.5V.

The DV_{CC} pin is monitored for adequate voltage. If DV_{CC} drops below approximately 1.5V the LTC1755 automatically enters the Idle state.

READY (Pin 21): (Output) Readiness Indicator of the Smart Card Supply Voltage (V_{CC}). When the LTC1755 is placed in the Active state the soft start feature slowly ramps the V_{CC} voltage. A low on the READY pin indicates that V_{CC} has reached its final value.

The READY pin is configured as an open-drain pull-down with a weak pull-up current source. This permits wired-OR connections of multiple LTC1755s to a single microcontroller.

ALARM (Pin 22): (Output) A low on this pin indicates that a fault has occurred and that the LTC1755 is in the Alarm state (see the State Diagram). Possible faults include V_{CC} underrange for at least 5 μ s, overtemperature shutdown, CLK or RST invalid output levels, and card removal during the Active state.

CLK or RST invalid and overtemperature faults are detected only after V_{CC} has reached its final value (as indicated by the READY pin). V_{CC} underrange and card removal during Active faults are detected at any time during the Active period (i.e., once $\overline{PWR} = 0V$).

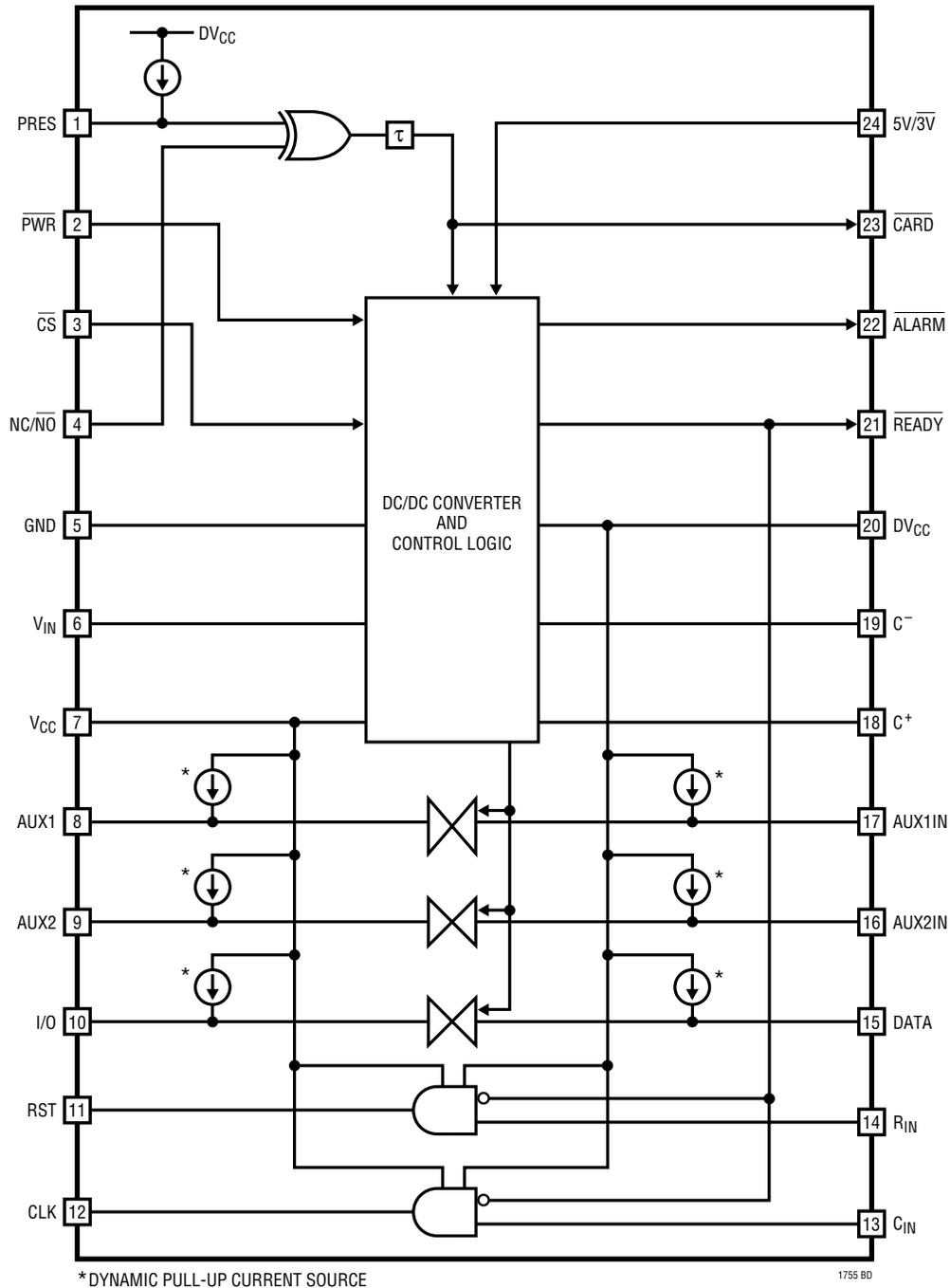
The ALARM pin is configured as an open-drain pull-down with a weak pull-up current source. This permits wired-OR connections of multiple LTC1755s to a single microcontroller.

CARD (Pin 23): (Output) Level-Shifted and Debounced PRES Signal from the Smart Card Acceptor Switch. When a valid card indication appears, this pin communicates the presence of the Smart Card to the microcontroller. The CARD pin has an open-drain active pull-down with a weak pull-up current source for logic-OR connections. The debounce circuit ensures that a card has been present for a continuous period of at least 40ms before asserting CARD low. The CARD pin returns high within 50 μ s of card removal. The PRES pin, in conjunction with the NC/NO pin, determines if a card is present.

5V/3V (Pin 24): (Input) Controls the output voltage (V_{CC}) of the DC/DC converter during the Active state. A valid high sets V_{CC} to 5V. A valid low sets V_{CC} to 3V. The 5V/3V pin is latched on the falling edge of the PWR pin. When PWR is low, changes on the 5V/3V pin are ignored. To change the voltage on V_{CC} the LTC1755 must first be returned to the Idle state by bringing the PWR pin high.

DV_{CC} sets the logic reference level for the 5V/3V pin.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

10kV ESD Protection

All Smart Card pins (CLK, RST, I/O, AUX1, AUX2, V_{CC} and GND) can withstand over 10kV of human body model ESD in situ. In order to ensure proper ESD protection, careful board layout is required. The GND pin should be tied directly to a ground plane. The V_{CC} capacitor should be located very close to the V_{CC} pin and tied immediately to the ground plane.

Capacitor Selection

The style and value of capacitors used with the LTC1755 determine several parameters such as output ripple voltage, charge pump strength, Smart Card switch debounce time and V_{CC} discharge rate.

Due to the switching nature of a capacitive charge pump, low equivalent series resistance (ESR) capacitors are recommended for the capacitors at V_{IN} and V_{CC} . Whenever the flying capacitor is switched to the V_{CC} charge storage capacitor, considerable current flows. The product of this high current and the ESR of the output capacitor can generate substantial voltage spikes on the V_{CC} output. These spikes may cause problems with the Smart Card or may interfere with the regulation loop of the LTC1755. Therefore, ceramic or tantalum capacitors are recommended rather than higher ESR aluminum capacitors. Between ceramic and tantalum, ceramic capacitors generally have the lowest ESR. Some manufacturers have developed low ESR tantalum capacitors but they can be expensive and may still have higher ESR than ceramic types. Thus, while they cannot be avoided, ESR spikes will typically be lowest when using ceramic capacitors.

For ceramic capacitors there are several different materials available to choose from. The choice of ceramic material is generally based on factors such as available capacitance, case size, voltage rating, electrical performance and cost. For example, capacitors made of Y5V material have high packing density, which provides high capacitance for a given case size. However, Y5V capacitors tend to lose considerable capacitance over the -40°C to 85°C temperature range. X7R ceramic capacitors are more stable over temperature but don't provide the high packing density. Therefore, large capacitance values are generally not available in X7R ceramic.

The value and style of the flying capacitor are important not only for the charge pump but also because they provide the large debounce time for the Smart Card detection channel. A $0.68\mu\text{F}$ X7R capacitor is a good choice for the flying capacitor because it provides fairly constant capacitance over temperature and its value is not prohibitively large.

The charge storage capacitor on the V_{CC} pin determines the ripple voltage magnitude and the discharge time of the Smart Card voltage. To minimize ripple, generally, a large value is needed. However, to meet the V_{CC} discharge rate specification, the value should not exceed $20\mu\text{F}$. A $10\mu\text{F}$ capacitor can be used but the ripple magnitude will be higher leading to worse apparent DC load regulation. Typically a $15\mu\text{F}$ to $18\mu\text{F}$ Y5V ceramic capacitor is the best choice for the V_{CC} charge storage capacitor. For best performance, this capacitor should be connected as close as possible to the V_{CC} and GND pins. Note that most of the electrostatic discharge (ESD) current on the six Smart Card pins is absorbed by this capacitor.

The bypass capacitor at V_{IN} is also important. Large dips on the input supply due to ESR may cause problems with the internal circuitry of the LTC1755. A good choice for the input bypass capacitor is a $10\mu\text{F}$ Y5V style ceramic

Dynamic Pull-Up Current Sources

The current sources on the bidirectional pins (DATA, AUX2IN, AUX1IN, I/O, AUX2 and AUX1) are dynamically activated to achieve a fast rise time with a relatively small static current (Figure 1). Once a bidirectional pin is relinquished, a small start-up current begins to charge the node. An edge rate detector determines if the pin is released by comparing its slew rate with an internal

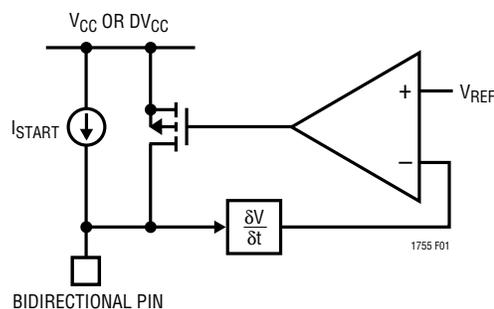


Figure 1. Dynamic Pull-Up Current Sources

APPLICATIONS INFORMATION

reference value. If a valid transition is detected, a large pull-up current enhances the edge rate on the node. The higher slew rate corroborates the decision to charge the node thereby effecting a dynamic form of hysteresis. Once the node has reached the power supply voltage the internal comparator requires several hundred nanoseconds to reset. Pulling down on the pin before the reset delay expires will result in a momentary contention and a higher current flow. Therefore, the comparator delay sets the upper limit on the maximum data rate of the bidirectional channels to about 500kHz.

Synchronous Card Applications

For multcard synchronous applications the LTC1755 has separate control pins for the CLK and I/O lines. The $\overline{\text{PWR}}$ pin enables the charge pump as well as the CLK and RST channels while the $\overline{\text{CS}}$ pin enables only the bidirectional channels. In multcard applications the $\overline{\text{CS}}$ pin can be used to disable communication to one card while leaving its clock line running. With this option the same I/O pin can be used for multiple cards. For simpler applications the $\overline{\text{CS}}$ and $\overline{\text{PWR}}$ pins can be connected together to enable or disable the entire chip.

Low Power Operation

The LTC1755 is inherently a low power device. When there is no Smart Card present the supply current is less than $10\mu\text{A}$. If DV_{CC} is 0V the current drops below $1\mu\text{A}$. When a Smart Card is present the LTC1755 operates with a quiescent current of only $60\mu\text{A}$, thus the majority of power is consumed by charge pump losses and the card itself. If the card can be made to consume less power during idle times a significant power savings will be achieved. Whenever possible Clock Stop Mode should be used (or alternatively a very low “idling” clock speed). Furthermore, in the Active state, the bidirectional pins should all be relinquished whenever possible since there is some static current flow when a bidirectional pin is pulled down.

Overtemperature Fault Protection

An overtemperature circuit disables the chip and activates the $\overline{\text{ALARM}}$ pin if the IC's junction temperature exceeds 150°C .

Self-Start Mode

By connecting the $\overline{\text{CARD}}$ pin to the $\overline{\text{CS}}$ and $\overline{\text{PWR}}$ pins the LTC1755 can be made to start up automatically when a Smart Card is detected (Figure 2). In this mode, the $\overline{\text{READY}}$ pin becomes an interrupt signal indicating to the microcontroller that a Smart Card is present and that V_{CC} , the charge pump voltage, is at its final value. The Smart Card remains powered as long as it is detected by the $\overline{\text{PRES}}$ pin. When the Smart Card is removed the LTC1755 will automatically be deactivated by the fault detection circuitry.

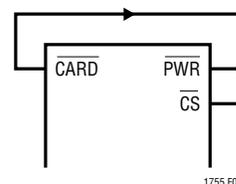


Figure 2. Self-Start Mode

Deactivation Sequence

For maximum flexibility the Smart Card can be deactivated either manually or automatically. In manual mode the deactivation is controlled by explicitly manipulating the LTC1755 input and control pins (DATA, AUX1IN, AUX2IN, RIN and CIN followed by $\overline{\text{PWR}}$ and $\overline{\text{CS}}$). In automatic mode the $\overline{\text{PWR}}$ pin is used to perform the built-in deactivation sequence. Once $\overline{\text{PWR}}$ is brought high the built-in deactivation sequence occurs as follows:

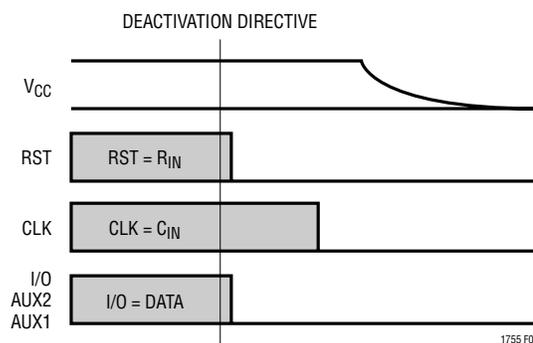


Figure 3. Deactivation Sequence

In the event of a fault, the LTC1755 automatically implements the built-in deactivation sequence.

APPLICATIONS INFORMATION

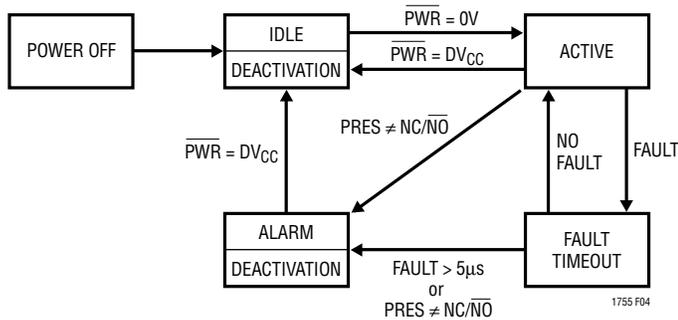


Figure 4. LTC1755 State Diagram

State Definitions

IDLE/DEACTIVATION

V_{CC} , RST, CLK, I/O AUX2, AUX1 = L

\overline{READY} , \overline{ALARM} , DATA, AUX2IN, AUX1IN = Z

$\overline{CARD} = \overline{PRES} \oplus \overline{NC/NO}$

Once the LTC1755 enters the Idle/Deactivation state the deactivation sequence begins. The deactivation sequence will continue until V_{CC} is discharged to approximately 1V. An activation command ($\overline{PWR} = 0V$) will only be acknowledged once this occurs.

ALARM/DEACTIVATION

Same as Idle/Deactivation except:

$\overline{ALARM} = L$

The only possible next state is Idle/Deactivation which is achieved by disabling the LTC1755 via the \overline{PWR} pin (i.e., $\overline{PWR} = DV_{CC}$).

The alarm indication can be cleared by rapidly cycling the \overline{PWR} pin. However, a new activation cycle will not begin until V_{CC} is or has dropped below approximately 1V.

ACTIVE

$V_{CC} = 3V$ or $5V$ (as determined by the $5V/3V$ pin)

RST = R_{IN} , CLK = C_{IN}

I/O, AUX2, AUX1, DATA, AUX2IN, AUX1IN = Ready for data (after \overline{READY} becomes low)

$\overline{CARD} = \overline{PRES} \oplus \overline{NC/NO}$

$\overline{ALARM} = H$

FAULT TIMEOUT

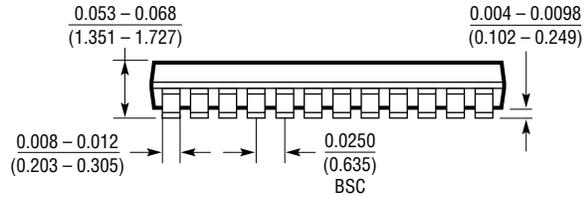
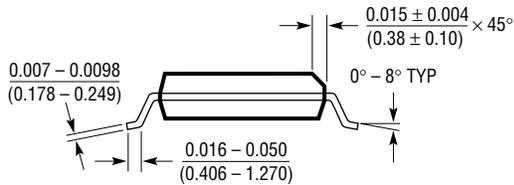
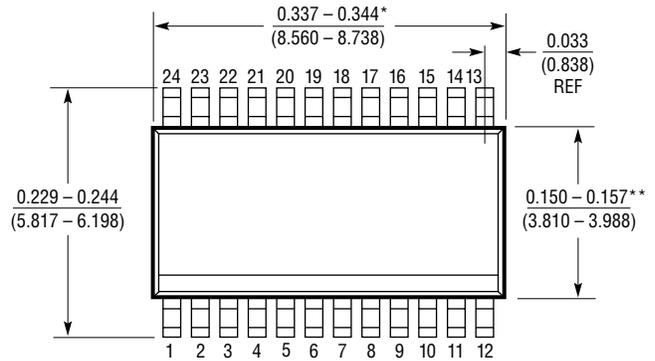
Same as Active except:

The duration of a fault is being measured. If the fault duration exceeds $5\mu s$ then the Alarm/Deactivation state follows. If the fault duration is less than $5\mu s$, then the device is returned to the Active state.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
24-Lead Plastic SSOP (Narrow 0.150)
 (LTC DWG # 05-08-1641)

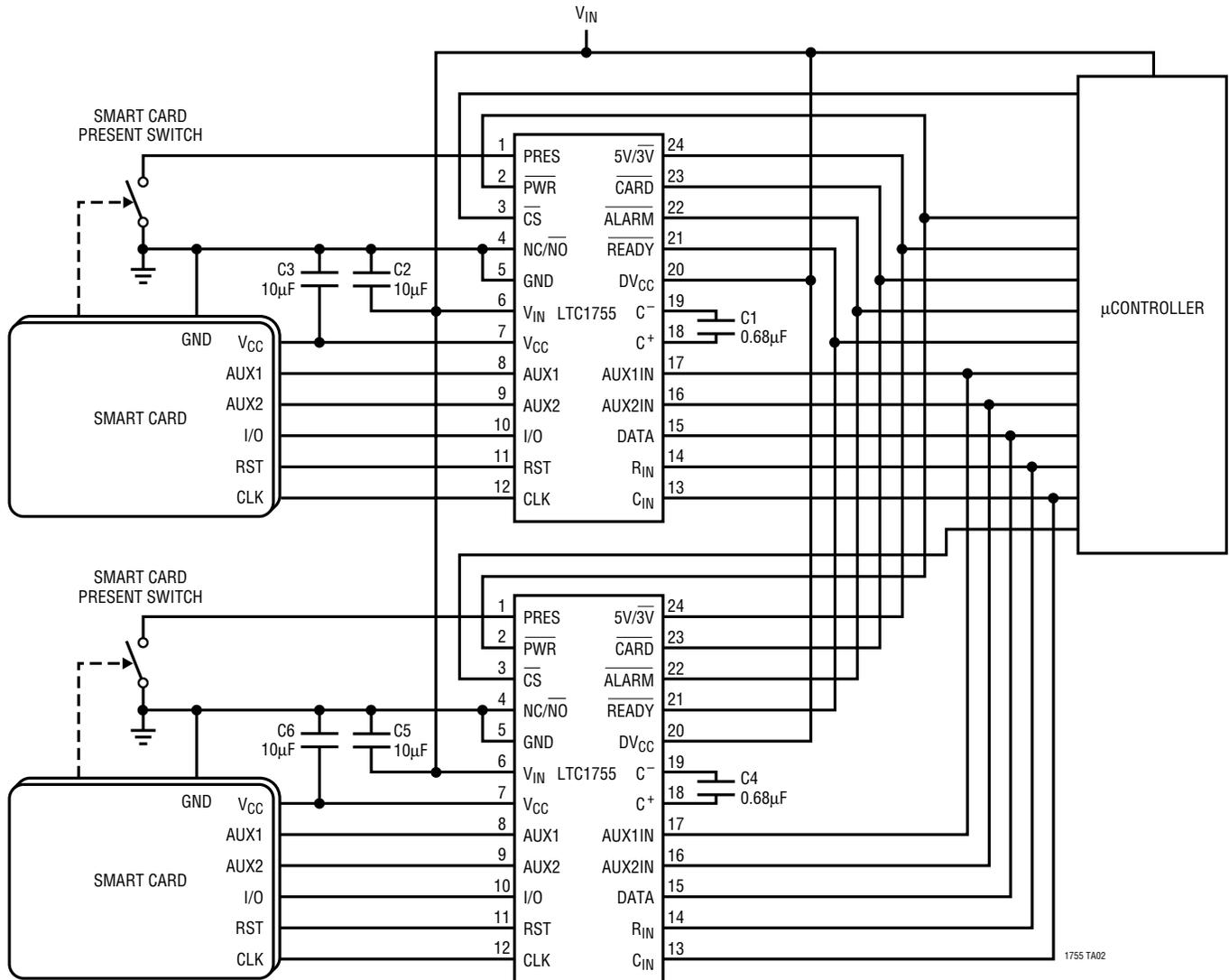


* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
 ** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN24 (SSOP) 1098

TYPICAL APPLICATION

Paralleling Devices for Multicard Applications



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1514/LTC1515	Micropower Step-Up/Step-Down Inductorless DC/DC Converters	Regulated Output Up to 50mA, V _{IN} from 2V to 10V, SO-8 Package
LTC1516	Micropower Regulated 5V Charge Pump	5V/50mA Output from 2V to 5V Input, SO-8 Package
LTC1555/LTC1556	SIM Power Supply and Level Translator	Step-Up/Step-Down Charge Pump + SIM Level Translators, >10kV ESD
LTC1754-5	5V Charge Pump with Shutdown in SOT-23	V _{IN} from 2.7V to 5.5V, 50mA Output with V _{IN} ≥ 3V
LTC1986	3V/5V SIM Power Supply in SOT-23	V _{IN} from 2.6V to 4.4V, 3V/5V Output at 10mA