

Micropower Precision Triple Supply Monitors in 8-Lead MSOP and 5-Lead SOT-23 Packages

November 1999

FEATURES

- Monitors Three Inputs Simultaneously
 LTC1727-5: 5V, 3.3V and ADJ
 LTC1727-2.5: 2.5V, 3.3V and ADJ
 LTC1728-5: 5V, 3.3V and ADJ
 LTC1728-2.5: 2.5V, 3.3V and ADJ
- $\pm 1.5\%$ Threshold Accuracy Over Temperature
- Very Low Supply Current: 10 μ A Typ
- 200ms Reset Time Delay
- Active Low RESET Output
- Power Supply Glitch Immunity
- Guaranteed $\overline{\text{RESET}}$ for $V_{CC3} \geq 1V$ or $V_{CC5}/V_{CC25} \geq 1V$
- LTC1727 Includes Monitor Output for Each Supply
- LTC1727: 8-Lead MSOP and SO Packages
- LTC1728: 5-Lead SOT-23 Package

APPLICATIONS

- Desktop Computers
- Notebook Computers
- Intelligent Instruments
- Portable Battery-Powered Equipment
- Network Servers

DESCRIPTION

The LTC[®]1727 is a triple supply monitor intended for systems with multiple supply voltages. Each supply monitor has its own open-drain output for individual supply monitoring. A common open-drain reset output remains low until all three supplies have been in compliance for 200ms. Tight 1.5% accuracy specifications and glitch immunity ensure reliable reset operation without false triggering.

The LTC1728 is functionally identical to the LTC1727 without the individual monitor outputs.

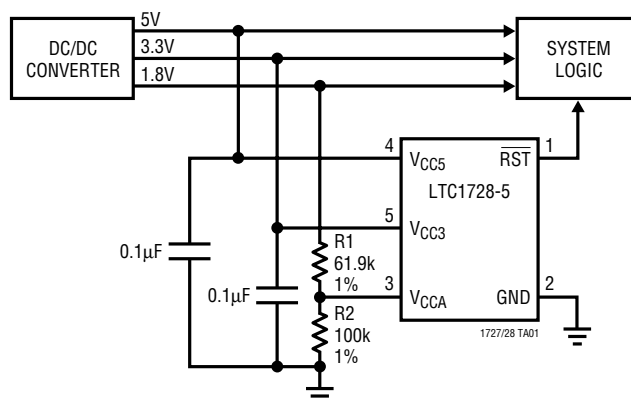
The $\overline{\text{RST}}$ output is guaranteed to be in the correct state for V_{CC5}/V_{CC25} or V_{CC3} down to 1V. The LTC1727/LTC1728 may also be configured to monitor any one or two V_{CC} inputs instead of three, depending on system requirements.

Very low (10 μ A typical) supply current makes the LTC1727/LTC1728 ideal for power conscious systems.

The LTC1727 is available in an 8-lead MSOP or SO package and the LTC1728 is available in a 5-lead SOT-23 package.

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TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

V_{CC3} , V_{CC5}/V_{CC25} , V_{CCA}	–0.5V to 7V	Operating Temperature Range	
RST	–0.5V to 7V	(Note 3)	–40°C to 85°C
COMP3, COMP25/COMP5		Storage Temperature Range	–65°C to 150°C
(MS8 and SO-8 Only)	–0.5V to 7V	Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 160^{\circ}\text{C/W}$</p>		<p>TOP VIEW</p> <p>S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 160^{\circ}\text{C/W}$</p>		<p>TOP VIEW</p> <p>S5 PACKAGE 5-LEAD PLASTIC SOT-23 $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 250^{\circ}\text{C/W}$</p>	
ORDER PART NUMBER	MS8 PART MARKING	ORDER PART NUMBER	S8 PART MARKING	ORDER PART NUMBER	S5 PART MARKING
LTC1727EMS8-2.5	LTHY	LTC1727ES8-2.5	172725	LTC1728ES5-2.5	LTIA
LTC1727EMS8-5	LTHX	LTC1727IS8-2.5	727I25	LTC1728ES5-5	LTHZ
		LTC1727ES8-5	17275		
		LTC1727IS8-5	1727I5		

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_{CC3} = 3.3\text{V}$, $V_{CC5} = 5\text{V}$, $V_{CC25} = 2.5\text{V}$, $V_{CCA} = V_{CC3}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{RT3}	Reset Threshold V_{CC3}	V_{CC3} Input Threshold	● 3.036	3.086	3.135	V
V_{RT5}	Reset Threshold V_{CC5}	V_{CC5} Input Threshold (5V Version)	● 4.600	4.675	4.750	V
V_{RT25}	Reset Threshold V_{CC25}	V_{CC25} Input Threshold (2.5V Version)	● 2.300	2.338	2.375	V
V_{RTA}	Reset Threshold V_{CCA}	V_{CCA} Input Threshold	● 0.985	1.000	1.015	V
V_{CCOP}	V_{CC3} , V_{CC5}/V_{CC25} Operating Voltage	RST, COMP3, COMP5, COMP25 in Correct Logic State	● 1		7	V
V_{CCOPA}	V_{CC3} , V_{CC5}/V_{CC25} Operating Voltage	Minimum Supply Voltage to Guarantee COMPA in Correct Logic State	●	2	2.3	V
I_{VCC3}	V_{CC3} Supply Current	$V_{CC5}/V_{CC25} > V_{CC3}$ $V_{CC5}/V_{CC25} < V_{CC3}$, $V_{CC3} = 3.3\text{V}$ (Note 4)	●	1	2	μA
			●	10	20	μA
I_{VCC25}	V_{CC25} Supply Current	$V_{CC25} < V_{CC3}$, $V_{CC25} = 2.5\text{V}$ (Note 4)	●	1	2	μA
I_{VCC5}	V_{CC5} Supply Current	$V_{CC5} = 5\text{V}$, $V_{CC3} < V_{CC5}$	●	11	20	μA
I_{VCCA}	V_{CCA} Input Current	$V_{CCA} = 1\text{V}$	● –15	0	15	nA
t_{RST}	Reset Pulse Width	RST Low with 10k Pull-Up to V_{CC3}	● 140	200	280	ms

ELECTRICAL CHARACTERISTICS The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CC3} = 3.3\text{V}$, $V_{CC5} = 5\text{V}$, $V_{CC25} = 2.5\text{V}$, $V_{CCA} = V_{CC3}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{UV}	V_{CC} Undervoltage Detect to $\overline{\text{RST}}$ or COMPX	V_{CC5} , V_{CC25} , V_{CC3} or V_{CCA} Less Than Reset Threshold V_{RT} by More Than 1%		110		μs
V_{OL}	Output Voltage Low, $\overline{\text{RST}}$, COMPX	$I_{\text{SINK}} = 2.5\text{mA}$, $V_{CC3} = 3\text{V}$, $V_{CC5}/V_{CC25} = 0\text{V}$	●	0.15	0.4	V
		$I_{\text{SINK}} = 100\mu\text{A}$, $V_{CC3} = 1\text{V}$, $V_{CC5}/V_{CC25} = 0\text{V}$	●	0.05	0.3	V
		$I_{\text{SINK}} = 100\mu\text{A}$, $V_{CC3} = 0\text{V}$, $V_{CC5}/V_{CC25} = 1\text{V}$	●	0.05	0.3	V
		$I_{\text{SINK}} = 100\mu\text{A}$, $V_{CC3} = 1\text{V}$, $V_{CC5}/V_{CC25} = 1\text{V}$	●	0.05	0.3	V
V_{OH}	Output Voltage High, $\overline{\text{RST}}$, COMPX (Note 5)	$I_{\text{SOURCE}} = 1\mu\text{A}$	●	$V_{CC3} - 1$		V

LTC1727-5/LTC1728-5 Only

V_{OVR}	V_{CC5} Reset Override Voltage (Note 6)	Override V_{CC5} Ability to Assert $\overline{\text{RST}}$		$V_{CC3} \pm 0.025$		V
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Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: The LTC1727E/LTC1728E are guaranteed to meet specified performance from 0°C to 70°C and are designed, characterized and assured to meet the extended temperature limits of -40°C to 85°C but are not tested at these temperatures.

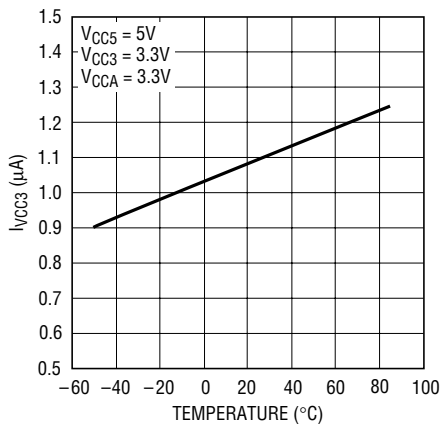
Note 4: Both V_{CC3} and V_{CC5}/V_{CC25} can act as the supply depending on which pin has the greatest potential.

Note 5: The output pins $\overline{\text{RST}}$ and COMPX have internal pull-ups to V_{CC3} of typically $6\mu\text{A}$. However, external pull-up resistors may be used when faster rise times are required or for V_{OH} voltages greater than V_{CC3} .

Note 6: The V_{CC5} reset override voltage is valid for an operating range less than approximately 4.15V . Above this point the override is turned off and the V_{CC5} pin functions normally.

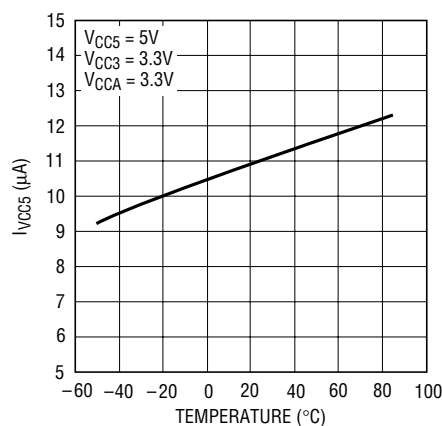
TYPICAL PERFORMANCE CHARACTERISTICS

I_{VCC3} vs Temperature
(LTC1727-5/LTC1728-5)



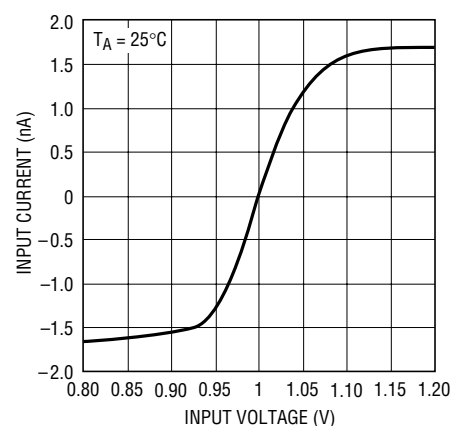
1727/28 G01

I_{VCC5} vs Temperature
(LTC1727-5/LTC1728-5)



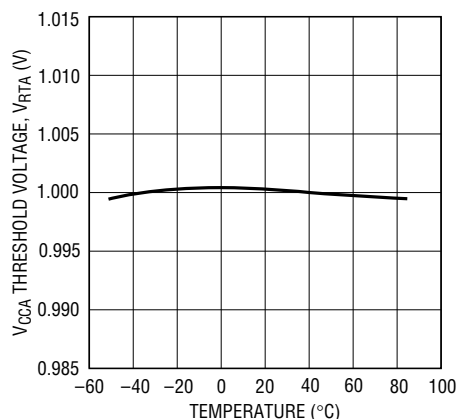
1727/28 G02

V_{CCA} Input Current
vs Input Voltage

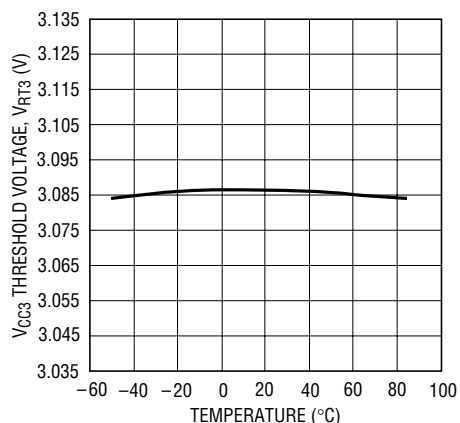


1727/28 G03

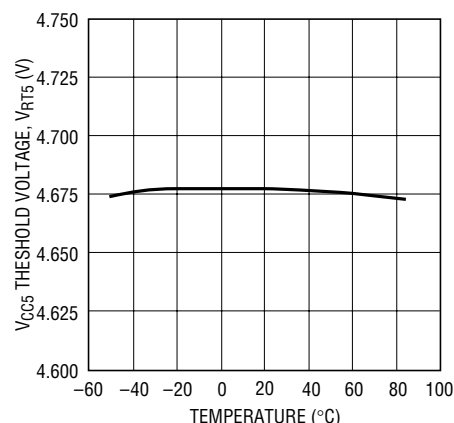
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CCA} Threshold Voltage vs Temperature

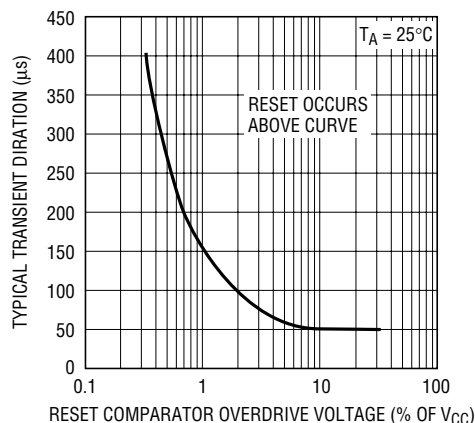
1727/28 G04

V_{CC3} Threshold Voltage vs Temperature

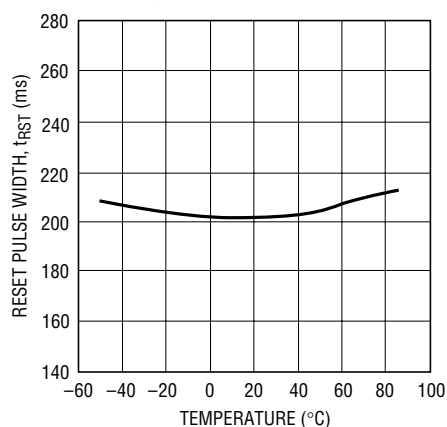
1727/28 G05

V_{CC5} Threshold Voltage vs Temperature

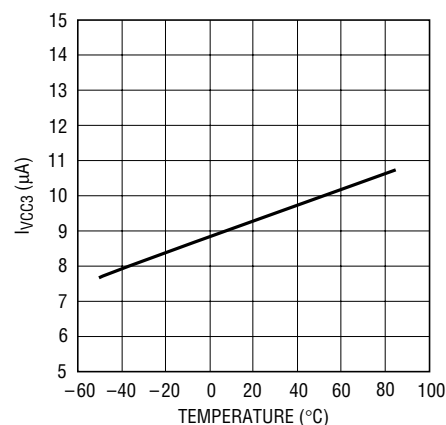
1727/28 G06

Typical Transient Duration vs Comparator Overdrive

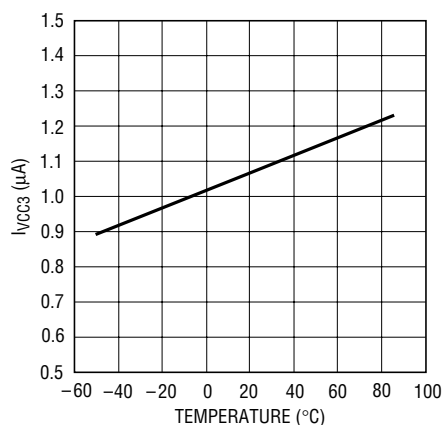
1727/28 G07

Reset Pulse Width vs Temperature

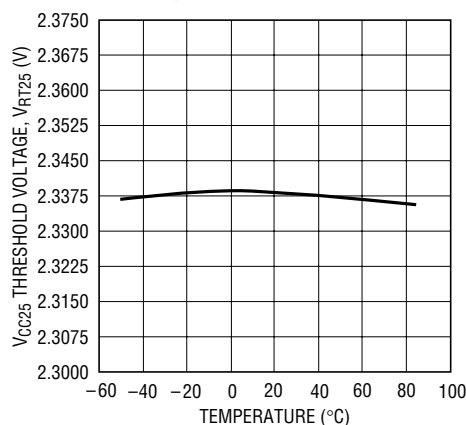
1727/28 G08

I_{VCC3} vs Temperature (LTC1727-2.5/LTC1728-2.5)

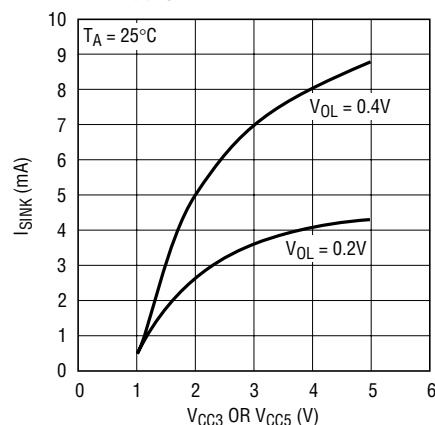
1727/28 G09

I_{VCC25} vs Temperature (LTC1727-2.5/LTC1728-2.5)

1727/28 G01

V_{CC25} Threshold Voltage vs Temperature

1727/28 G11

R_{ST}, COMPX I_{SINK} vs Supply Voltage

1727/28 G12

PIN FUNCTIONS (LTC1727/LTC1728)

V_{CC3} (Pin 1/Pin 5): 3.3V Sense Input and Power Supply Pin. This pin provides power to the part when the voltage on V_{CC3} is greater than the voltage on V_{CC5}/V_{CC25}. Bypass to ground with a $\geq 0.1\mu\text{F}$ ceramic capacitor.

V_{CC5} (Pin 2/Pin 4): 5V Sense Input and Power Supply Pin. This pin is used on the LTC1727-5/LTC1728-5 to provide power to the part when the voltage on V_{CC5} is greater than the voltage on V_{CC3}. Bypass to ground with a $\geq 0.1\mu\text{F}$ ceramic capacitor.

V_{CC25} (Pin 2/Pin 4): 2.5V Sense Input and Power Supply Pin. This pin is used on the LTC1727-2.5/LTC1728-2.5 to provide power to the part when the voltage on V_{CC25} is greater than the voltage on V_{CC3}. Bypass to ground with a $\geq 0.1\mu\text{F}$ ceramic capacitor.

V_{CCA} (Pin 3/Pin 3): 1V Sense, High Impedance Input. If unused it can be tied to either V_{CC3} or V_{CC5}/V_{CC25}.

GND (Pin 4/Pin 2): Ground.

COMPA (Pin 5): V_{CCA} Comparator Output for the LTC1727. Active high, open-drain logic output with weak pull-up to V_{CC3}. Asserted when V_{CCA} is above V_{RTA}. Deasserted when V_{CCA} is below V_{RTA} or if both the V_{CC3} and V_{CC5}

supply pins are too low to power the internal bandgap reference (typically $< 2.3\text{V}$). Can be pulled greater than V_{CC3} using an external pull-up.

RST (Pin 6/Pin 1): Reset Logic Output. Active low, open-drain logic output with weak pull-up to V_{CC3}. Can be pulled up greater than V_{CC3} when interfacing to 5V logic. Asserted when one or all of the supplies are below trip thresholds and held for 200ms after all supplies become valid.

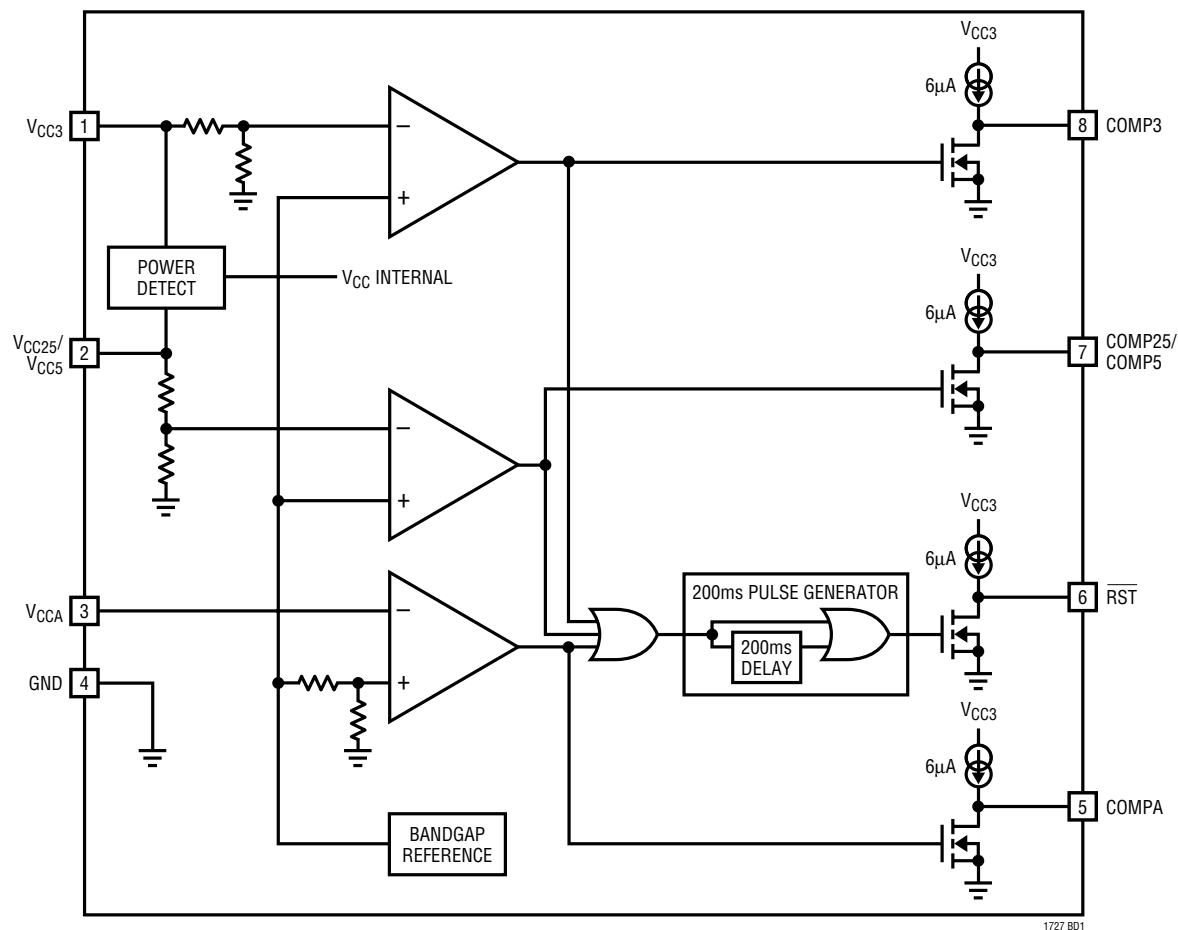
COMP5 (Pin 7): V_{CC5} Comparator Output for the LTC1727-5. Active high, open-drain logic output with weak pull-up to V_{CC3}. Asserted when V_{CC5} is above V_{RT5}. Can be pulled greater than V_{CC3} using an external pull-up.

COMP25 (Pin 7): V_{CC25} Comparator Output for the LTC1727-2.5. Active high, open-drain logic output with weak pull-up to V_{CC3}. Asserted when V_{CC25} is above V_{RT25}. Can be pulled greater than V_{CC3} using an external pull-up.

COMP3 (Pin 8): V_{CC3} Comparator Output for the LTC1727. Active high, open-drain logic output with weak pull-up to V_{CC3}. Asserted when V_{CC3} is above V_{RT3}. Can be pulled greater than V_{CC3} using an external pull-up.

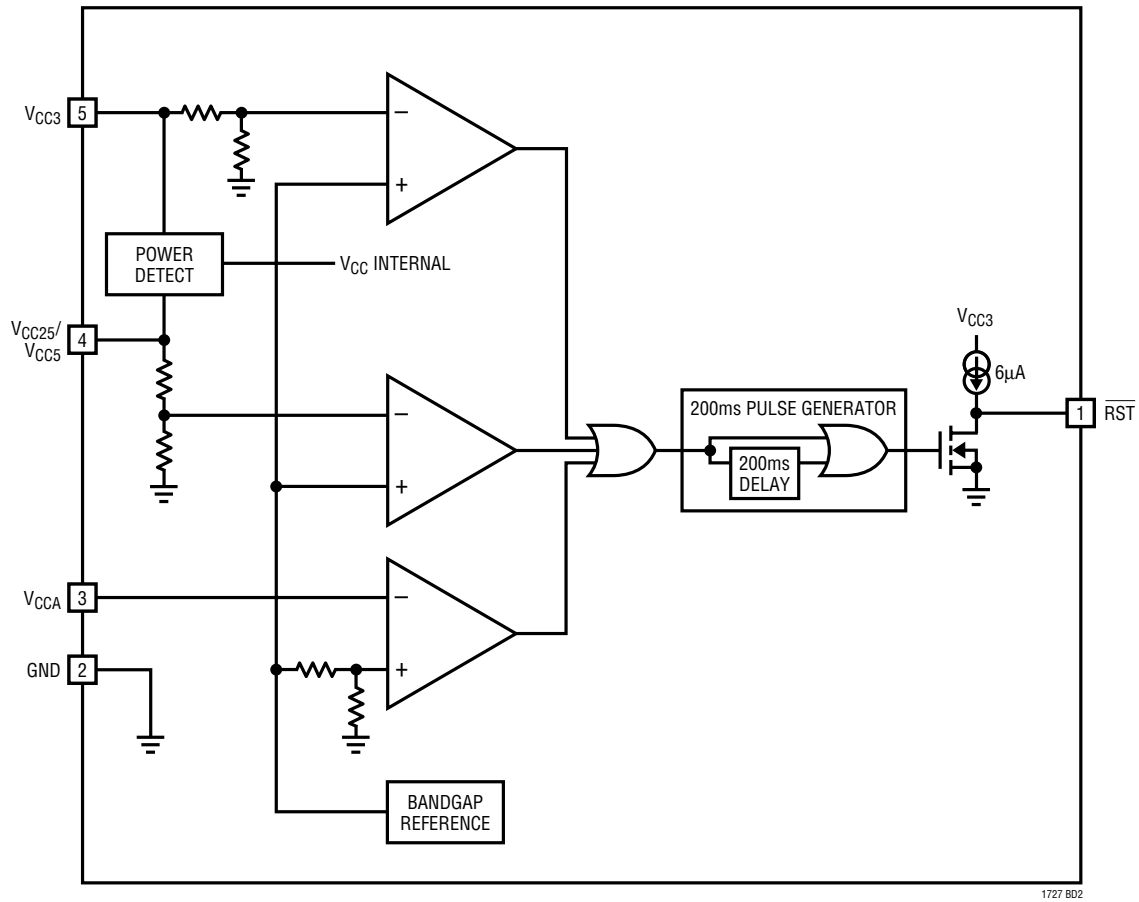
BLOCK DIAGRAMS

LTC1727-2.5/LTC1727-5



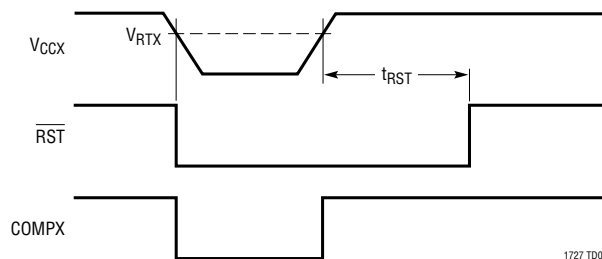
BLOCK DIAGRAMS

LTC1728-2.5/LTC1728-5



TIMING DIAGRAM

VCC Monitor Timing



APPLICATIONS INFORMATION

Supply Monitoring

The LTC1727 is a low power, high accuracy triple supply monitoring circuit with three monitor outputs and a 200ms μ processor reset output.

The LTC1728 is a low power, high accuracy triple supply monitoring circuit with a single 200ms μ processor reset output.

All three V_{CC} inputs must be above predetermined thresholds for reset not to be invoked. The LTC1727/LTC1728 will assert reset during power-up, power-down and brown-out conditions on any one or all of the V_{CC} inputs.

3V or 5V Power Detect

The LTC1727/LTC1728 are powered from the 3.3V input pin (V_{CC3}), the 2.5V input pin (V_{CC25}) or the 5V input pin (V_{CC5}), whichever pin has the highest potential. This ensures the part pulls the \overline{RST} pin low as soon as either input pin is $\geq 1V$.

Power-Up

Upon power-up, either the V_{CC5}/V_{CC25} or V_{CC3} pin, can power the part. This ensures that \overline{RST} will be low when either V_{CC5}/V_{CC25} or V_{CC3} reaches 1V. As long as any one of the V_{CC} inputs is below its predetermined threshold, \overline{RST} will stay a logic low. Once all of the V_{CC} inputs rise above their thresholds, an internal timer is started and \overline{RST} is released after 200ms.

\overline{RST} is reasserted whenever any one of the V_{CC} inputs drops below its predetermined threshold and remains asserted until 200ms after all of the V_{CC} inputs are above their thresholds.

On the LTC1727, each of the comparator outputs will be low until the V_{CC} input that is monitored by that comparator rises above the appropriate predetermined threshold. The COMP3, and COMP5/COMP25 outputs are guaranteed to be in the correct logic state for either V_{CC3} or V_{CC5}/V_{CC25} greater than 1V. The COMP4 output requires the internal bandgap reference to be valid before the correct logic state can be output. Therefore, the COMP4 output will be held low until V_{CCA} is above 1V and V_{CC3} or V_{CC5}/V_{CC25} is greater than 2V (typ).

Power-Down

On power-down, once any of the V_{CC} inputs drop below its threshold, \overline{RST} is held at a logic low. A logic low of 0.3V is guaranteed until both V_{CC3} and V_{CC5}/V_{CC25} drop below 1V.

Glitch Immunity

The \overline{RST} output of the LTC1727/LTC1728 have two forms of glitch immunity built in. First, the input monitors require the input voltage to transition at least 10% of the input threshold ($0.1 \cdot V_{RTH}$) below the input threshold for approximately 50 μ s in order to force the monitor output low. The duration of the transition must be longer for voltage transitions of lesser magnitude (see Figure 1). Secondly, the reset pulse width of approximately 200ms acts to debounce the \overline{RST} output ensuring that the \overline{RST} output will always be in the correct state.

The individual monitor outputs of the LTC1727 do not have hysteresis and will track the monitor inputs relative to the monitor's input threshold (V_{RTA} , V_{RT25} , V_{RT3} and V_{RT5}). A very slow moving input voltage with ripple riding on it may cause the individual monitor outputs (COMP4, COMP25, COMP3 and COMP5) to toggle on the ripple as the input voltage passes the input threshold. The slow response time of the LTC1727's input monitors has a tendency to integrate signals on the inputs improving their immunity to noise and ripple.

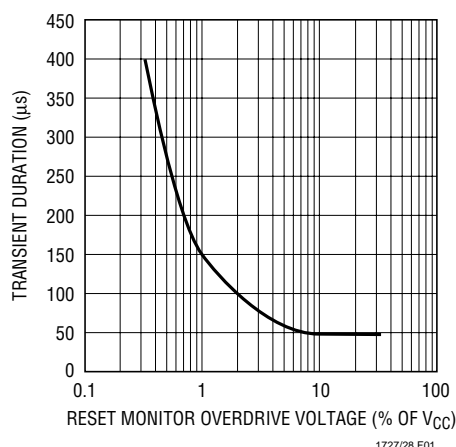


Figure 1. Transient Duration vs Comparator Overdrive

APPLICATIONS INFORMATION

Override Functions (5V Versions Only)

The V_{CCA} pin, if unused, can be tied to either V_{CC3} or V_{CC5} . This is an obvious solution since the trip points for V_{CC3} and V_{CC5} will always be greater than the trip point for V_{CCA} .

The V_{CC5} input trip point is disabled if its voltage is equal to the voltage on $V_{CC3} \pm 25\text{mV}$ and the voltage on V_{CC5} is less than 4.15V. In this manner the LTC1727-5/ LTC1728-5 will behave as a 3.3V monitor and V_{CC5} reset capability will be disabled.

The V_{CC5} trip point is reenabled when the voltage on V_{CC5} is equal to the voltage on $V_{CC3} \pm 25\text{mV}$ and the two inputs are greater than approximately 4.15V. In this manner the part can function as a 5V monitor with the 3.3V monitor disabled.

When monitoring either 3.3V or 5V with V_{CC3} strapped to V_{CC5} , (see Figure 2) the part determines which is the appropriate range. The part handles this situation as shown in Figure 3. Above 1V and below V_{RT3} , $\overline{\text{RST}}$ is held low. From V_{RT3} to approximately 4.15V the part assumes 3.3V supply monitoring and $\overline{\text{RST}}$ is deasserted. Above approximately 4.15V the part operates as a 5V monitor. In most systems the 5V supply will pass through the 3.1V to 4.15V region in <200ms during power-up, and the $\overline{\text{RST}}$ output will behave as desired. Table 1 summarizes the state of $\overline{\text{RST}}$ at various operating voltages with $V_{CC3} = V_{CC5}$.

Table 1. Override Truth Table ($V_{CC3} = V_{CC5}$)

INPUTS ($V_{CC3} = V_{CC5} = V_{CC}$)	$\overline{\text{RST}}$
$0\text{V} \leq V_{CC} \leq 1\text{V}$	—
$1\text{V} \leq V_{CC} \leq V_{RT3}$	0
$V_{RT3} \leq V_{CC} \leq 4.15\text{V}$	1
$4.15\text{V} \leq V_{CC} \leq V_{RT5}$	0
$V_{RT5} \leq V_{CC}$	1

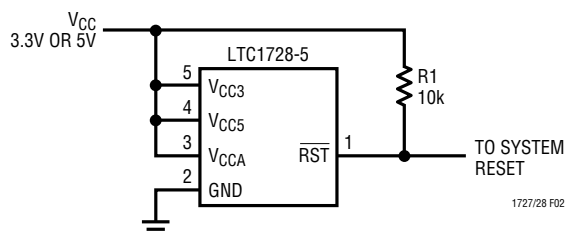


Figure 2. Single Supply Monitor with Others Disabled

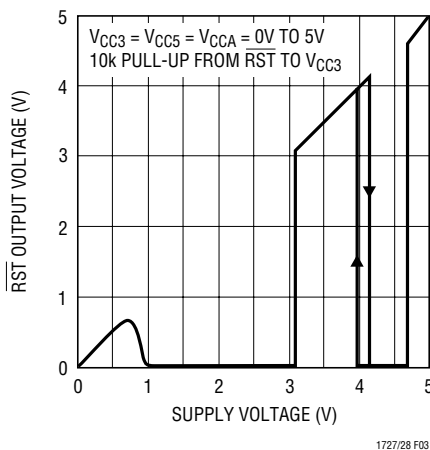


Figure 3. $\overline{\text{RST}}$ Voltage vs Supply Voltage

APPLICATIONS INFORMATION

Figure 4 contains a simple circuit for 5V systems that can't risk the $\overline{\text{RST}}$ output going high in the 3.1V to 4.15V range (possibly due to very slow rise time on the 5V supply). Diode D1 powers the LTC1728-5 while dropping $\approx 0.6\text{V}$ from the V_{CC5} pin to the V_{CC3} pin. This prevents the part's internal override circuit from being activated. Without the override circuit active, the $\overline{\text{RST}}$ pin stays low until V_{CC5} reaches $\text{V}_{\text{RT5}} \approx 4.675\text{V}$. (See Figure 5.)

LTC1727-2.5/LTC1728-2.5 Override Functions

The V_{CCA} pin, if unused, can be tied to either V_{CC3} or V_{CC25} . This is an obvious solution since the trip points for V_{CC3} and V_{CC25} will always be greater than the trip point for V_{CCA} . Likewise, the V_{CC25} , if unused, can be tied to V_{CC3} . V_{CC3} must always be used. Tying V_{CC3} to V_{CC25} and operating off of a 2.5V supply will result in the continuous assertion of $\overline{\text{RST}}$.

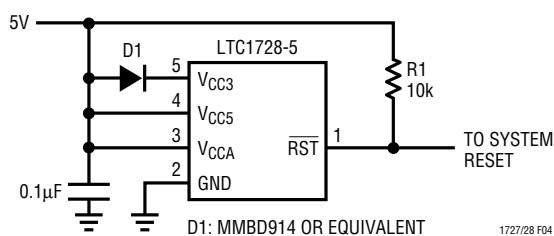


Figure 4. LTC1728-5 Monitoring a Single 5V Supply. D1 Used to Avoid $\overline{\text{RST}}$ High Near 3.1V to 4V (See Figure 3).

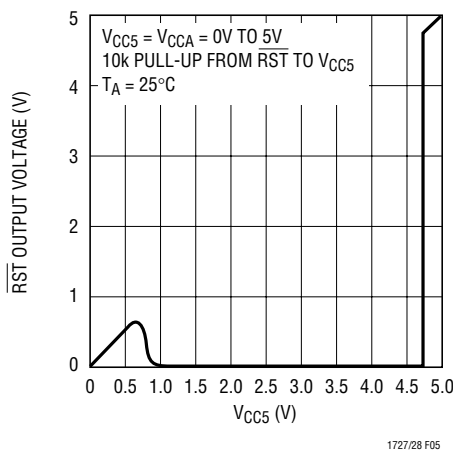
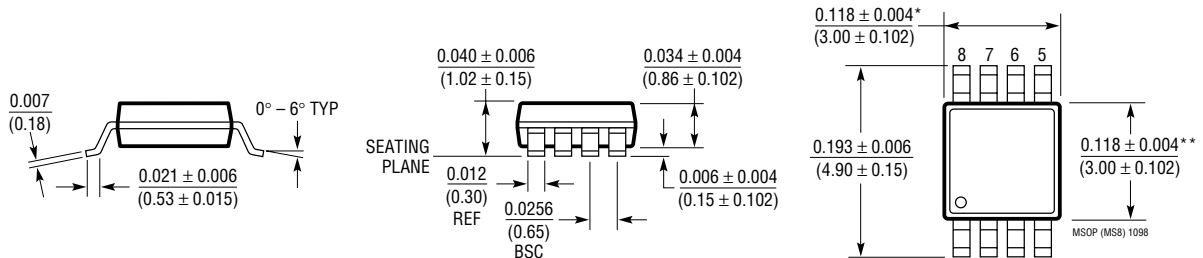


Figure 5. $\overline{\text{RST}}$ Output Voltage Characteristics of the Circuit in Figure 4

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

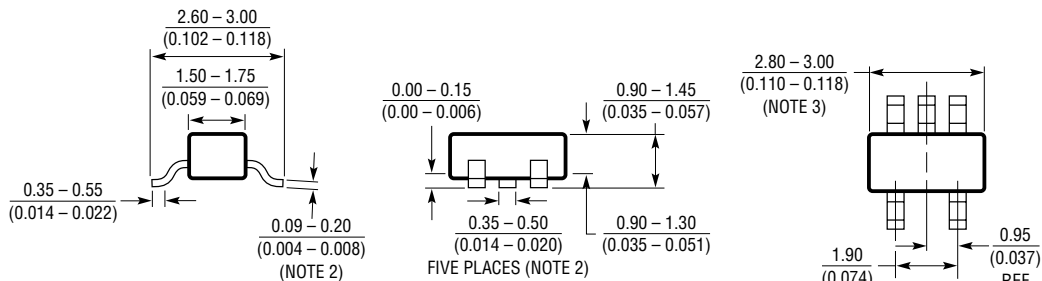
MS8 Package
8-Lead Plastic MSOP
 (LTC DWG # 05-08-1660)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006^* (0.152mm) PER SIDE

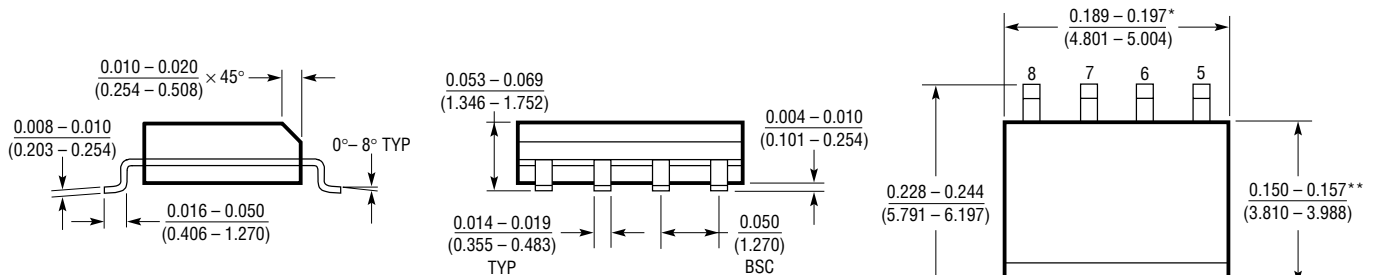
** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006^* (0.152mm) PER SIDE

S5 Package
5-Lead Plastic SOT-23
 (LTC DWG # 05-08-1633)

**NOTE:**

1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
4. MOLD FLASH SHALL NOT EXCEED 0.254mm
5. PACKAGE EIAJ REFERENCE IS SC-74A (EIAJ)

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
 (LTC DWG # 05-08-1610)

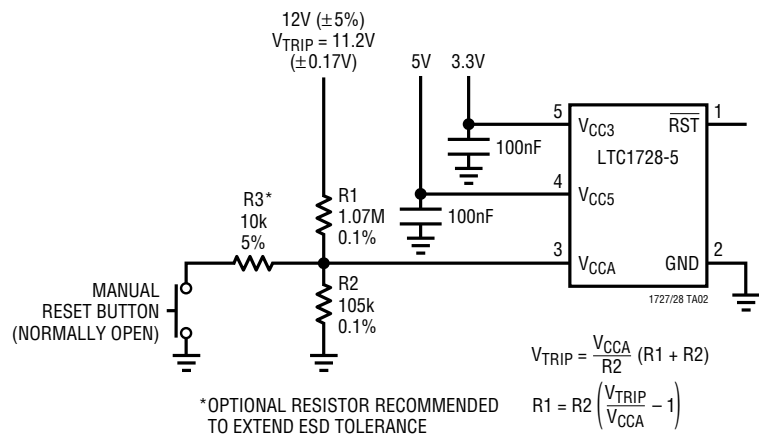


* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006^* (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010^* (0.254mm) PER SIDE

TYPICAL APPLICATION

Triple Supply Monitor with Manual Reset Button



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC690	5V Supply Monitor, Watchdog Timer and Battery Backup	4.65V Threshold
LTC694-3.3	3.3V Supply Monitor, Watchdog Timer and Battery Backup	2.9V Threshold
LTC699	5V Supply Monitor and Watchdog Timer	4.65V Threshold
LTC1232	5V Supply Monitor, Watchdog Timer and Push-Button Reset	4.37V/4.62V Threshold
LTC1326	Micropower Precision Triple Supply Monitor for 5V, 3.3V and ADJ	4.725V, 3.118V, 1V Thresholds (±0.75%)
LTC1326-2.5	Micropower Precision Triple Supply Monitor for 2.5V, 3.3V and ADJ	2.363V, 3.118V, 1V Thresholds (±0.75%)
LTC1536	Precision Triple Supply Monitor for PCI Applications	Meets PCI t_{FAIL} Timing Specifications