LTC1484

Low Power EIA485 Transceiver with Receiver Fail-Safe

September 1998

FEATURES

- **No Damage or Latchup to ±15kV ESD (Human Body Model), IEC-1000-4-2 Level 4 Contact (±8kV) and Level 3 (±8kV) Air Gap Specifications**
- **Guaranteed High Receiver Output State for Floating, Shorted or Terminated Inputs with No Signal Present**
- **Drives Low Cost Residential Telephone Wires**
- Low Power: I_{CC} = 700µA Max with Driver Disabled
- I_{CC} = 900µA Max for Driver Enable with No Load
- 20µA Max Quiescent Current in Shutdown Mode
- Single 5V Supply
- –7V to 12V Common Mode Range Permits ±7V Ground Difference Between Devices on the Data Line
- Power Up/Down Glitch-Free Driver Outputs
- Up to 32 Transceivers on the Bus
- Pin Compatible with the LTC485
- Available in 8-Lead **MSOP**, PDIP and SO Packages

APPLICATIONS

- Battery-Powered EIA485/EIA422 Applications
- Low Power EIA485/EIA422 Transceiver
- Level Translator

DESCRIPTION

The LTC®1484 is a low power EIA485 compatible transceiver. In receiver mode, it offers a fail-safe feature which guarantees a high receiver output state when the inputs are left open, shorted together or terminated with no signal present. No external components are required to ensure the high receiver output state.

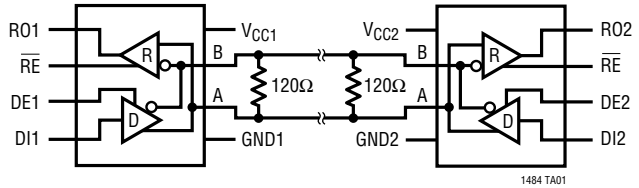
Both driver and receiver feature three-state outputs with separate receiver and driver control pins. The driver outputs maintain high impedance over the entire common mode range when three-stated. Excessive power dissipation caused by bus contention or faults is prevented by a thermal shutdown circuit that forces the driver outputs into a high impedance state.

Enhanced ESD protection allows the LTC1484 to withstand ±15kV (human body model), IEC-1000-4-2 level 4 (±8kV) contact and level 3 (±8kV) air discharge ESD without latchup or damage.

The LTC1484 is fully specified over the commercial and industrial temperature ranges and is available in 8-lead MSOP, PDIP and SO packages.

TYPICAL APPLICATION

EIA485 Interface

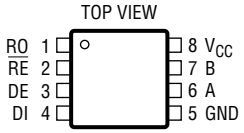


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 6.5V
Control Input Voltages ..... −0.3V to (V_{CC} + 0.3V)
Driver Input Voltage ..... −0.3V to (V_{CC} + 0.3V)
Driver Output Voltages ..... −7V to 10V
Receiver Input Voltages (Driver Disabled) .. −12V to 14V
Receiver Output Voltage ..... −0.3V to (V_{CC} + 0.3V)
Junction Temperature ..... 125°C
Operating Temperature Range
LTC1484C ..... 0°C ≤ T_A ≤ 70°C
LTC1484I ..... −40°C ≤ T_A ≤ 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

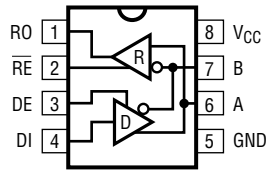
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 200°C/W

ORDER PART NUMBER
LTC1484CMS8
MS8 PART MARKING
LTDX



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 125°C, θ_{JA} = 135°C/W (S8)

ORDER PART NUMBER
LTC1484CN8 LTC1484CS8 LTC1484IN8 LTC1484IS8
S8 PART MARKING
1484 1484I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±5% (Notes 2 and 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	I_{OUT} = 0	●			V_{CC}	V
V_{OD2}	Differential Driver Output Voltage (with Load)	R = 50Ω (RS422) R = 27Ω (RS485) Figure 1 R = 22Ω, Figure 1	● ●	2 1.5		 5	V V V
V_{OD3}	Differential Driver Output Voltage (with Common Mode)	V_{TST} = −7V to 12V, Figure 2	●	1.5		5	V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 22Ω, 27Ω or R = 50Ω, Figure 1 V_{TST} = −7V to 12V, Figure 2	●			0.2	V
V_{OC}	Driver Common Mode Output Voltage	R = 22Ω, 27Ω or R = 50Ω, Figure 1	●			3	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Driver Common Mode Output Voltage for Complementary Output States	R = 22Ω, 27Ω or R = 50Ω, Figure 1	●			0.2	V
V_{IH}	Input High Voltage	DE, DI, $\overline{RE}$	●	2.0			V
V_{IL}	Input Low Voltage	DE, DI, $\overline{RE}$	●			0.8	V
I_{IN1}	Input Current	DE, DI, $\overline{RE}$	●			±2	µA
I_{IN2}	Input Current (A, B)	DE = 0, V_{CC} = 0 or 5V, V_{IN} = 12V DE = 0, V_{CC} = 0 or 5V, V_{IN} = −7V	● ●			1.0 −0.8	mA mA
V_{TH}	Differential Input Threshold Voltage for Receiver	−7V ≤ V_{CM} ≤ 12V, DE = 0	●	−0.20		−0.015	V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±5% (Notes 2 and 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔV_{TH}	Receiver Input Hysteresis	V_{CM} = 0V, DE = 0	●		±30		mV
V_{OH}	Receiver Output High Voltage	I_{OUT} = –4mA, (V_A – V_B) = 200mV	●	3.5			V
V_{OL}	Receiver Output Low Voltage	I_{OUT} = 4mA, (V_A – V_B) = –200mV	●			0.4	V
I_{OZR}	Three-State (High Impedance) Output Current at Receiver	V_{CC} = Max, 0.4V ≤ V_{OUT} ≤ 2.4V, DE = 0	●			±1	µA
R_{IN}	Receiver Input Resistance	–7V ≤ V_{CM} ≤ 12V	●	12	22		kΩ
I_{CC}	Supply Current	No Load, Output Enabled (DE = V_{CC}) No Load, Output Disabled (DE = 0)	● ●		600 400	900 700	µA µA
I_{SHDN}	Supply Current in Shutdown Mode	DE = 0, $\overline{RE}$ = V_{CC}, DI = 0	●		10	20	µA
I_{OSD1}	Driver Short-Circuit Current, V_{OUT} = High (Note 4)	–7V ≤ V_{OUT} ≤ 10V		35		250	mA
I_{OSD2}	Driver Short-Circuit Current, V_{OUT} = Low (Note 4)	–7V ≤ V_{OUT} ≤ 10V		35		250	mA
I_{OSR}	Receiver Short-Circuit Current	0V ≤ V_{OUT} ≤ V_{CC}	●	7		85	mA

SWITCHING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Driver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF (Figures 4, 6)	●	10	25	60	ns
t_{PHL}	Driver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF (Figures 4, 6)	●	10	25	60	ns
t_{SKEW}	Driver Output to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF (Figures 4, 6)	●		5	10	ns
t_r, t_f	Driver Rise or Fall Time	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF (Figures 4, 6)	●	3	15	40	ns
t_{ZH}	Driver Enable to Output High	C_L = 100pF (Figures 5, 7) S2 Closed	●		40	70	ns
t_{ZL}	Driver Enable to Output Low	C_L = 100pF (Figures 5, 7) S1 Closed	●		40	100	ns
t_{LZ}	Driver Disable Time from Low	C_L = 15pF (Figures 5, 7) S1 Closed	●		40	70	ns
t_{HZ}	Driver Disable Time from High	C_L = 15pF (Figures 5, 7) S2 Closed	●		40	70	ns
t_{PLH}	Receiver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figures 4, 8)	●	30	140	200	ns
t_{PHL}	Receiver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figures 4, 8)	●	30	140	200	ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figures 4, 8)			5		ns
t_{ZL}	Receiver Enable to Output Low	C_{RL} = 15pF (Figures 3, 9) S1 Closed	●		20	50	ns
t_{ZH}	Receiver Enable to Output High	C_{RL} = 15pF (Figures 3, 9) S2 Closed	●		20	50	ns
t_{LZ}	Receiver Disable from Low	C_{RL} = 15pF (Figures 3, 9) S1 Closed	●		20	50	ns
t_{HZ}	Receiver Disable from High	C_{RL} = 15pF (Figures 3, 9) S2 Closed	●		20	50	ns
t_{DZR}	Driver Enable to Receiver Valid	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF (Figures 4, 10)	●		1600	3000	ns
f_{MAX}	Maximum Data Rate (Note 5)		●	4	5		Mbps
t_{SHDN}	Time to Shutdown (Note 6)	DE = 0, $\overline{RE}$↑	●	50	300	600	ns

SWITCHING CHARACTERISTICS

V_{CC} = 5V ±5% (Notes 2 and 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{ZH(SHDN)}$	Driver Enable from Shutdown to Output High	C_L = 100pF (Figures 5, 7) S2 Closed, DI = DE	●		40	100	ns
$t_{ZL(SHDN)}$	Driver Enable from Shutdown to Output Low	C_L = 100pF (Figures 5, 7) S1 Closed, DI = 0	●		40	100	ns
$t_{ZH(SHDN)}$	Receiver Enable from Shutdown to Output High	C_L = 15pF (Figures 3, 9) S2 Closed, DE = 0	●			10	µs
$t_{ZL(SHDN)}$	Receiver Enable from Shutdown to Output Low	C_L = 15pF (Figures 3, 9) S1 Closed, DE = 0	●			10	µs

The ● denotes specifications which apply over the full specified temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 4: For higher ambient temperatures, the part may enter thermal shutdown during short-circuit conditions.

Note 5: Guaranteed by design.

Note 6: Time for I_{CC} to drop to $I_{CC}/2$ when the receiver is disabled.

PIN FUNCTIONS

RO (Pin 1): Receiver Output. If the receiver output is enabled ($\overline{RE}$ low) and the part is not in shutdown, RO is high if (A – B) > $V_{TH(MAX)}$ and low if (A – B) < $V_{TH(MIN)}$. RO is also high if the receiver inputs are open or shorted together, with or without a termination resistor.

$\overline{RE}$ (Pin 2): Receiver Output Enabled. A high on this pin three-states the receiver output (RO) and a low enables it.

DE (Pin 3): Driver Enable Input. DE = high enables the output of the driver with the driver outputs determined by the DI pin. DE = low forces the driver outputs into a high impedance state. The LTC1484 enters shutdown when both receiver and driver outputs are disabled ($\overline{RE}$ is high and DE is low).

DI (Pin 4): Driver Input. When the driver outputs are enabled (DE high), DI high takes the A output high and the B output low. DI low takes the A output low and the B output high.

GND (Pin 5): Ground.

A (Pin 6): Driver Output/Receiver Input. The input resistance is typically 22k when the driver is disabled (DE = 0). When the driver is enabled, the A output follows the logic level at the DI pin.

B (Pin 7): Driver Output/Receiver Input. The input resistance is typically 22k when the driver is disabled (DE = 0). When the driver is enabled, the B output is inverted from the logic level at the DI pin.

V_{CC} (Pin 8): Positive Supply. 4.75V ≤ V_{CC} ≤ 5.25V. A 0.1µF bypass capacitor is recommended.

FUNCTION TABLES

Driver

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	Z	Z
1	0	X	Z*	Z*

Note: Z = high impedance, X = don't care

*Shutdown mode for LTC1484

Receiver

INPUTS			OUTPUTS
$\overline{RE}$	DE	A – B	RO
0	0	$\geq V_{TH(MAX)}$	1
0	0	$\leq V_{TH(MIN)}$	0
0	0	Inputs Open	1
0	0	Inputs Shorted	1
1	X	X	Z†

†Shutdown mode for LTC1484 if DE = 0. Table valid with or without termination resistors.

TEST CIRCUITS

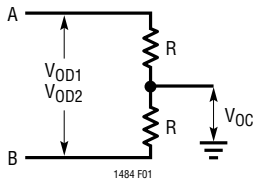


Figure 1

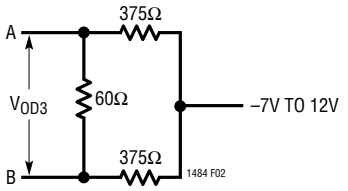


Figure 2

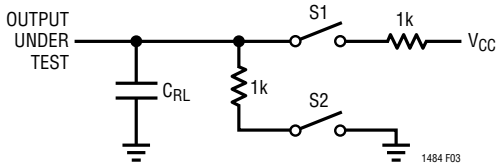


Figure 3

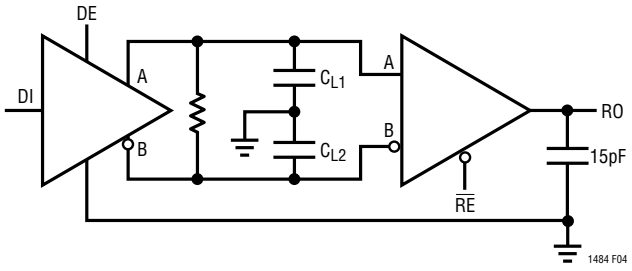


Figure 4

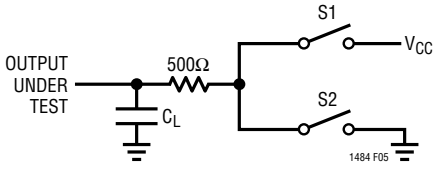
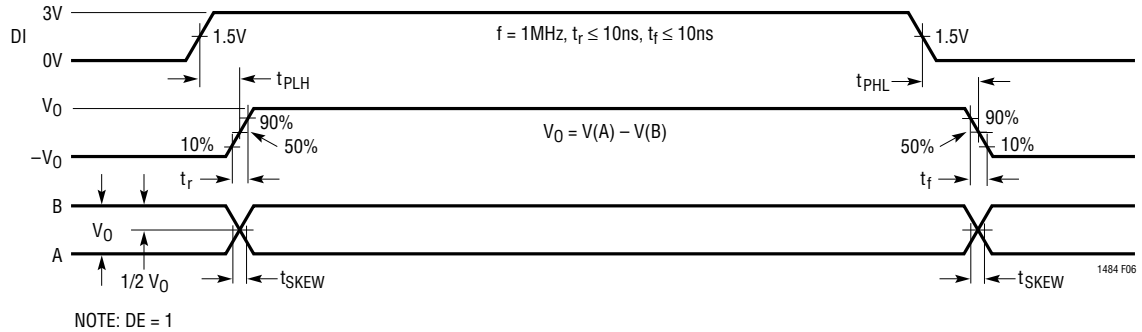


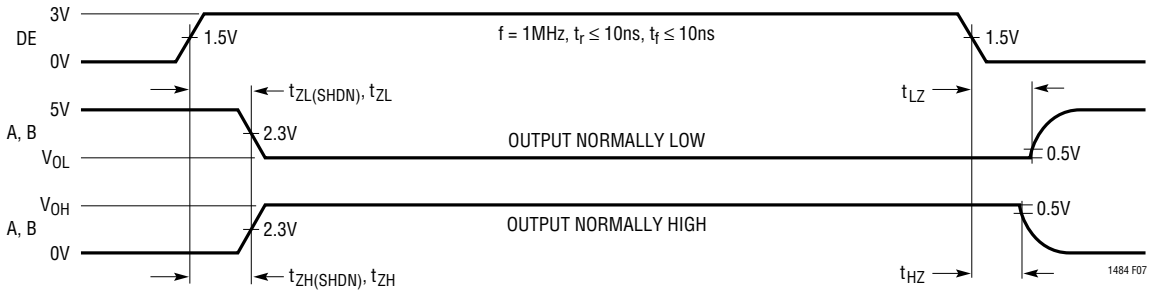
Figure 5

SWITCHING TIME WAVEFORMS



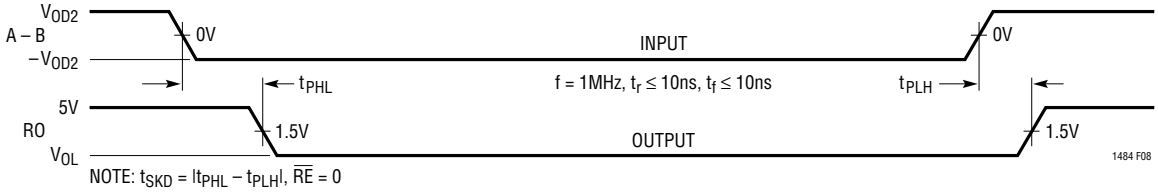
NOTE: DE = 1

Figure 6. Driver Propagation Delays



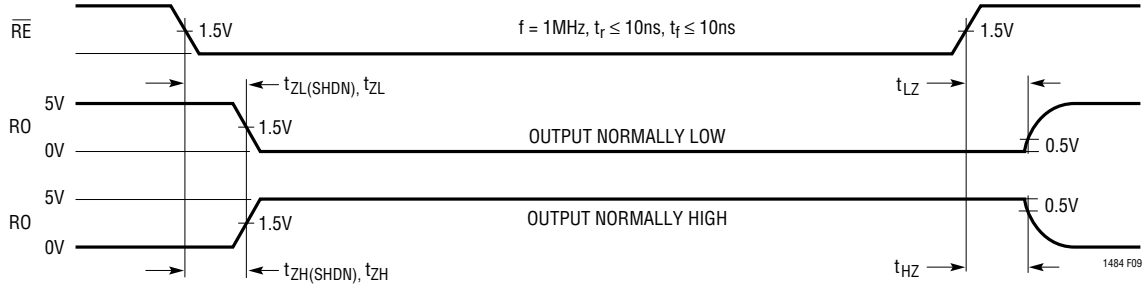
NOTE: A, B ARE THREE-STATED WHEN DE = 0, 1kΩ PULL-UP OR 1kΩ PULL-DOWN

Figure 7. Driver Enable and Disable Timing



NOTE: $t_{SKD} = |t_{PHL} - t_{PLH}|$, $\overline{RE} = 0$

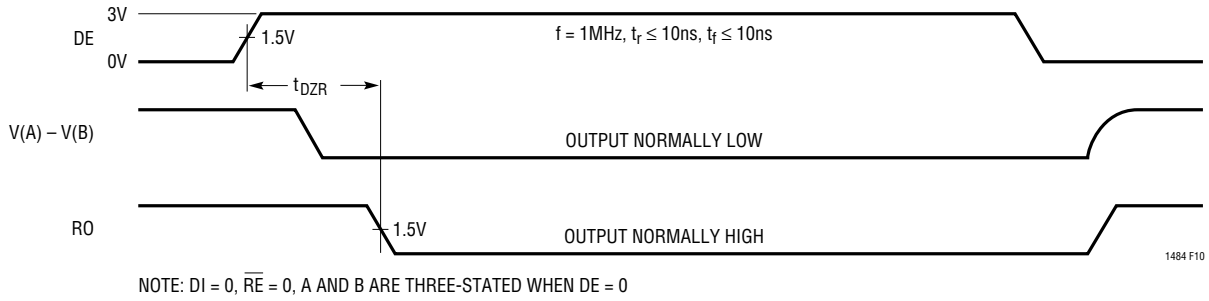
Figure 8. Receiver Propagation Delays



NOTE: DE = 0, RO IS THREE-STATED IN SHUTDOWN, 1kΩ PULL-UP FOR NORMALLY LOW OUTPUT, 1kΩ PULL-DOWN FOR NORMALLY HIGH OUTPUT

Figure 9. Receiver Enable and Shutdown Timing

SWITCHING TIME WAVEFORMS



NOTE: DI = 0, $\overline{RE}$ = 0, A AND B ARE THREE-STATED WHEN DE = 0

Figure 10. Driver Enable to Receiver Valid Timing

APPLICATIONS INFORMATION

Low Power Operation

The LTC1484 has a quiescent current of 900µA max when the driver is enabled. With the driver in three-state, the supply current drops to 700µA max. The difference in these supply currents is due to the additional current drawn by the internal 22k receiver input resistors when the driver is enabled. Under normal operating conditions, the additional current is overshadowed by the 50mA current drawn by the external termination resistor.

Receiver Open-Circuit Fail-Safe

Some encoding schemes require that the output of the receiver maintain a known state (usually a logic 1) when data transmission ends and all drivers on the line are forced into three-state. Earlier EIA485 receivers with a weak pull-up at the A input will give a high output only when the inputs are floated. When terminated or shorted together, the weak pull-up is easily defeated causing the receiver output to go low. External components are needed if a high receiver output is mandatory. The receiver of the LTC1484 has a fail-safe feature which guarantees the output to be in a logic 1 when the receiver inputs are left open or shorted together, regardless of whether the termination resistor is present or not.

In encoding schemes where the required known state is a low, external components are needed for the LTC1484 and other EIA485 parts.

Fail-safe is achieved by making the receiver trip points fall within the $V_{TH(MIN)}$ to $V_{TH(MAX)}$ range. When any of the listed receiver input conditions exist, the receiver inputs are effectively at 0V and the receiver output goes high.

The receiver fail-safe mechanism is designed to reject fast common mode steps (–7V to 12V in 10ns) switching at 100kHz typ. This is achieved through an internal carrier detect circuit similar to the LTC1482. This circuit has built-in delays to prevent glitches while the input swings between $\pm V_{TH(MAX)}$ levels. When all the drivers connected to the receiver inputs are three-stated, the internal carrier detect signal goes low to indicate that no differential signal is present. When any driver is taken out of three-state, the carrier detect signal takes 1.6µs typ (see t_{DZR}) to detect the enabled driver. During this interval, the transceiver output (RO) is forced to the fail-safe high state. After 1.6µs, the receiver will respond normally to changes in driver output.

If the part is taken out of shutdown mode with the receiver inputs floating, the receiver output takes about 10µs to leave three-state. If the receiver inputs are actively driven to a high state, the outputs go high after about 5.5µs (see $t_{ZL(SHDN)}$).

APPLICATIONS INFORMATION

Shutdown Mode

The receiver output (RO) and the driver outputs (A, B) can be three-stated by taking the $\overline{RE}$ and DE pins high and low respectively. Taking $\overline{RE}$ high and DE low at the same time puts the LTC1484 into shutdown mode and I_{CC} drops to 20μA max.

In some applications (see CDMA), the A and B lines are pulled to V_{CC} or GND through external resistors to force the line to a high or low state when all connected drivers are disabled. In shutdown, the supply current will be higher than 20μA due to the additional current drawn through the external pull-up and the 22k input resistance of the LTC1484.

ESD Protection

The ESD performance of the LTC1484 A and B pins is characterized to meet ±15kV using the Human Body Model (100pF, 1.5kΩ), IEC-1000-4-2 level (±8kV) contact mode and IEC-1000-4-2 level 3 (±8kV) air discharge mode.

This means that external voltage suppressors are not required in many applications when compared with parts that are only protected to ±2kV. Pins other than the A and B pins are protected to ±4.5kV typical per the Human Body Model.

When powered up, the LTC1484 does not latch up or sustain damage when the A and B pins are tested using any of the three conditions listed. The data during the ESD event may be corrupted, but after the event the LTC1484 continues to operate normally. The additional ESD protection at the A and B pins is important in applications where these pins are exposed to the external world via connections to sockets.

Fault Protection

When shorted to –7V or 10V at room temperature, the short-circuit current in the driver pins is limited by internal resistance or protection circuitry to 250mA. Over the industrial temperature range, the absolute maximum positive voltage at any driver pin should be limited to 10V to avoid damage to the driver pins. At higher ambient temperatures, the rise in die temperature due to the short-circuit current may trip the thermal shutdown circuit.

When the driver is disabled, the receiver inputs can withstand the entire –7V to 12V EIA485 common mode range without damage.

The LTC1484 includes a thermal shutdown circuit which protects the part against prolonged shorts at the driver outputs. If a driver output is shorted to another output or to V_{CC}, the current will be limited to 250mA. If the die temperature rises above 150°C, the thermal shutdown circuit three-states the driver outputs to open the current path. When the die cools down to about 130°C, the driver outputs are taken out of three-state. If the short persists, the part will heat again and the cycle will repeat. This thermal oscillation occurs at about 10Hz and protects the part from excessive power dissipation. The average fault current drops as the driver cycles between active and three-state. When the short is removed, the part will return to normal operation.

Carrier Detect Multiple Access (CDMA) Application

In normal half-duplex EIA485 systems, only one node can transmit at a time. If an idle node suddenly needs to gain access to the twisted pair whilst other communications are in progress, it must wait its turn. This delay is unacceptable in safety-related applications. A scheme known as Carrier Detect Multiple Access (CDMA) solves this problem by allowing any node to interrupt on-going communications.

Figure 11 shows four nodes in a typical CDMA communications system. In the absence of any active drivers, bias resistors (1.2k) force a “1” across the twisted pair. All drivers in the system are connected so that when enabled, they transmit a “0”. This is accomplished by tying DI low and using DE as the driver data input. A “1” is transmitted by disabling the driver’s “0” output and allowing the bias resistors to reestablish a “1” on the twisted pair.

Control over communications is achieved by asserting a “0” during the time an active transmitter is sending a “1”. Any node that is transmitting data watches its own

APPLICATIONS INFORMATION

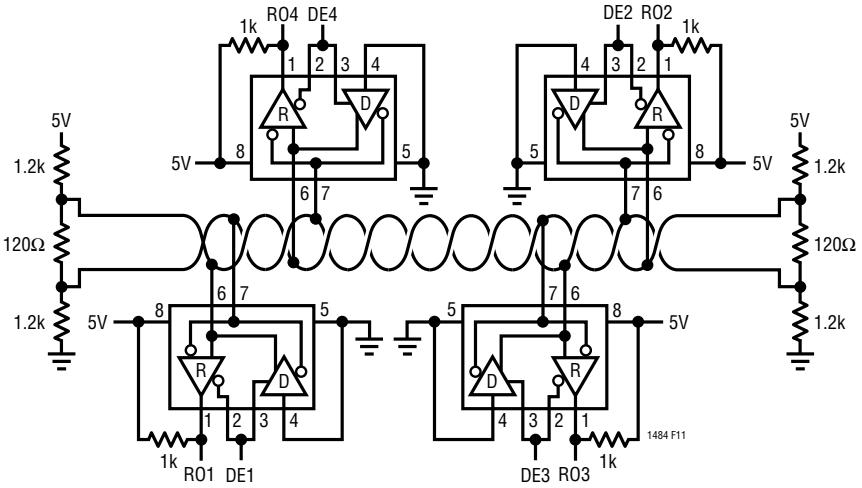


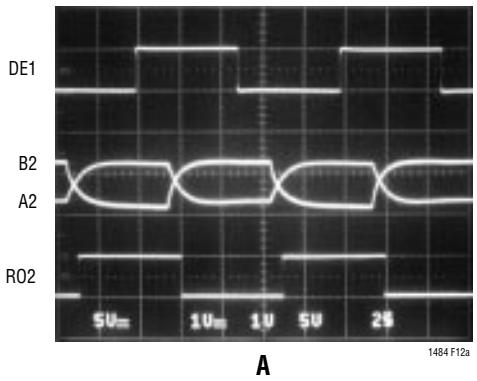
Figure 11. Transmit "0" CDMA Application

receiver output and expects to see perfect agreement between the two data streams. (Note that the driver inverts the data, so the transmitted and received data streams are actually opposites.) If the simultaneously transmitted and received data streams differ (usually detected by comparing RO and DE with an XOR), it signals the presence of a second, active driver. The first driver falls silent, and the second driver seizes control.

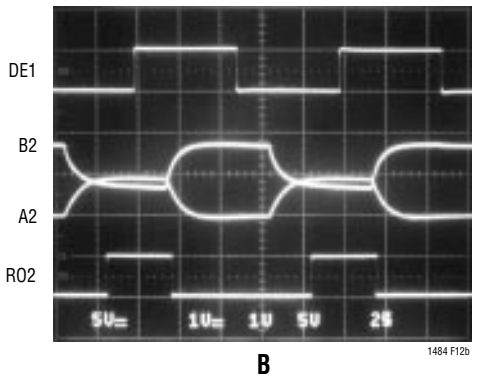
If the LTC1484 is connected as shown in Figure 11, the overhead of XORing the transmitted and received data in hardware or software is eliminated. DE and $\overline{RE}$ are connected together so the receiver is disabled and its output three-stated whenever a "0" is transmitted. A 1k pull-up ensures a "1" at the receiver output during this condition. The receiver is enabled when the driver is disabled. During this interval the receiver output should also be "1". Thus, under normal operation the receiver output is always "1". If a "0" is detected, it indicates the presence of a second active driver attempting to seize control of communications.

The maximum frequency at which the system in Figure 11 can operate is determined by the cable capacitance, the value of the 1.2k pull-up and pull-down resistors and receiver propagation delay. The external resistors take a longer time to pull the line to a "1" state due to higher source resistance compared to an active driver, thereby affecting the duty cycle of the receiver output at the far end of the line.

Figure 12a shows a 100kHz DE1 waveform for an LTC1484 driving a 1000-foot shielded twisted-pair (STP) cable and the A2, B2 and RO2 waveforms of a receiving LTC1484 at the far end of the cable. The propagation delay between DE1 of the driver and RO2 at the far end of the line is 1.8µs at the rising edge and 3.7µs at the falling edge of DE1. The



A



B

Figure 12. LTC1484 Driving a 1000 Foot STP Cable

APPLICATIONS INFORMATION

longer delay for the falling edge is due to the larger voltage range the line must swing (typically >2V compared to 370mV) before the receiver trips high again. The difference in delay affects the duty cycle of the received data and depends on cable capacitance. For a 1-foot STP cable, the delays drop to 0.13µs and 0.4µs. Using smaller valued pull-up and pull-down resistors to equalize the positive and negative voltage swings needed to trip the receivers will reduce the difference in delay and increase the maximum data rate. With 220Ω resistors, both rising and falling edge delays are 2.2µs when driving a 1000-foot STP cable as shown in Figure 12b.

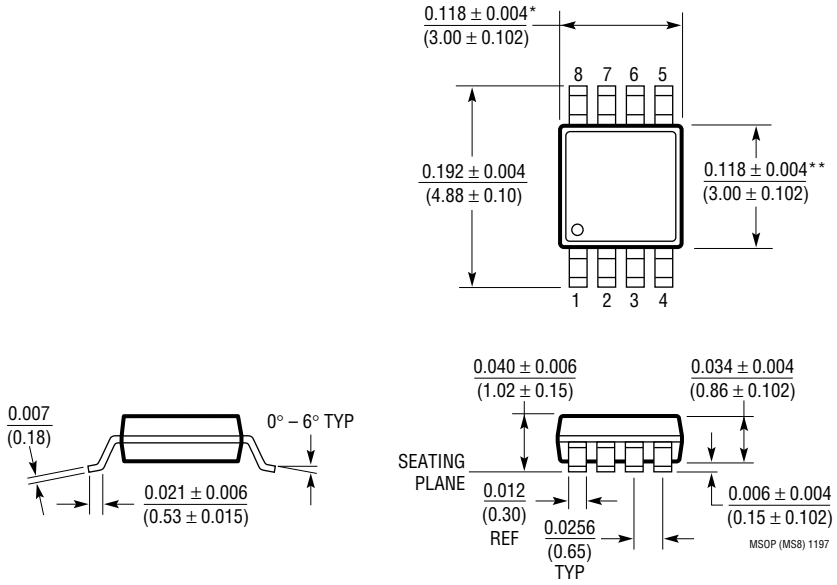
The fail-safe feature of the LTC1484 receiver allows a CDMA system to function without the A and B pull-up and pull-down resistors. However, if the resistors are left out, noise margin will be reduced to as low as 15mV and propagation delays will increase significantly. Operation in this mode is not recommended.

Since DE and $\overline{RE}$ are tied together, the part never shuts down. The receiver inputs are never floating (due to the external bias resistors) so that the t_{DZR} timing does not apply to this application. The whole system can be changed to actively transmit only a "1" by swapping the pull-up and pull-down resistors in Figure 11, shorting DI to V_{CC} and connecting the 1k resistor as a pull-down. In this configuration the driver is noninverting and the receiver output RO truly follows DE.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters), unless otherwise noted.

MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)



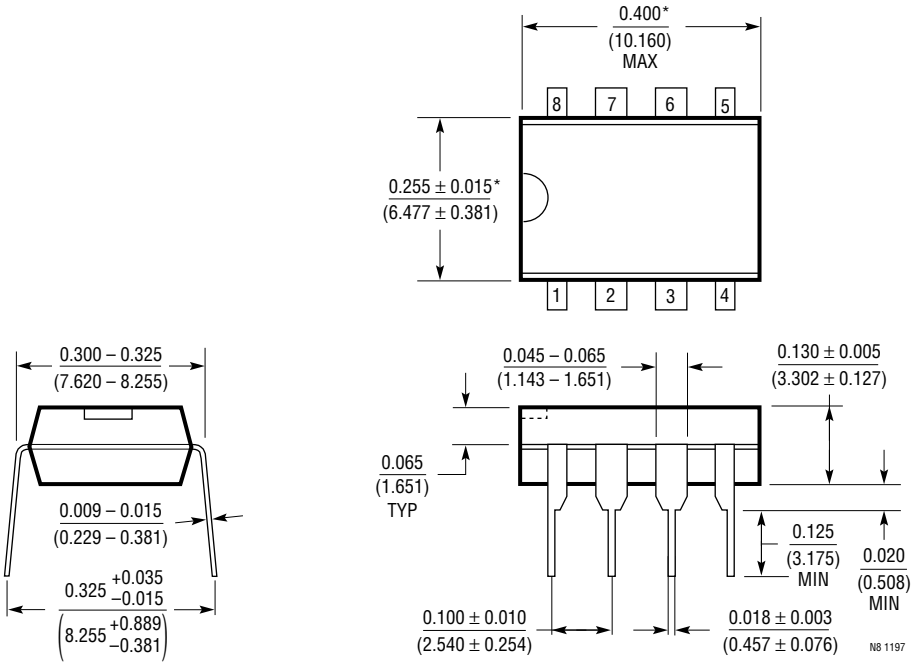
* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters), unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

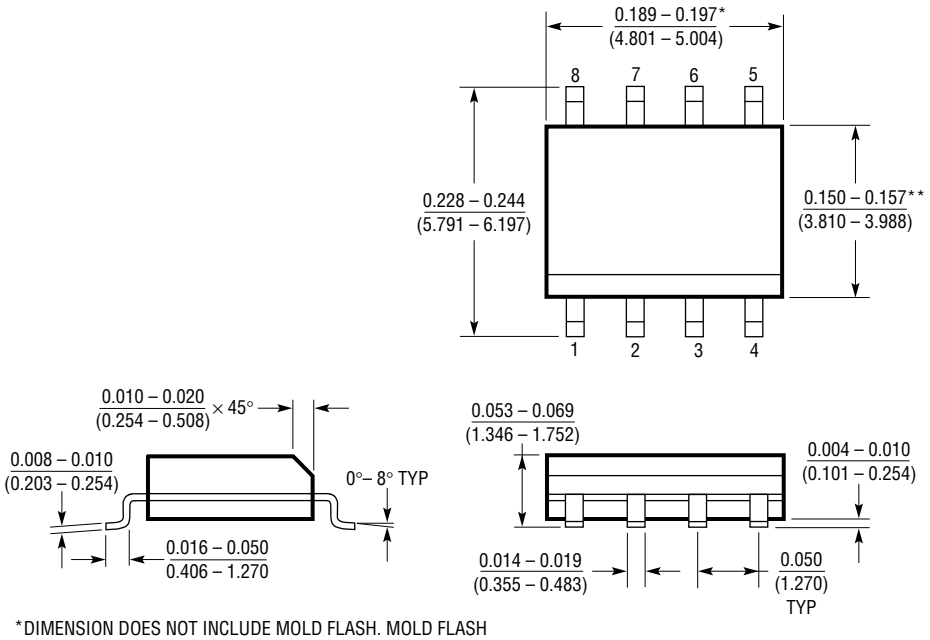


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters), unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 0996

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC485	5V Low Power EIA485 Interface Transceiver	Low Power
LTC1480	3.3V Ultralow Power EIA485 Transceiver with Shutdown	Lower Supply Voltage
LTC1481	5V Ultralow Power EIA485 Transceiver with Shutdown	Lowest Power
LTC1482	5V Low Power EIA485 Transceiver with Carrier Detect Output	Low Power, High Output State When Inputs are Open, Shorted or Terminated
LTC1483	5V Ultralow Power EIA485 Low EMI Transceiver with Shutdown	Low EMI, Lowest Power
LTC1485	5V Differential Bus Transceiver	Highest Speed
LTC1487	5V Ultralow Power EIA485 with Low EMI, Shutdown and High Input Impedance	Highest Input Impedance, Low EMI, Lowest Power
LTC1690	5V Differential Driver and Receiver Pair with Fail-Safe Receiver Output	Low Power

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