

Switched Capacitor Regulated Voltage Inverter

October 1998

FEATURES

- Regulated Negative Voltage from a Single Positive Supply
- REG Pin Indicates Output is in Regulation
- Adjustable or Fixed Output Voltages
- Output Regulation: $\pm 3.5\%$
- Supply Current: 650 μ A Typ
- Shutdown Mode Drops Supply Current to 5 μ A
- Up to 20mA Output Current
- Requires Only Three or Four External Capacitors
- Available in MS8 and SO-8 Packages

APPLICATIONS

- GaAs FET Bias Generators
- Negative Supply Generators
- Battery-Powered Systems
- Single Supply Applications

DESCRIPTION

The LTC[®]1261L is a switched-capacitor voltage inverter designed to provide a regulated negative voltage from a single positive supply. The LTC1261L operates from a single 2.7V to 5.25V supply and provides an adjustable output voltage from -1.23 V to -5 V. The LTC1261L-4/LTC1261L-4.5 needs a single 4.5V to 5.25V supply and provides a fixed output voltage of -4 V to -4.5 V respectively. Three external capacitors are required: a 0.1 μ F flying capacitor and an input and output bypass capacitors. An optional compensation capacitor at ADJ (COMP) can be used to reduce the output voltage ripple.

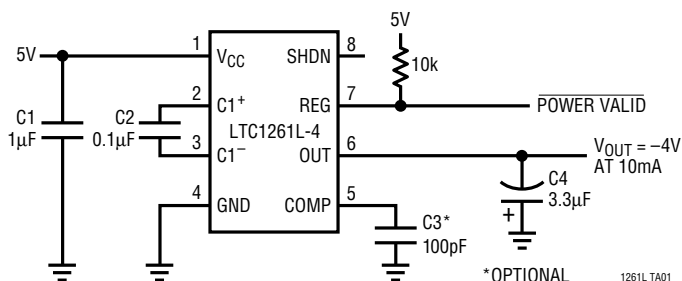
Each version of the LTC1261L will supply up to 20mA output current with guaranteed output regulation of $\pm 3.5\%$. The LTC1261L includes an open-drain REG output that pulls low when the output is within 5% of the set value. Quiescent current is typically 650 μ A when operating and 5 μ A in shutdown.

The LTC1261L is available in an 8-pin MSOP and SO package.

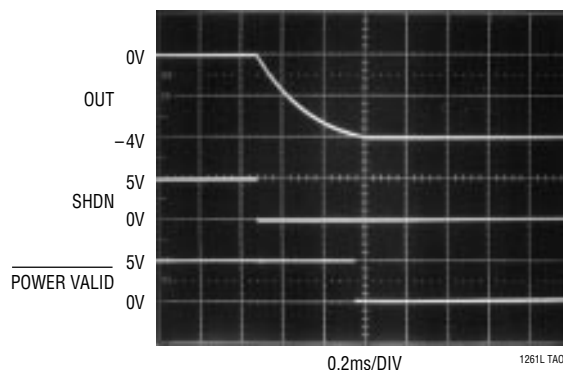
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TYPICAL APPLICATION

-4V Generator with Power Valid



Waveforms for -4V Generator with Power Valid



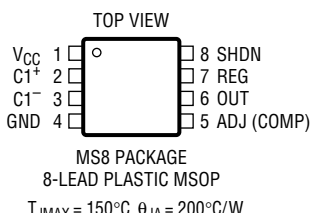
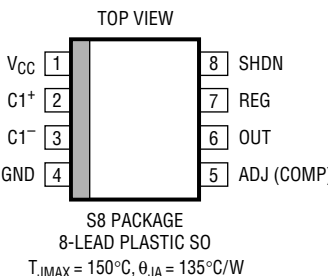
LTC1261L

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (Note 2)	5.5V	Output Short-Circuit Duration	Indefinite
Output Voltage (Note 3)	0.3V to -5.3V	Commercial Temperature Range	0°C to 70°C
Total Voltage, V_{CC} to V_{OUT} (Note 2)	10.8V	Extended Commercial Operating	
SHDN Pin	-0.3V to ($V_{CC} + 0.3V$)	Temperature Range (Note 4)	-40°C to 85°C
REG Pin	-0.3V to 6V	Storage Temperature Range	-65°C to 150°C
ADJ Pin	($V_{OUT} - 0.3V$) to ($V_{CC} + 0.3V$)	Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

 <p>MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 200^{\circ}C/W$</p>	ORDER PART NUMBER	 <p>S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 135^{\circ}C/W$</p>	ORDER PART NUMBER
	LTC1261LCMS8 LTC1261LCMS8-4 LTC1261LCMS8-4.5		LTC1261LCS8 LTC1261LCS8-4 LTC1261LCS8-4.5
	MS8 PART MARKING		S8 PART MARKING
	LTFM LTFN LTFP		1261L 1261L4 261L45

Consult factory for Industrial or Military grade parts or additional fixed voltage parts.

ELECTRICAL CHARACTERISTICS $C_1 = 0.1\mu F$, $C_{OUT} = 3.3\mu F$ (Notes 2, 4) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage (LTC1261LCMS8/LTC1261LCS8) (LTC1261LCMS8-4/LTC1261LCS8-4) (LTC1261LCMS8-4.5/LTC1261LCS8-4.5)	● ● ● (Note 5) (Note 5)	2.7		5.25	V
			4.35		5.25	V
			4.75		5.25	V
V_{REF}	Reference Voltage			1.23		V
I_{CC}	Supply Current	$V_{CC} = 5.25V$, No Load, SHDN Floating	●	650	1500	μA
		$V_{CC} = 5.25V$, No Load, $V_{SHDN} = V_{CC}$	●	5	20	μA
f_{OSC}	Internal Oscillator Frequency	$V_{CC} = 5V$, $V_{OUT} = -4V$		650		kHz
V_{OL}	REG Output Low Voltage	$I_{REG} = 1mA$, $V_{CC} = 5V$, $V_{OUT} = -4V$	●	0.1	0.8	V
I_{REG}	REG Sink Current	$V_{REG} = 0.8V$, $V_{CC} = 3.3V$	●	4	8	mA
		$V_{REG} = 0.8V$, $V_{CC} = 5V$	●	5	12	mA
I_{ADJ}	Adjust Pin Current	$V_{ADJ} = 1.23V$	●	± 0.01	± 1	μA
V_{IH}	SHDN Input High Voltage	$V_{CC} = 5V$	●	2		V
V_{IL}	SHDN Input Low Voltage	$V_{CC} = 5V$	●		0.8	V
I_{IN}	SHDN Input Current	$V_{SHDN} = V_{CC}$	●	2.5	25	μA
t_{ON}	Turn-On Time	$I_{OUT} = 10mA$		250		μs

ELECTRICAL CHARACTERISTICS

$C_1 = 0.1\mu\text{F}$, $C_{\text{OUT}} = 3.3\mu\text{F}$ (Notes 2, 4) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OUT}	Output Regulation (LTC1261L)	$2.70\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$, $0\text{mA} \leq I_{\text{OUT}} \leq 10\text{mA}$	● -1.552	-1.5	-1.448	V
		$3.25\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$, $0\text{mA} \leq I_{\text{OUT}} \leq 20\text{mA}$	● -1.552	-1.5	-1.448	V
		$2.70\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$, $0\text{mA} \leq I_{\text{OUT}} \leq 5\text{mA}$	● -2.070	-2.0	-1.930	V
		$2.95\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$, $0\text{mA} \leq I_{\text{OUT}} \leq 10\text{mA}$	● -2.070	-2.0	-1.930	V
		$3.50\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$, $0\text{mA} \leq I_{\text{OUT}} \leq 20\text{mA}$	● -2.070	-2.0	-1.930	V
		$2.95\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$, $0\text{mA} \leq I_{\text{OUT}} \leq 5\text{mA}$	● -2.587	-2.5	-2.413	V
		$3.30\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$, $0\text{mA} \leq I_{\text{OUT}} \leq 10\text{mA}$	● -2.587	-2.5	-2.413	V
		$3.85\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$, $0\text{mA} \leq I_{\text{OUT}} \leq 20\text{mA}$	● -2.587	-2.5	-2.413	V
		$3.40\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$, $0\text{mA} \leq I_{\text{OUT}} \leq 5\text{mA}$	● -3.105	-3.0	-2.895	V
		$3.70\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$, $0\text{mA} \leq I_{\text{OUT}} \leq 10\text{mA}$	● -3.105	-3.0	-2.895	V
		$4.25\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$, $0\text{mA} \leq I_{\text{OUT}} \leq 20\text{mA}$	● -3.105	-3.0	-2.895	V
		$3.85\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$, $0\text{mA} \leq I_{\text{OUT}} \leq 5\text{mA}$	● -3.622	-3.5	-3.378	V
I_{SC}	Output Short-Circuit Current	$4.10\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$, $0\text{mA} \leq I_{\text{OUT}} \leq 10\text{mA}$	● -3.622	-3.5	-3.378	V
		$4.60\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$, $0\text{mA} \leq I_{\text{OUT}} \leq 20\text{mA}$	● -3.622	-3.5	-3.378	V
		$4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$, $0\text{mA} \leq I_{\text{OUT}} \leq 5\text{mA}$	● -4.657	-4.5	-4.343	V
I_{SC}	Output Short-Circuit Current	$5.05\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$, $0\text{mA} \leq I_{\text{OUT}} \leq 10\text{mA}$	● -4.657	-4.5	-4.343	V
		$V_{\text{OUT}} = 0\text{V}$, $V_{\text{CC}} = 5.25\text{V}$	● 100	220		mA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: The Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

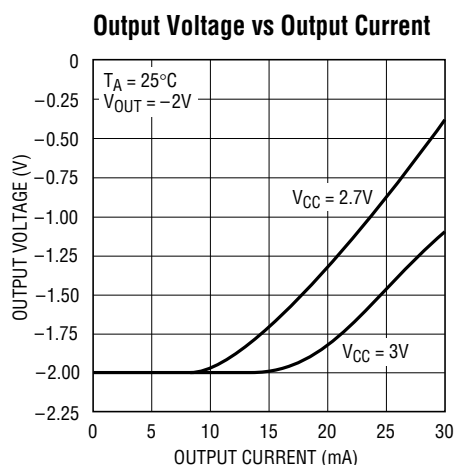
Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 3: The output should never be set to exceed $V_{\text{CC}} - 10.8\text{V}$.

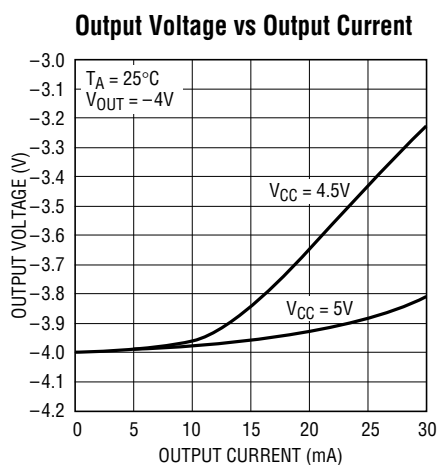
Note 4: The LTC1261L is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet these extended commercial temperature limits, but is not tested at -40°C and 85°C . Guaranteed I grade parts are available, consult factory.

Note 5: The LTC1261L-4 and LTC1261L-4.5 will operate with less than the minimum V_{CC} specified in the electrical characteristics table, but they are not guaranteed to meet the $\pm 3.5\%$ V_{OUT} specification.

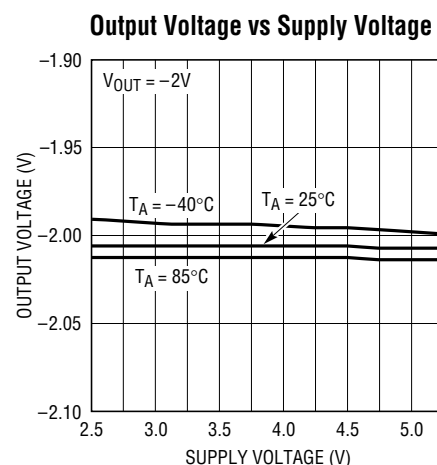
TYPICAL PERFORMANCE CHARACTERISTICS (See Test Circuits)



1261L G01



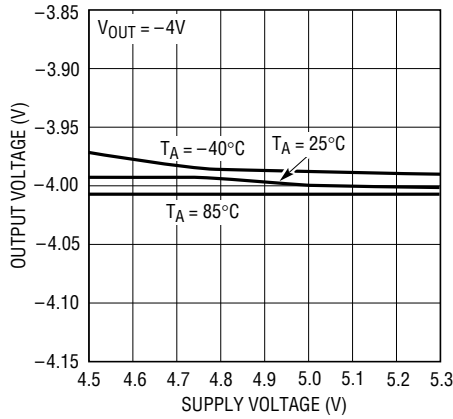
1261L G02



1261L G03

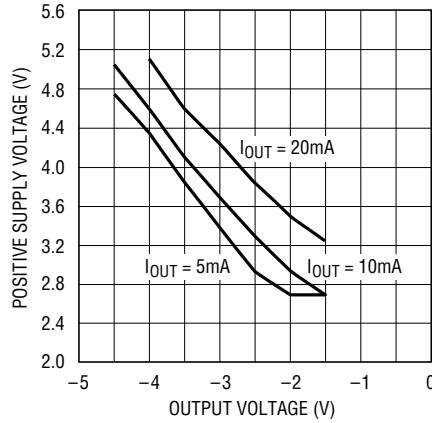
TYPICAL PERFORMANCE CHARACTERISTICS (See Test Circuits)

Output Voltage vs Supply Voltage



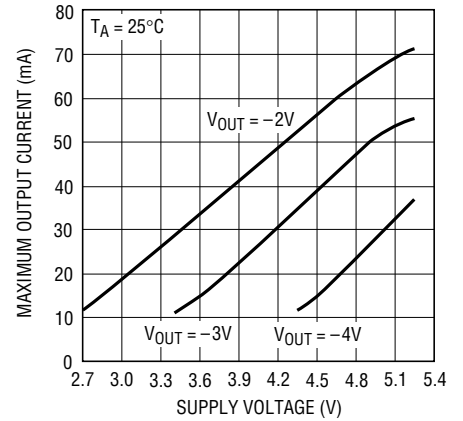
1261L G04

Minimum Required V_{CC} vs V_{OUT} and I_{OUT}



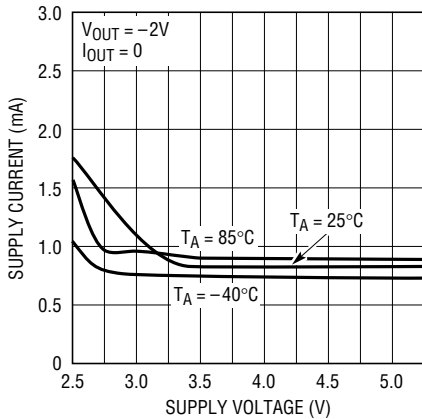
1261L G05

Maximum Output Current vs Supply Voltage



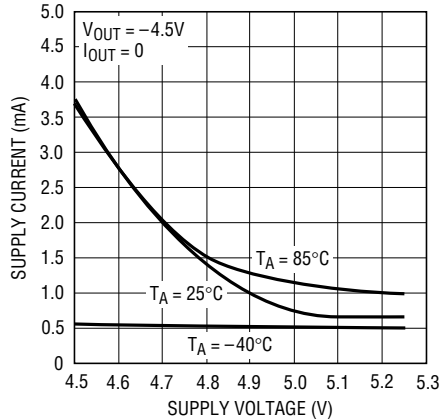
1261L G06

Supply Current vs Supply Voltage



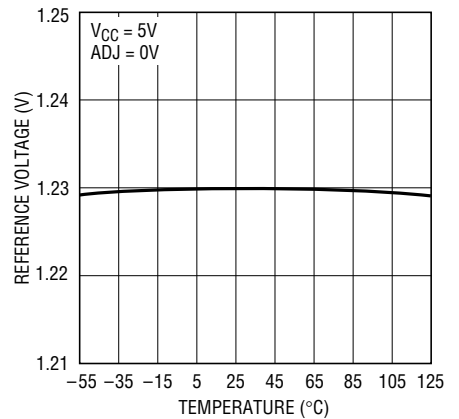
1261L G07

Supply Current vs Supply Voltage



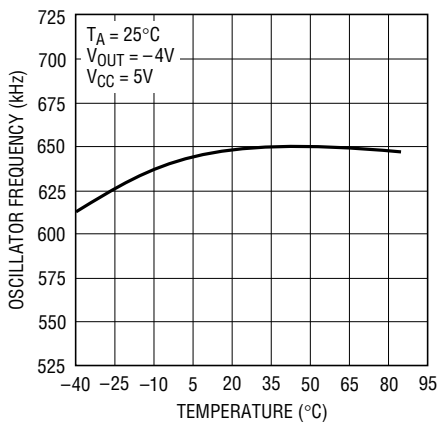
1261L G08

Reference Voltage vs Temperature



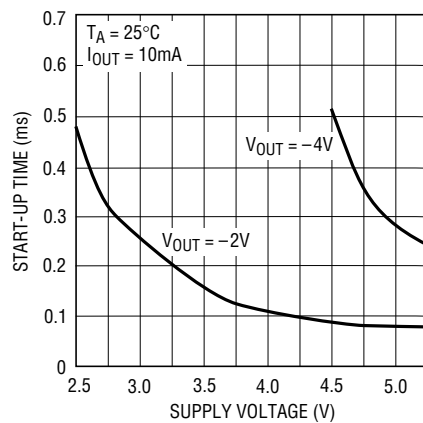
1261L G09

Oscillator Frequency vs Temperature



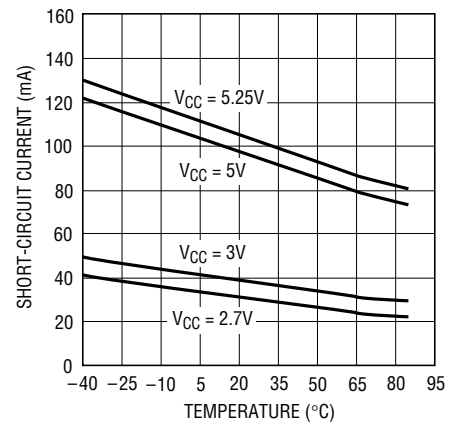
1261L G10

Start-Up Time vs Supply Voltage



1261L G11

Output Short-Circuit Current vs Temperature



1261L G12

PIN FUNCTIONS

V_{CC} (Pin 1): Power Supply. This requires an input voltage between 2.7V and 5.25V. V_{CC} must be bypassed to ground with at least a 1 μ F capacitor placed in close proximity to the chip. See the Applications Information section for details.

C1⁺ (Pin 2): C1 Positive Input. Connect a 0.1 μ F capacitor between C1⁺ and C1⁻.

C1⁻ (Pin 3): C1 Negative Input. Connect a 0.1 μ F capacitor from C1⁺ to C1⁻.

GND (Pin 4): Ground. Connect to a low impedance ground. A ground plane will help to minimize regulation errors.

ADJ (COMP for fixed versions) (Pin 5): Output Adjust/Compensation Pin. For adjustable parts this pin is used to set the output voltage. The output voltage is divided down with an external resistor divider and fed back to this pin to set the regulated output voltage. Typically the resistor string should draw $\geq 10\mu$ A from the output to minimize errors due to the bias current at the adjust pin. Fixed output voltage parts have the internal resistor string connected to this pin inside the package. The pin can be used to trim the output voltage if desired. It can

also be used as an optional feedback compensation pin to reduce output ripple on both the adjustable and fixed output voltage parts. See the Applications Information section for more information on compensation and output ripple.

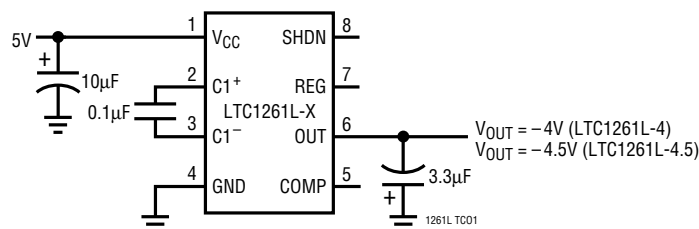
OUT (Pin 6): Negative Voltage Output. This pin must be bypassed to ground with a 1 μ F or larger capacitor. The value of the output capacitor and its ESR have a strong effect on output ripple. See the Applications Information section for more details.

REG (Pin 7): This is an open-drain output that pulls low when the output voltage is within 5% of the set value. It will sink 5mA to ground with a 5V supply. The external circuitry must provide a pull-up or REG will not swing high. The voltage at REG may exceed V_{CC} and can be pulled up to 6V above ground without damage.

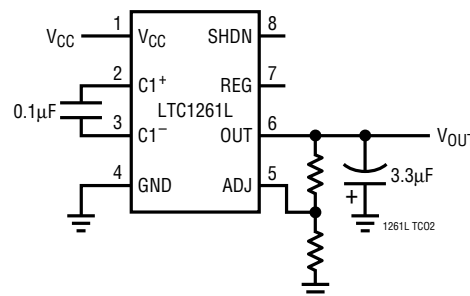
SHDN (Pin 8): Shutdown. When this pin is at ground the LTC1261L operates normally. An internal 5 μ A pull-down keeps SHDN low if it is left floating. When SHDN is pulled high, the LTC1261L enters shutdown mode. In shutdown, the charge pump is disabled, the output collapses to 0V and the quiescent current drops to 5 μ A typically.

TEST CIRCUITS

Fixed Output



Adjustable Output



APPLICATIONS INFORMATION

The LTC1261L uses an inverting charge pump to generate a regulated negative output voltage that is either equal to or less than the supply voltage. The LTC1261L needs only three external capacitors and is available in the MSOP and SO-8 packages

THEORY OF OPERATION

A block diagram of the LTC1261L is shown in Figure 1. The heart of the LTC1261L is the charge pump core shown in the dashed box. It generates a negative output voltage by first charging the flying capacitor (C1) between V_{CC} and ground. It then connects the top of the flying capacitor to ground, forcing the bottom of the flying capacitor to a negative voltage. The charge on the flying capacitor is transferred to the output bypass capacitor, leaving it charged to the negative output voltage. This process is driven by the internal 650kHz clock.

Figure 1 shows the charge pump configuration. With the clock low, C1 is charged to V_{CC} by S1 and S3. At the next rising clock edge, S1 and S3 are open and S2 and S4 close.

S2 connects $C1^+$ to ground, $C1^-$ is connected to the output by S4. The charge in $C1$ is transferred to C_{OUT} , setting it to a negative voltage.

The output voltage is monitored by COMP1 which compares a divided replica of the output at ADJ (COMP for fixed output voltage parts) to the internal reference. At the beginning of a cycle the clock is low, forcing the output of the AND gate low and charging the flying capacitor. The next rising clock edge sets the RS latch, setting the charge pump to transfer charge from the flying capacitor to the output capacitor. As long as the output is below the set point, COMP1 stays low, the latch stays set and the charge pump runs at the full 50% duty cycle of the clock gated through the AND gate. As the output approaches the set voltage, COMP1 will trip whenever the divided signal exceeds the internal 1.23V reference relative to OUT. This resets the RS latch and truncates the clock pulses, reducing the amount of charge transferred to the output capacitor and regulating the output voltage. If the output exceeds the set point, COMP1 stays high, inhibiting the RS latch and disabling the charge pump.

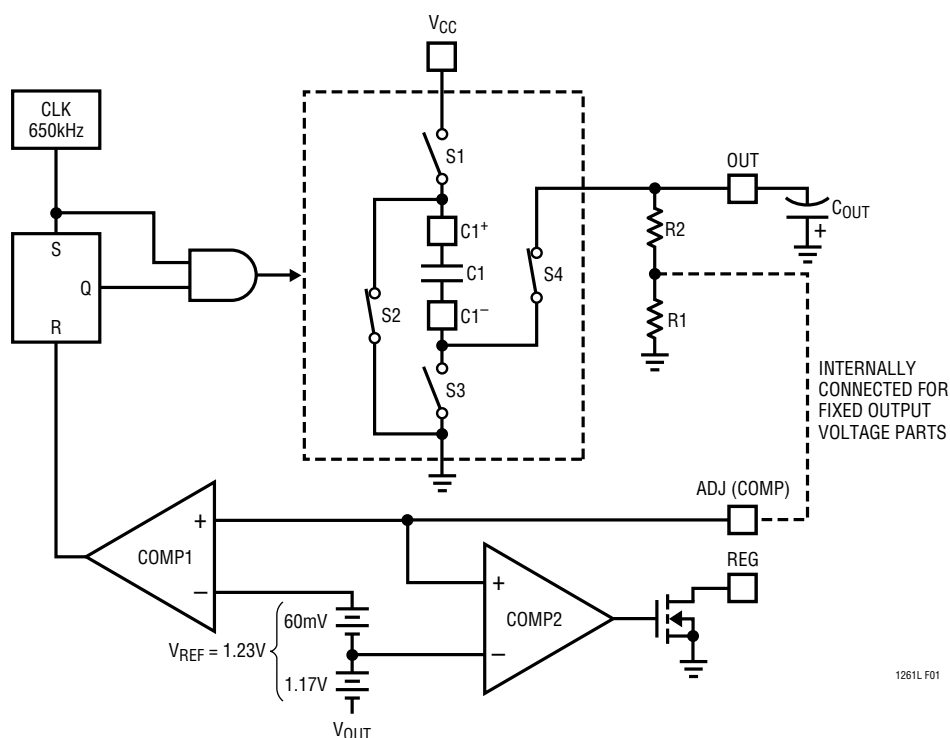


Figure 1. Block Diagram

APPLICATIONS INFORMATION

COMP2 also monitors the divided signal at ADJ but it is connected to a 1.17V reference, 5% below the main reference voltage. When the divided output exceeds this lower reference voltage indicating that the output is within 5% of the set value, COMP2 goes high turning on the REG output transistor. This is an open drain N-channel device capable of sinking 4mA with a 3.3V V_{CC} and 5mA with a 5V V_{CC} . When in the “off” state (divided output is more than 5% below V_{REF}) the drain can be pulled above V_{CC} without damage up to a maximum of 6V above ground. Note that the REG output only indicates if the magnitude of the output is *below* the magnitude of the set point by 5% (i.e., $V_{OUT} > -4.75V$ for a $-5V$ set point). If the magnitude of the output is forced *higher* than the magnitude of the set point (i.e., to $-5.25V$ when the output is set for $-5V$) the REG output will stay low.

OUTPUT RIPPLE

Output ripple in the LTC1261L is present from two sources; voltage droop at the output capacitor between clocks and frequency response of the regulation loop. Voltage droop is easy to calculate. With a typical clock frequency of 650kHz, the charge on the output capacitor is refreshed once every 1.54 μ s. With a 15mA load and a 3.3 μ F output capacitor, the output will droop by:

$$I_{LOAD} \left(\frac{\Delta t}{C_{OUT}} \right) = 15mA \left(\frac{1.54\mu s}{3.3\mu F} \right) = 7mV$$

This can be a significant ripple component when the output is heavily loaded, especially if the output capacitor is small. If absolute minimum output ripple is required, a 10 μ F or greater output capacitor should be used.

Regulation loop frequency response is the other major contributor to output ripple. The LTC1261L regulates the output voltage by limiting the amount of charge transferred to the output capacitor on a cycle-by-cycle basis. The output voltage is sensed at the ADJ pin (COMP for fixed output voltage versions) through an internal or external resistor divider from the OUT pin to ground. As the flying capacitor is first connected to the output, the output voltage begins to change quite rapidly. As soon as it exceeds the set point COMP1 trips, switching the state

of the charge pump and stopping the charge transfer. Because the RC time constant of the capacitors and the switches is quite short, the ADJ pin must have a wide AC bandwidth to be able to respond to the output in time. External parasitic capacitance at the ADJ pin can reduce the bandwidth to the point where the comparator cannot respond by the time the clock pulse finishes. When this happens the comparator will allow a few complete pulses through, then overcorrect and disable the charge pump until the output drops below the set point. Under these conditions the output will remain in regulation but the output ripple will increase as the comparator “hunts” for the correct value.

To prevent this from happening, an external capacitor can be connected from ADJ (or COMP for fixed output voltage parts) to ground to compensate for external parasitics and increase the regulation loop bandwidth (Figure 2). This sounds counterintuitive until we remember that the internal reference is generated with respect to OUT, not ground. The feedback loop actually sees ground as its “output,” thus the compensation capacitor should be connected across the “top” of the resistor divider, from ADJ (or COMP) to ground. By the same token, avoid adding capacitance between ADJ (or COMP) and V_{OUT} . This will slow down the feedback loop and increase output ripple. A 100pF capacitor from ADJ or COMP to ground will compensate the loop properly under most conditions for fixed voltage versions of the LTC1261L. For the adjustable LTC1261L, the capacitor value will be dependent upon the values of the external resistors in the divider network.

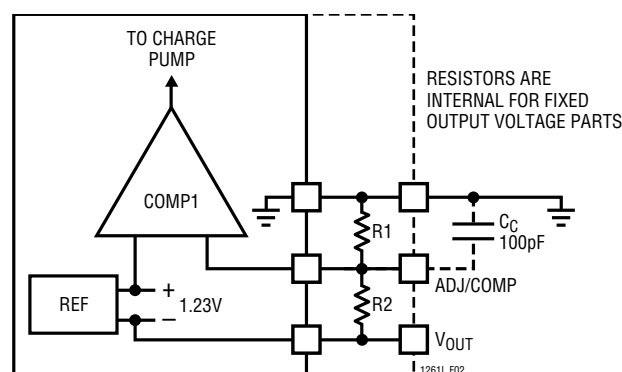


Figure 2. Regulator Loop Compensation

APPLICATIONS INFORMATION

OUTPUT FILTERING

If extremely low output ripple (<5mV) is required, additional output filtering is required. Because the LTC1261L uses a high 650kHz switching frequency, fairly low value RC or LC networks can be used at the output to effectively filter the output ripple. A 10 Ω series output resistor and a 3.3 μ F capacitor will cut output ripple to below 3mV (Figure 3). Further reductions can be obtained with larger filter capacitors or by using an LC output filter.

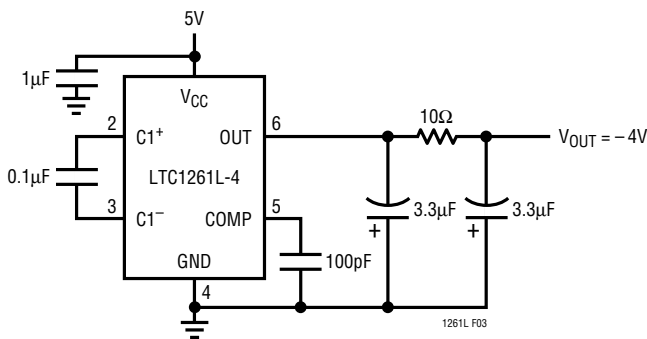


Figure 3. Output Filter Cuts Ripple Below 3mV

CAPACITOR SELECTION

Capacitor Sizing

The performance of the LTC1261L is affected by the capacitors to which it connects. The LTC1261L requires bypass capacitors to ground for both the V_{CC} and OUT pins. The input capacitor provides most of LTC1261L's supply current while it is charging the flying capacitors. This capacitor should be mounted as close to the package as possible and its value should be at least ten times larger than the flying capacitor. Ceramic capacitors generally provide adequate performance. Avoid using a tantalum capacitor as the input bypass unless there is at least a 0.1 μ F ceramic capacitor in parallel with it. The charge pump capacitor is somewhat less critical since its peak current is limited by the switches inside the LTC1261L. Most applications should use a 0.1 μ F as the flying capacitor value. Conveniently, ceramic capacitors are the most common type of 0.1 μ F capacitor and they work well here. Usually the easiest solution is to use the same

capacitor type for both the input bypass capacitor and the flying capacitor.

In applications where the maximum load current is well-defined and output ripple is critical or input peak currents need to be minimized, the flying capacitor value can be tailored to the application. Reducing the value of the flying capacitor reduces the amount of charge transferred with each clock cycle. This limits maximum output current, but also cuts the size of the voltage step at the output with each clock cycle. The smaller capacitor draws smaller pulses of current out of V_{CC} as well, limiting peak currents and reducing the demands on the input supply. Table 1 shows recommended values of flying capacitor vs maximum load capacity.

Table 1. Typical Max Load (mA) vs Flying Capacitor Value at T_A = 25°C, V_{OUT} = -4V

FLYING CAPACITOR VALUE (μ F)	MAX LOAD (mA) V _{CC} = 5V
0.1	20
0.047	15
0.033	10
0.022	5
0.01	1

The output capacitor performs two functions: it provides output current to the load during half of the charge pump cycle and its value helps to set the output ripple voltage. For applications that are insensitive to output ripple, the output bypass capacitor can be as small as 1 μ F. Larger output capacitors will reduce output ripple further at the expense of turn-on time.

Capacitor ESR

Output capacitor Equivalent Series Resistance (ESR) is another factor to consider. Excessive ESR in the output capacitor can fool the regulation loop into keeping the output artificially low by prematurely terminating the charging cycle. As the charge pump switches to recharge the output a brief surge of current flows from the flying capacitors to the output capacitor. This current surge can be as high as 100mA under full load conditions. A typical

APPLICATIONS INFORMATION

3.3 μ F tantalum capacitor has 1 Ω or 2 Ω of ESR; 100mA \times 2 Ω = 200mV. If the output is within 200mV of the set point this additional 200mV surge will trip the feedback comparator and terminate the charging cycle. The pulse dissipates quickly and the comparator returns to the correct state, but the RS latch will not allow the charge pump to respond until the next clock edge. This prevents the charge pump from going into very high frequency oscillation under such conditions but it also creates an output error as the feedback loop regulates based on the top of the spike, not the average value of the output (Figure 4). The resulting output voltage behaves as if a resistor of value $C_{ESR} \times (I_{PK}/I_{AVE})\Omega$ was placed in series with the output. To avoid this nasty sequence of events, connect a 0.1 μ F ceramic capacitor in parallel with the larger output capacitor. The ceramic capacitor will “eat” the high frequency spike, preventing it from fooling the feedback loop, while the larger but slower tantalum or aluminum output capacitor supplies output current to the load between charge cycles.

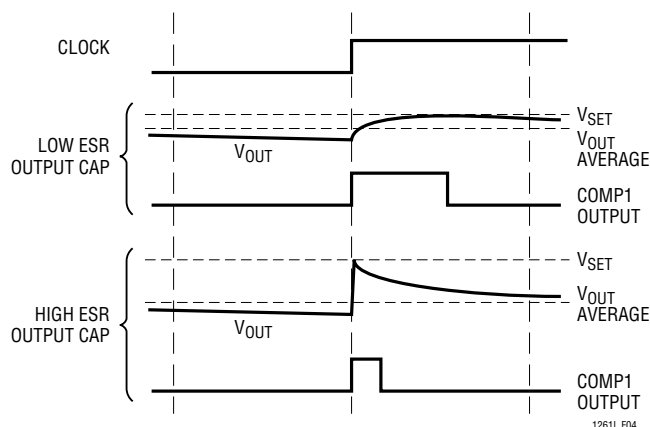


Figure 4. Output Ripple with Low and High ESR Capacitors

Note that ESR in the flying capacitor will not cause the same condition; in fact, it may actually improve the situation by cutting the peak current and lowering the amplitude of the spike. However, more flying capacitor ESR is not necessarily better. As soon as the RC time constant

approaches half of a clock period (the time the capacitors have to share charge at full duty cycle) the output current capability of the LTC1261L starts to diminish. For a 0.1 μ F flying capacitor, this gives a maximum total series resistance of:

$$\frac{1}{2} \left(\frac{t_{CLK}}{C_{FLY}} \right) = \frac{1}{2} \left(\frac{1}{650kHz} \right) / 0.1\mu F = 7.7\Omega$$

Most of this resistance is already provided by the internal switches in the LTC1261L. More than 1 Ω or 2 Ω of ESR on the flying capacitors will start to affect the regulation at maximum load.

RESISTOR SELECTION

Resistor selection is easy with the fixed output voltage versions of the LTC1261L—no resistors are needed! Selecting the right resistors for the adjustable parts is only a little more difficult. A resistor divider should be used to divide the signal at the output to give 1.23V at the ADJ pin *with respect to* V_{OUT} (Figure 5). The LTC1261L uses a positive reference with respect to V_{OUT} , not a negative reference with respect to ground (Figure 1 shows the reference connection). Be sure to keep this in mind when connecting the resistors! If the initial output is not what you expected, try swapping the two resistors.

The LTC1261L can be internally configured for other fixed output voltages. Contact the Linear Technology Marketing department for details.

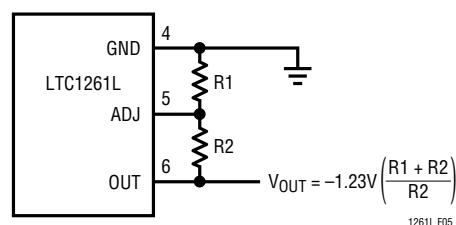
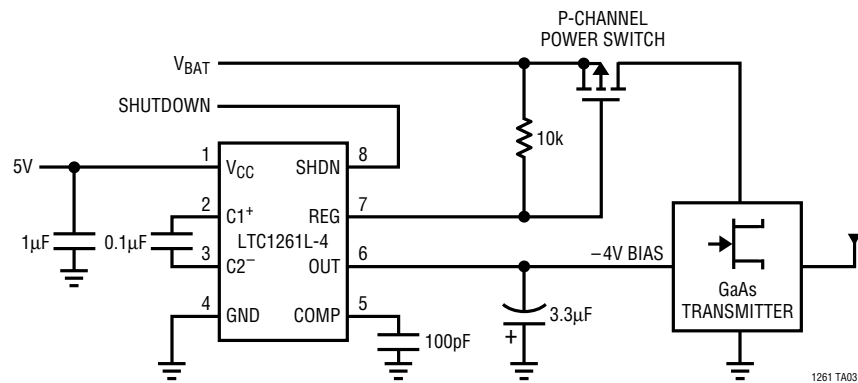


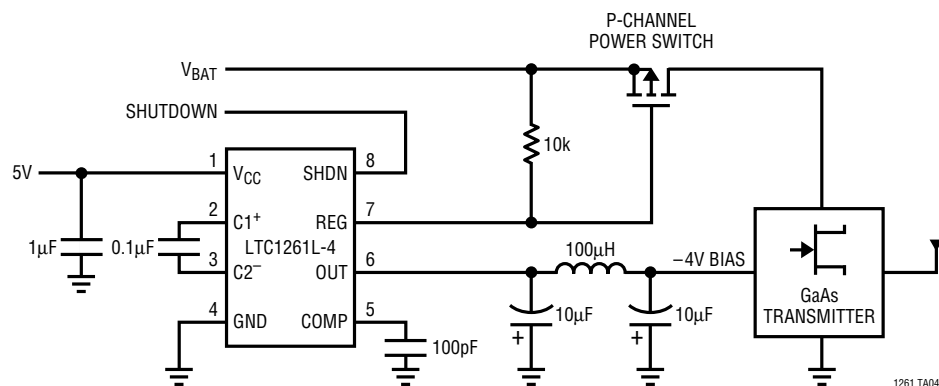
Figure 5. External Resistor Connections

TYPICAL APPLICATIONS

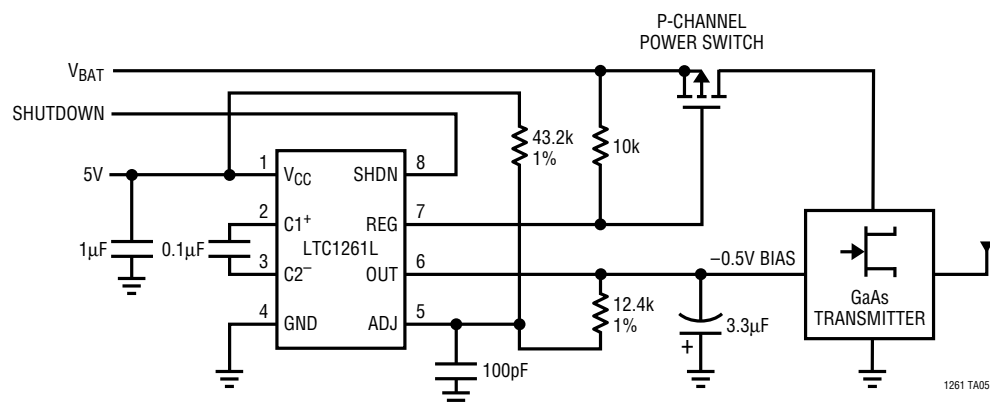
5V Input, -4V Output GaAs FET Bias Generator



1mV Ripple, 5V Input, -4V Output GaAs FET Bias Generator



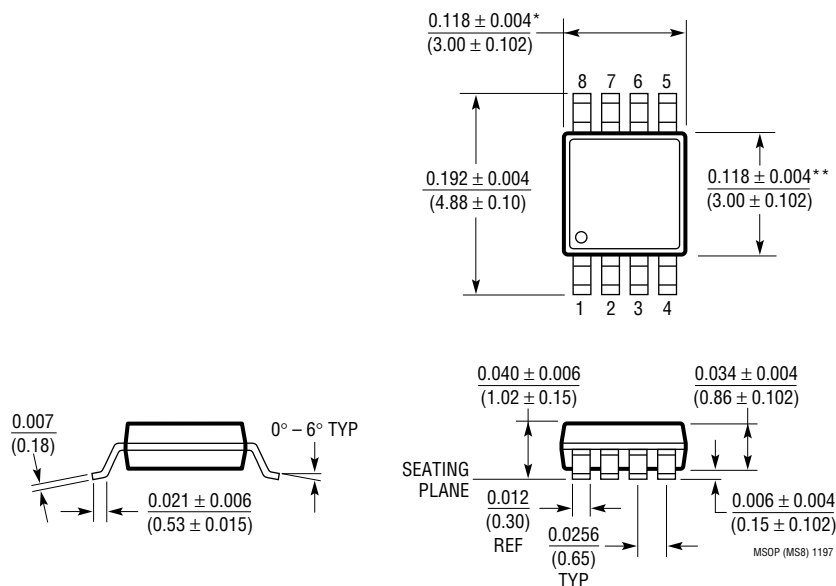
5V Input, -0.5V Output GaAs FET Bias Generator



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

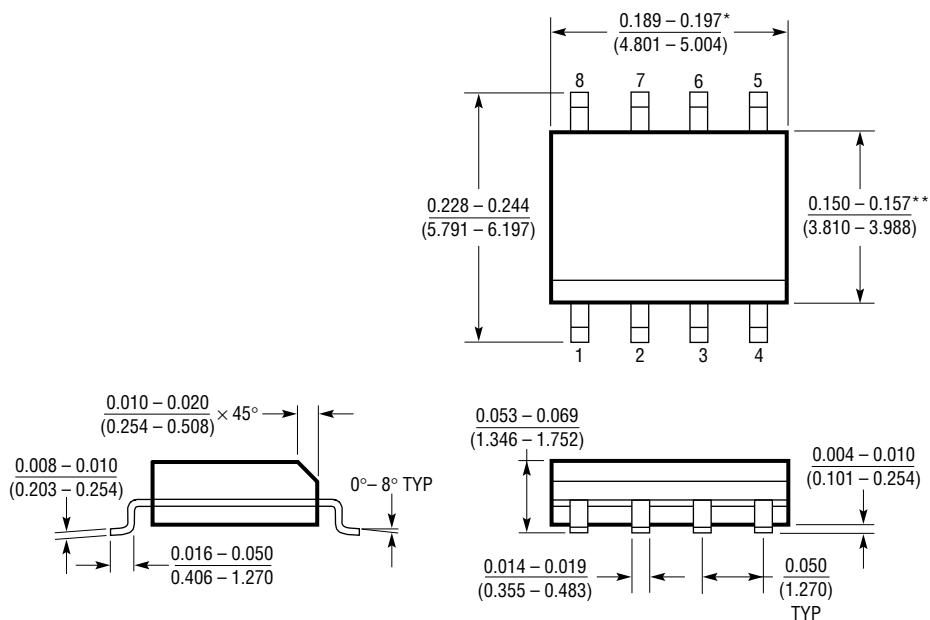
MS8 Package 8-Lead Plastic MSOP (LTC DWG # 05-08-1660)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

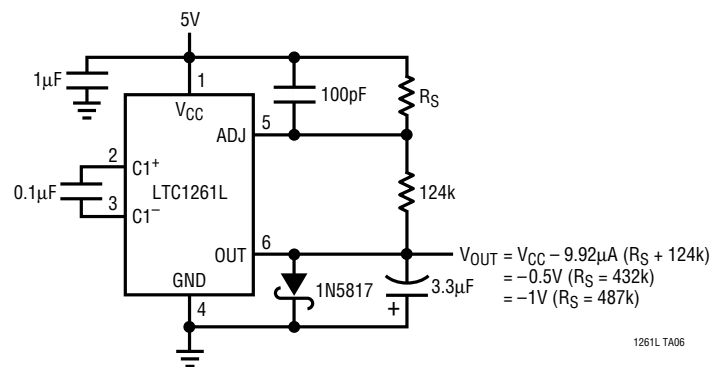
** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SOP 0996

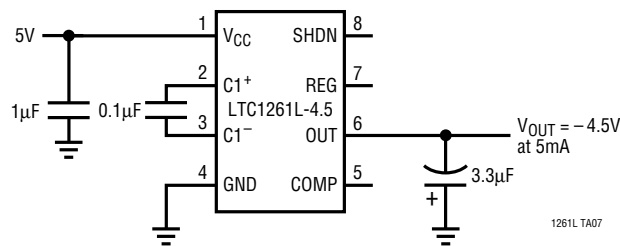
LTC1261L

TYPICAL APPLICATIONS

Low Output Voltage Generator



Minimum Parts Count – 4.5V Generator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1550L/LTC1551L	Low Noise Switched Capacitor Regulated Voltage Inverter	GaAs FET Bias with Linear Regulator, < 1mV Ripple, MSOP
LTC1429	Clock Synchronized Switched Capacitor Regulated Voltage Inverter	GaAs FET Bias
LT1121	Micropower Low Dropout Regulator with Shutdown	0.4V Dropout Voltage at 150mA, Low Noise, Switched Capacitor Regulated Voltage Inverter