PRODUCT INFORMATION

SHARP

Integrated Circuits Group

APPLICATIONS:
Pager
PDA
Set Top Box
Cellular Phone

LRS1306 Stacked Chip

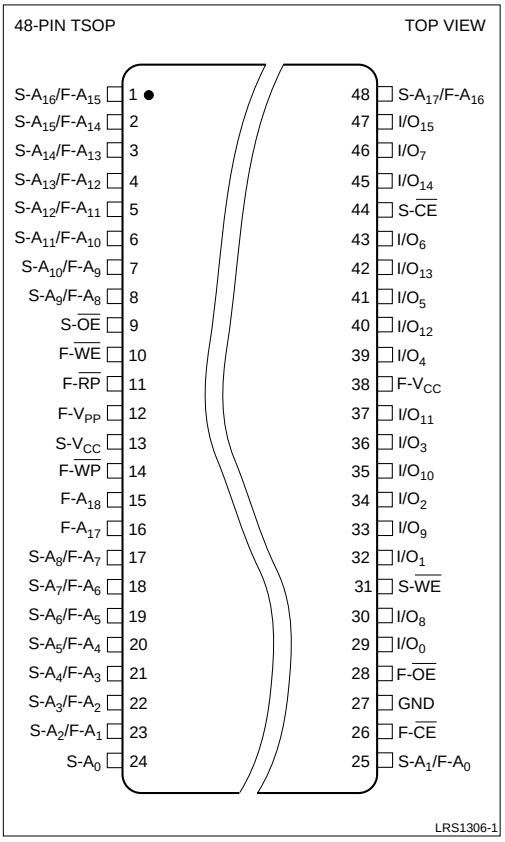
FEATURES

- 8M Flash and 2 M SRAM
- Flash memory access time 120 ns MAX.
- SRAM access time 85 ns MAX.
- Operating current
  - Flash memory read 25 mA MAX. (t_{CYCLE} = 200 ns)
  - Flash word write 57 mA MAX. (F-V_{CC} ≥ 3.0 V)
  - Flash block erase 42 mA MAX. (F-V_{CC} ≥ 3.0 V)
  - SRAM operating 25 mA MAX. (t_{CYCLE} = 200 ns)
- Standby current
  - Flash memory 25 µA MAX.
    (F-$\overline{CE}$ ≥ F-V_{CC} – 0.2 V, F-$\overline{RP}$ ≤ 0.2 V, F-V_{PP} ≤ 0.2 V)
  - SRAM 120 µA MAX. (S-$\overline{CE}$ ≥ S-V_{cc} – 0.2 V)
    1.0 µA TYP. (T_A = 25°C, S-V_{CC} = 3 V, S-$\overline{CE}$ ≥ S-V_{CC} – 0.2 V)
  - Total standby current is the summation of flash memory's standby current and SRAM's standby current
- Power supply 2.7 V to 3.6 V.
- Operating temperature -40°C to +85°C
  - Block erase and word write operations of flash memory with T_A < -30°C are Not Supported
- Fully static operation
- Three-state output
- Not designed or rated as radiation hardened
- 48-pin TSOP (TSOP48-P-1014) plastic package
- Flash Memory has P-type bulk silicon, and SRAM has N-type bulk silicon

DESCRIPTION

The LRS1306 is a combination memory organized as 524,288 × 8 bit flash memory and 262,144 × 8 bit static RAM in one package. It is fabricated using silicon-gate CMOS process technology.

48-PIN TSOP PINOUT



PIN DESCRIPTION

PIN	DESCRIPTION
S-A_1/F-A_0 to S-A_{17}/F-A_{16}	Common Address Input Pins
S-A_0	Address Input Pin for SRAM
F-A_{17} to F-A_{18}	Address Input Pin for Flash Memory
F-$\overline{CE}$	Chip Enable Input Pin for Flash Memory
S-$\overline{CE}$	Chip Enable Input Pin for SRAM
F-$\overline{WE}$	Write Enable Input Pin for Flash Memory
S-$\overline{WE}$	Write Enable Input Pin for SRAM
F-$\overline{OE}$	Output Enable Input Pin for Flash Memory
S-$\overline{OE}$	Output Enable Input Pin for SRAM
I/O_0 to I/O_7	Common Data Input/Output Pins
I/O_8 to I/O_{15}	Data Input/Output Pins for Flash Memory
F-$\overline{RP}$	Reset/Deep Power Down Input Pin for Flash Memory
F-$\overline{WP}$	Write Protect Pin for Flash Memory's Boot Block
F-V_{CC}	Power Supply Pin for Flash Memory
F-V_{PP}	Power Supply for Flash Memory Write/Erase
S-V_{CC}	Power Supply Pin for SRAM
GND	Common GND

The information for this document is from Specification No. EL09X159A, issued on December 11, 1997.