

LRS1302 Stacked Chip

APPLICATIONS:

Pager
PDA
Set Top Box
Cellular Phone

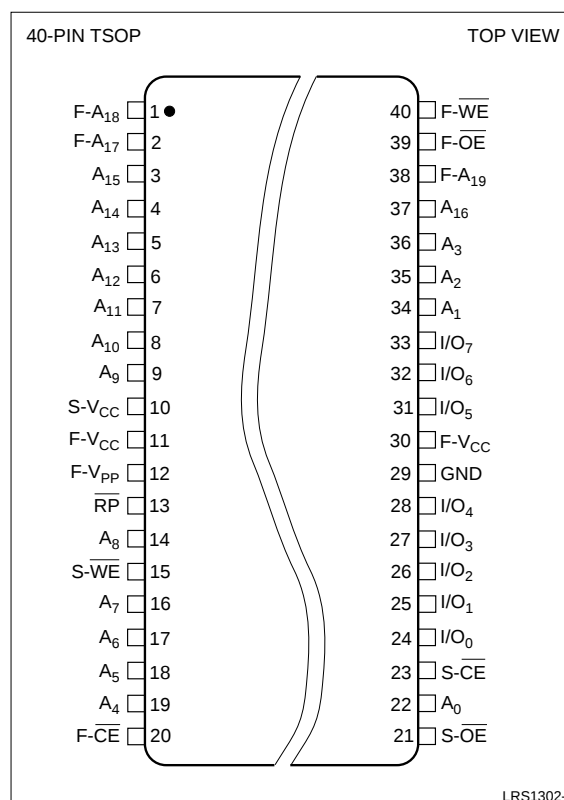
FEATURES

- 8M Flash and 1M SRAM
- Flash memory access time 130 ns MAX.
- SRAM access time 70 ns MAX.
- Operating current
 - Flash memory read 12 mA MAX. ($t_{\text{CYCLE}} = 200 \text{ ns}$)
 - Flash byte write 57 mA MAX.
 - Flash block erase 37 mA MAX.
 - SRAM operating 25 mA MAX. ($t_{\text{CYCLE}} = 200 \text{ ns}$)
- Standby current
 - Flash memory 20 μA MAX.
($F\text{-}\overline{\text{CE}} \geq F\text{-}V_{\text{CC}} - 0.2 \text{ V}$, $\overline{\text{RP}} \leq 0.2 \text{ V}$, $F\text{-}V_{\text{PP}} \leq 0.2 \text{ V}$)
 - SRAM 50 μA MAX. ($S\text{-}\overline{\text{CE}} \geq S\text{-}V_{\text{CC}} - 0.2 \text{ V}$)
0.7 μA TYP. ($T_A = 25^\circ\text{C}$, $S\text{-}V_{\text{CC}} = 3 \text{ V}$, $S\text{-}\overline{\text{CE}} \geq S\text{-}V_{\text{CC}} - 0.2 \text{ V}$)
 - Total standby current is the summation of flash memory's standby current and SRAM's standby current
- Power supply 2.7 V to 3.6 V. (Block erase, byte write and lock-bit configuration operations with $V_{\text{CC}} \leq 3.0 \text{ V}$ are not supported)
- SRAM data retention current 1.0 μA MAX. ($V_{\text{CCDR}} = 3 \text{ V}$, $T_A = 25^\circ\text{C}$)
- Operating temperature -40°C to $+85^\circ\text{C}$
- Fully static operation
- Three-state output
- Not designed or rated as radiation hardened
- 40-pin TSOP (TSOP40-P-0813) plastic package
- Flash memory has P-type bulk silicon, and SRAM has N-type bulk silicon

DESCRIPTION

The LRS1302 is a combination memory organized as $1,048,576 \times 8$ bit flash memory and $131,072 \times 8$ bit static RAM in one package. It is fabricated using silicon-gate CMOS process technology.

40-PIN TSOP PINOUT



PIN DESCRIPTION

PIN	DESCRIPTION
A ₀ to A ₁₆	Common Address Input Pins
F-A ₁₇ to F-A ₁₉	Address Input Pins for Flash Memory
F- $\overline{\text{CE}}$	Chip Enable Input Pin for Flash Memory
S- $\overline{\text{CE}}$	Chip Enable Input Pin for SRAM
F- $\overline{\text{WE}}$	Write Enable Input Pin for Flash Memory
S- $\overline{\text{WE}}$	Write Enable Input Pin for SRAM
F- $\overline{\text{OE}}$	Output Enable Input Pin for Flash Memory
S- $\overline{\text{OE}}$	Output Enable Input Pin for SRAM
I/O ₀ to I/O ₇	Common Data Input/Output Pins
$\overline{\text{RP}}$	Reset/Deep Power Down Input Pin for Flash Memory
F-V _{CC}	Power Supply Pin for Flash Memory
F-V _{PP}	Power Supply for Flash Memory Write/Erase
S-V _{CC}	Power Supply Pin for SRAM
GND	Common GND