PRODUCT INFORMATION

SHARP

Integrated Circuits Group

APPLICATIONS:
Pager
PDA
Set Top Box
Cellular Phone

LRS13011
Stacked Chip

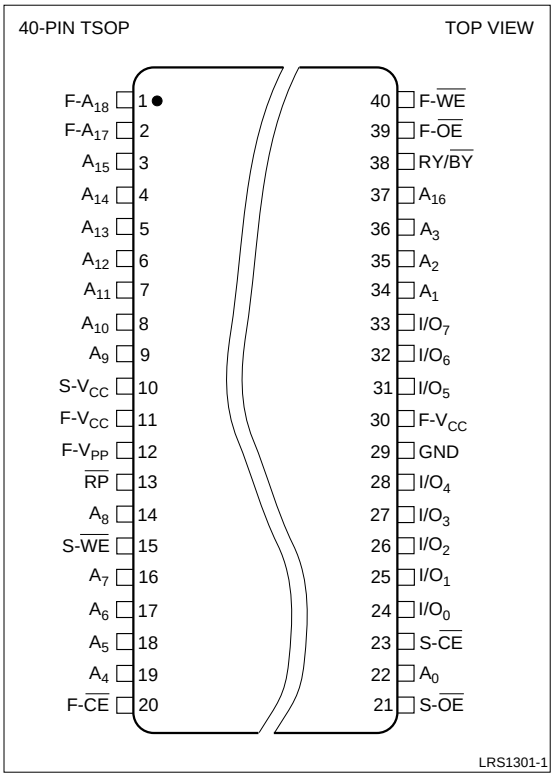
FEATURES

- 4M Flash and 1M SRAM
- Flash memory access time 150 ns MAX.
- SRAM access time 70 ns MAX.
- Operating current
  - Flash memory read 12 mA MAX. (t_{CYCLE} = 200 ns)
  - Flash byte write 40 mA MAX.
  - Flash block erase 37 mA MAX.
  - SRAM operating 25 mA MAX. (t_{CYCLE} = 200 ns)
- Standby current
  - Flash memory 10 µA MAX.
    (F-$\overline{CE}$ ≥ V_{CC} – 0.2 V, $\overline{RP}$ ≤ 0.2 V)
  - SRAM 30 µA MAX. (S-$\overline{CE}$ ≥ V_{cc} – 0.2 V)
    0.3 µA TYP. (T_A = 25°C, V_{CC} = 3 V, S-$\overline{CE}$ ≥ V_{CC} – 0.2 V)
  - Total standby current is the summation of flash memory's standby current and SRAM's standby current
- Power supply 2.7 V to 3.6 V. (Block erase, byte write and lock-bit configuration operations with V_{CC} < 3.0 V are not supported)
- SRAM data retention current 0.5 µA MAX.
  (V_{CCDR} = 3 V, T_A, = 25°C)
- Operating temperature -25°C to +85°C
- Fully static operation
- Three-state output
- Not designed or rated as radiation hardened
- 40-pin TSOP (TSOP40-P-0813) plastic package
- Flash Memory has P-type bulk silicon, and SRAM has N-type bulk silicon

DESCRIPTION

The LRS13011 is a combination memory organization as 524,288 × 8 bit flash memory and 131,072 × 8 bit static RAM in one package. It is fabricated using silicon-gate CMOS process technology.

40-PIN TSOP PINOUT



PIN DESCRIPTION

PIN	DESCRIPTION
A_0 to A_{16}	Common Address Input Pins
F-A_{17} to F-A_{18}	Address Input Pins for Flash Memory
F-$\overline{CE}$	Chip Enable Input Pin for Flash Memory
S-$\overline{CE}$	Chip Enable Input Pin for SRAM
F-$\overline{WE}$	Write Enable Input Pin for Flash Memory
S-$\overline{WE}$	Write Enable Input Pin for SRAM
F-$\overline{OE}$	Output Enable Input Pin for Flash Memory
S-$\overline{OE}$	Output Enable Input Pin for SRAM
I/O_0 to I/O_7	Common Data Input/Output Pins
$\overline{RP}$	Reset/Deep Power Down Input Pin for Flash Memory
RY/$\overline{BY}$	Ready/Busy Output Pin for Flash Memory
F-V_{CC}	Power Supply Pin for Flash Memory
F-V_{PP}	Power Supply for Flash Memory Write/Erase
S-V_{CC}	Power Supply Pin for SRAM
GND	Common GND

The information for this document is from Specification No. MFM2-J09801, issued on September 29, 1997.