

To: \_\_\_\_\_

# PRELIMINARY SPECIFICATIONS

Product Type Timing IC (350K/380K/450K pixels CCD)

Model No. LR38516

※This specifications contains 29 pages including the cover and appendix.  
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

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## CONTENTS

1. General .....	P.2
1-1. Features	
1-2. Functions	
2. Pin Assignment .....	P.3
3. Block Diagram .....	P.5
4. Pin Description .....	P.6
4-1. Pin Description	
4-2. Serial data control	
5. Electrical Characteristics .....	P.12
5-1. Absolute Maximum Ratings	
5-2. DC Characteristics	
6. Pulse Timing .....	P.13
6-1. Vertical pulse for driving CCD	
6-2. Horizontal pulse for driving CCD	
6-3. Read out pulse	
6-4. Low-speed shutter pulse	
7. Package Outline .....	P.27

## 1. General

The LR38516 is a CMOS gate array LSI. It is designed for Video-camcoder, and it generates timing pulses for driving 1/3" 350K, 380K and 450K pixels progressive Scan CCD area sensor, and synchronous pulses for TV signals and processing pulses for video signals.

### 1-1. Features

- \* The package material is plastic.
- \* A p-type silicon circuit board is used.
- \* The package type is 48-pin QFP (0.5mm pin-pitch)
- \* The process (structure) is CMOS.
- \* The delay time per 1 gate is 0.4ns.
- \* Not designed or rated as radiation hardened.

### 1-2. Functions

- \* Designed for CCD area sensor with 350,000, 380,000 or 450,000 pixels on 1/3 Format size for OFD shutter.
- \* The Frame rate is 30 Frame/sec at 350,000 and 380,000 pixels CCD, and is 25 Frame/sec at 450,000 pixels CCD,
- \* +3V, +4.5V and 5V power supply.
- \* Shutter speed can be controlled in 1H period using a serial code.
- \* To select TV mode, power save mode and the phase select of DCLK can be also controlled using a serial code.

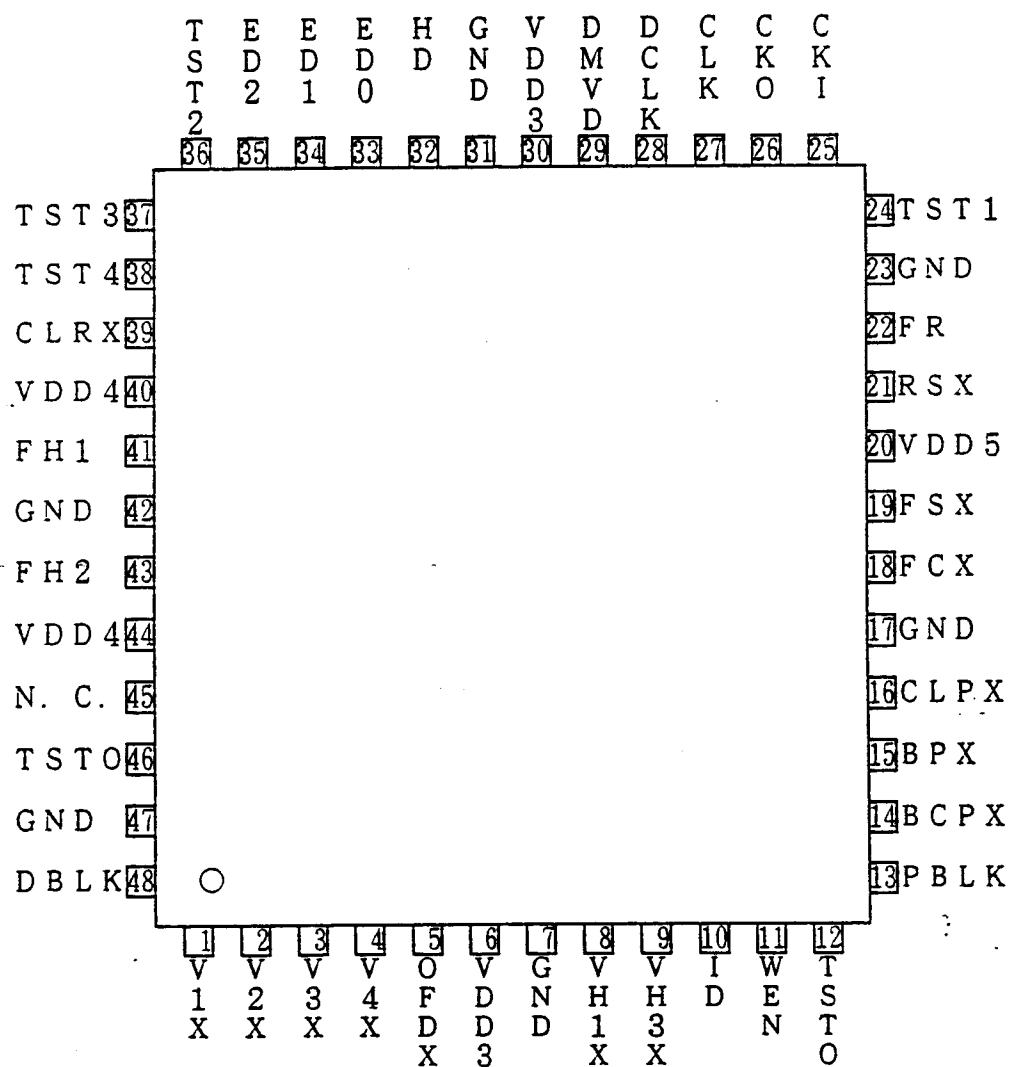
## 2. Pin Assignment

## 2-1. Table of pin assignment

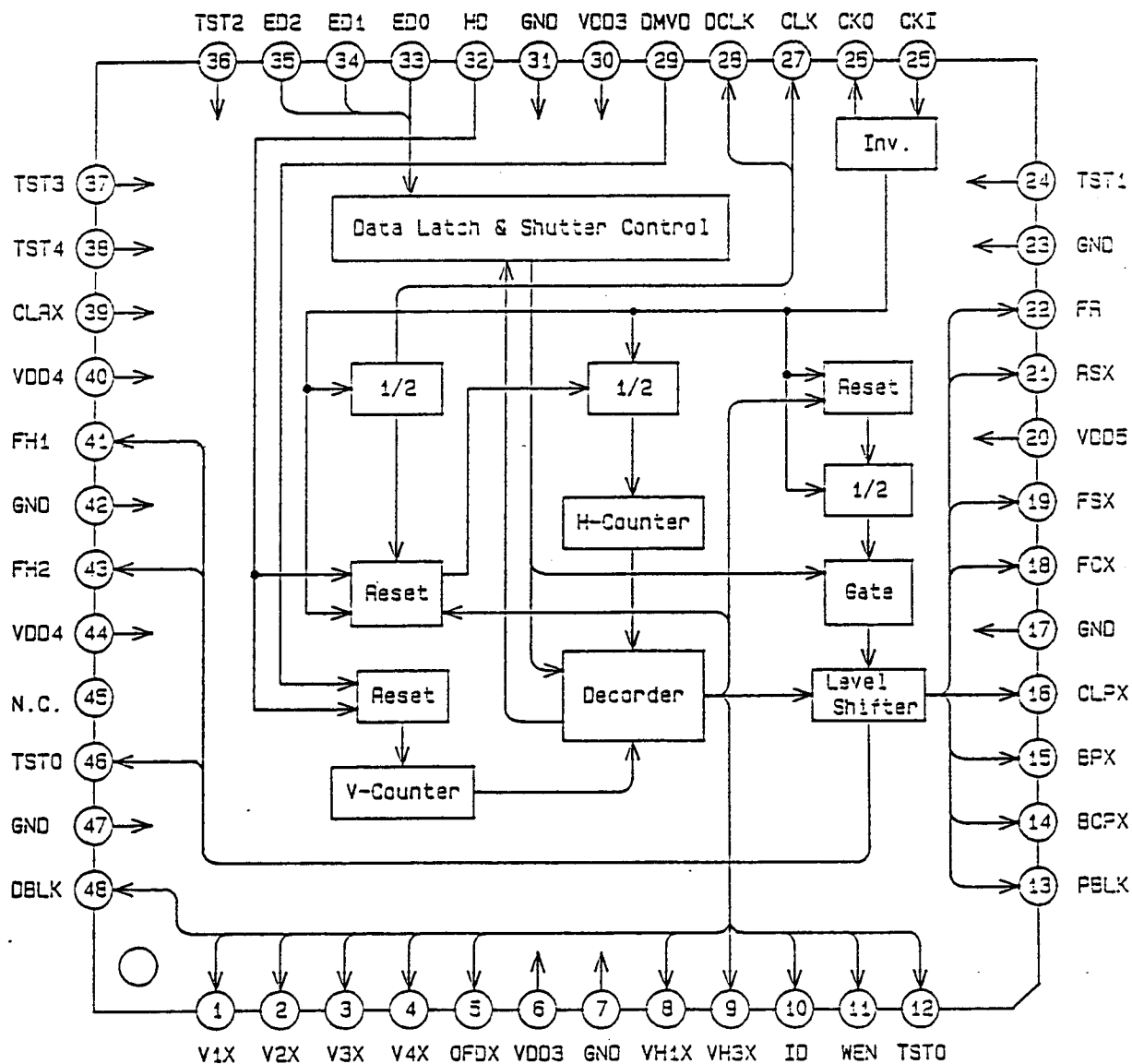
PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O3	V1X	25	OSCI3	CKI
2	O3	V2X	26	OSCO3	CKO
3	O3	V3X	27	O6MA3	CLK
4	O3	V4X	28	O6MA3	DCLK
5	O3	OFDX	29	IC3	DMVD
6	-	VDD3	30	-	VDD3
7	-	GND	31	-	GND
8	O3	VH1X	32	IC3	H D
9	O3	VH3X	33	ICD3	ED0
10	O3	I D	34	ICD3	ED1
11	O3	WEN	35	ICD3	ED2
12	O3	TSTO	36	ICD3	TST2
13	O5	PBLK	37	ICU4	TST3
14	O5	BCPX	38	ICU4	TST4
15	O5	B PX	39	ICU4	CLR X
16	O5	CLPX	40	-	VDD4
17	-	GND	41	O6MA44	FH1
18	O6MA5	FCX	42	-	GND
19	O6MA5	FSX	43	O6MA44	FH2
20	-	VDD5	44	-	VDD4
21	O6MA5	RSX	45	-	N. C.
22	O6MA52	FR	46	O6MA44	TSTO
23	-	GND	47	-	GND
24	ICD3	TST1	48	O3	DBLK

IC3	: Input (CMOS level)
ICU4	: Input (CMOS level with pull-up resister)
ICD3	: Input (CMOS level with pull-down resister)
O3	: Output
O6MA3	: Output
O6MA43	: Output
O5	: Output
O6MA5	: Output
O6MA52	: Output
OSCI3	: Input pin for oscillation
OSCO3	: Output pin for oscillation
VDD3	: +3V Power supply
VDD4	: +4.5V Power Supply
VDD5	: +5V Power supply

2-2. Figure of pin assignment



















### 3. Block Diagram












## 4. Pin Description

## 4-1. Description

No.	Symbol	I/O	Pol.	Pin Name	Description
1	V1X	03		Ver. transfer pulse 1	A vertical transfer pulse for CCD. Connect to the 1AX pin of the vertical driver IC.
2	V2X	03		Ver. transfer pulse 1	A vertical transfer pulse for CCD. Connect to the 2AX pin of the vertical driver IC.
3	V3X	03		Ver. transfer pulse 3	A vertical transfer pulse for CCD. Connect to the 3AX pin of the vertical driver IC.
4	V4X	03		Ver. transfer pulse 4	A vertical transfer pulse for CCD. Connect to the 4AX pin of the vertical driver IC.
5	OFDX	03		OFD pulse output	A pulse that sweeps the charge of the photodiode for electrical shutter. Held at H level at normal mode.
6	VDD3	-	-	Power supply	Supply +3 V power.
7	GND	-	-	Ground	A grounding pin.
8	VH1X	03		Read out pulse 1	A pulse that transfers the charge of the photodiode to the vertical shift resistor. Connect to the 1BX pin of the vertical driver IC.
9	VH3X	03		Read out pulse 2	A pulse that transfers the charge of the photodiode to the vertical shift resistor. Connect to the 3BX pin of the vertical driver IC.
10	ID	03		Line index pulse	The pulse is used in color separator. The signal switches H and L at every line. H: R color line L: B color line
11	WEN	03		Write enable output	Write enable output for low-speed shutter pulse.
12	TST0	03	-	Test output pin	A test pin. Set open in the normal
13	PBLK	05		Pre-blanking pulse output	A pulse that corresponds to the cease period of horizontal transfer pulse.
14	BCPX	05		Optical black clamp pulse	A pulse to clamp the optical black signal. Output stays Low during the absence of effective pixels within Ver. blanking.
15	BPX	05		Clamp pulse	A pulse to clamp the signal. The phase is same as as BCPX (pin 14). This pulse is continuous at Hor. cycle.
16	CLPX	05		Clamp pulse	A pulse to clamp the dummy outputs of CCD.
17	GND	-	-	Ground	A grounding pin.
18	FCX	06 MA5		CDS pulse 1	A pulse to clamp the feed-through level from CCD.
19	FSX	06 MA5		CDS pulse 2	A pulse to sample-hold the signal from CCD.
20	VDD5	-	-	Power supply	Supply +5 V power.
21	RSX	06 MA5		S/h pulse	A pulse to sample-hold the signal after CDS circuit.



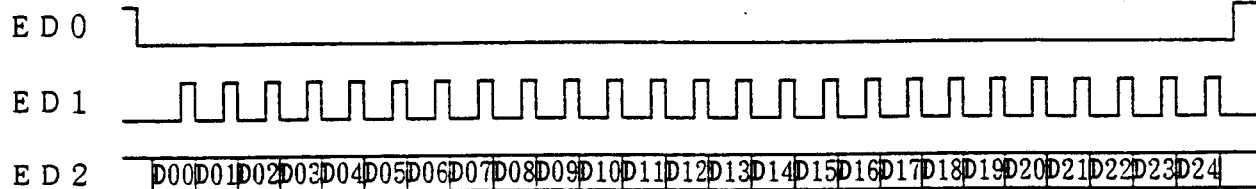
22	FR	06MA 52		Reset pulse	A reset pulse for CCD. Connect to $\phi R$ of CCD through the D.C. offset circuit.
23	GND	-	-	Ground	A grounding pin.
24	TST1	ICD3	-	Test pin 1	A test pin. Set open or to L level in the normal
25	CKI	OSCI 3		Clock input	An input pin for reference clock oscillation. The frequencies are as follows : at TST3=L in NTSC mode : 27.0MHz (1716fH) in PAL mode : 27.0MHz (1728fH) at TST3=H in NTSC mode : 24.54545MHz (1560fH) fH=Hor. frequency
26	CKO	OSCO 3	-	Clock output	An output pin for reference clock oscillation. The output is the inverse CKI (pin 37).
27	CLK	06 MA3		1/2 dividing output 1	The frequency is 1/2 dividing pulse of a reference clock CKI (pin 25). Connect to clock input terminal of SSG IC. at TST3=L in NTSC mode : 13.5MHz (858fH) in PAL mode : 13.5MHz (864fH) at TST3=H in NTSC mode : 12.27273MHz (780fH) fH=Hor. frequency
28	DCLK	06 MA3		1/2 dividing output 2	The frequency is 1/2 dividing pulse of a reference clock CKI (pin 25) as same as CLK (pin 27).. The output phase is selected by the serial data step by 90°. *1 at TST3=L in NTSC mode : 13.5MHz (858fH) in PAL mode : 13.5MHz (864fH) at TST3=H in NTSC mode : 12.27273MHz (780fH) fH=Hor. frequency
29	VD	IC3		Ver. reference input	An input pin for the Vertical reference signal. Connect to VD pin of SSG IC.
30	VDD3	-	-	Power supply	Supply +3 V power.
31	GND	-	-	Ground	A grounding pin.
32	HD	IC3		Hor. reference input	An input pin for the Horizontal reference signal. Connect to HD pin of SSG IC.
33	ED0	ICD3	-	Shutter speed control input 0	An input pin to control the shutter speed. For details, see shutter control. *1
34	ED1	ICD3	-	Shutter speed control input 1	An input pin to control the shutter speed. For details, see shutter control. *1
35	ED2	ICD3	-	Shutter speed control input 2	An input pin to control the shutter speed. For details, see shutter control. *1

36	TST2	ICD3	-	Test pin 4	A test pin. Set open or to L level in the normal
37	TST3	ICU4	-	Select input for CCD	An input pin to select CCD type. at TST3=L 380K pixels CCD (at NTSC) 450K pixels CCD (at PAL) at TST3=H 350K pixels CCD (at NTSC)
38	TST4	ICU4	-	Test pin 4	A test pin. Set open or to H level in the normal
39	CLR <sub>X</sub>	ICU4	-	Data clear input	An input pin for resetting all serial data at power on. To connect Diode with VDD4, and Capacitor with GND.
40	VDD4	-	-	Power supply	Supply +4.5 V power.
41	FH1	06MA 44		Hor. transfer pulse 1	A horizontal transfer pulse for CCD. Connect to $\phi H1$ of CCD without inverting driver.
42	GND	-	-	Ground	A grounding pin.
43	FH2	06MA 44		hor. transfer pulse 2	A horizontal transfer pulse for CCD. Connect to $\phi H2$ of CCD without inverting driver.
44	VDD4	-	-	Power supply	Supply +4.5 V power.
45	N. C.	-	-	Non connection	A pin for no use.
46	TST0	06MA 44	-	Test output pin	A test pin. Set open in the normal
47	GND	-	-	Ground	A grounding pin.
48	DBLK	03		Dummy composit	Composit blanking pulse. In NTSC mode : V:33H period In PAL mode ; V:45H period

(\*1) ; For details, see page 9~11.

## 4-2. Serial data control

## (1) Serial data inputs



The data on ED2 is latched in the register at the rising edge of ED1.  
 The data of D13 is effective. Other data is effective at next Hor. line  
 (NTSC:12H, PAL:15H) of Readout hor. line while VH1X and VH3X are active.  
 ED0 has to be stayed L level in effective data input period

## (2) Serial data

(2) Serial data						
Data	Name	Function		Data=L	Data=H	at CLRX=L
D00	S D 0	Electronic shutter speed control		See shutter speed Table		All L
D09	S D 9					
D10	SMD 0	Electronic shutter mode control		See shutter speed Table		L
D11	SMD 1					L
D12	T VMD	Select TV mode		NTSC	PAL	L
D13	PWSA-	Power save control		Normal	Power save	-
D14	D U M M Y 1	Dummy	Input to Right side data	L	-	L
D15	D U M M Y 2			L		L
D16	D U M M Y 3			H		L
D17	D U M M Y 4			L		L
D18	D U M M Y 5			H		L
D19	D U M M Y 6			H		L
D20	D U M M Y 7			H		L
D21	D U M M Y 8			H		L
D22	M L 1	DCLK phase control		See DCLK pahse control		L
D23	M L 2					L
D24	D U M M Y 9	Dummy		-	-	-

## (3) SD0~SD9, SMD0, SMD1

## (3-1) Shutter mode

D10	D11	Shutter mode	Function
SMD0	SMD1		
L	L	Shutter off	•No shutter operation.
H	H	Flickerless	•Flickerless mode •1/100(NTSC), 1/120(PAL)
H	L	High-speed shutter	•High-sped shutter:Shutter speed faster than 1/30(NTSC) 1/25(PAL)
L	H	Low-speed shutter	•High-sped shutter:Shutter speed slower than 1/30(NTSC) 1/25(PAL)

## (3-2) Shutter speed calculation formula

## • High-speed shutter

NTSC :  $T = 1 / ((n - 498) \times 63.56 + 30.8)$  [ $\mu s$ ] ( $499 \leq n \leq 1021$ )PAL :  $T = 1 / ((n - 398) \times 64.00 + 30.8)$  [ $\mu s$ ] ( $399 \leq n \leq 1021$ )

## • Low-speed shutter

NTSC :  $T = 1 / ((1023 - n) \times 33.37)$  [ms] ( $1015 \leq n \leq 1021$ )PAL :  $T = 1 / ((1023 - n) \times 40.00)$  [ms] ( $1015 \leq n \leq 1021$ )

D00	D01	D02	D03	D04	D05	D06	D07	D08	D09	D10	D11	D12	HEX	Shutter speed	Note
SD0	SD1	SD2	SD3	SD4	SD5	SD6	SD7	SD8	SD9	SMD0	SMD1	TVMD			
H	H	L	L	H	H	H	H	H	L	H	L	L	05F3	1/10.000	NTSC High speed shutter
H	L	H	L	H	H	H	H	H	L	H	L	L	05F5	1/ 4.000	
H	L	L	H	H	H	H	H	H	L	H	L	L	05F9	1/ 2.000	
H	L	L	L	L	L	L	L	L	H	H	L	L	0601	1/ 1.000	
H	L	L	L	H	L	L	L	L	H	H	L	L	0611	1/ 500	
L	L	L	L	H	H	L	L	L	H	H	L	L	0630	1/ 250	
H	H	H	H	L	H	H	L	L	H	H	L	L	066F	1/ 125	
H	H	H	H	L	L	L	H	L	H	H	L	L	068F	1/ 100	
L	L	L	H	H	H	H	H	L	H	H	L	L	06F8	1 / 60	
H	L	H	H	H	H	H	H	H	H	H	L	L	07FD	$\approx 1/30$	
H	H	H	H	L	L	L	H	H	L	H	L	H	158F	1/10.000	PAL High speed shutter
H	L	L	L	H	L	L	H	H	L	H	L	H	1591	1/ 4.000	
H	L	H	L	H	L	L	H	H	L	H	L	H	1595	1/ 2.000	
H	L	H	H	H	L	L	H	H	L	H	L	H	159D	1/ 1.000	
H	L	H	H	L	H	L	H	H	L	H	L	H	15AD	1/ 500	
L	L	H	H	L	L	H	H	H	L	H	L	H	15CC	1/ 250	
L	H	L	H	L	L	L	L	L	H	H	L	H	160A	1/ 125	
L	L	L	L	H	L	L	L	L	H	H	L	H	1610	1/ 120	
L	H	H	L	L	L	H	H	L	H	H	L	H	16C6	1/ 50	
H	L	H	H	H	H	H	H	H	H	H	L	H	17FD	$\approx 1/25$	
H	L	H	H	H	H	H	H	H	H	L	H	×	BFD	2 Frame	Low speed shutter
L	L	H	H	H	H	H	H	H	H	L	H	×	BFC	3 Frame	
H	H	L	H	H	H	H	H	H	H	L	H	×	BFB	4 Frame	
L	H	L	H	H	H	H	H	H	H	L	H	×	BFA	5 Frame	
H	L	L	H	H	H	H	H	H	H	L	H	×	BF9	6 Frame	
L	L	L	H	H	H	H	H	H	H	L	H	×	BF8	7 Frame	
H	H	H	L	H	H	H	H	H	H	L	H	×	BF7	8 Frame	
×	×	×	×	×	×	×	×	×	×	H	H	L	-	1/ 100	Flicker- less
×	×	×	×	×	×	×	×	×	×	H	H	H	-	1/ 120	
×	×	×	×	×	×	×	×	×	×	L	L	L	-	1/ 30	Shutter OFF
×	×	×	×	×	×	×	×	×	×	L	L	H	-	1/ 25	

## (4) PWSA

H level input : Power save ON.

No operatin input : HD, DMVD

Operating output : CKO, CLK, DCLK

No operating output : Stay L level

L level input : Normal operation

## (5) ML1, ML2

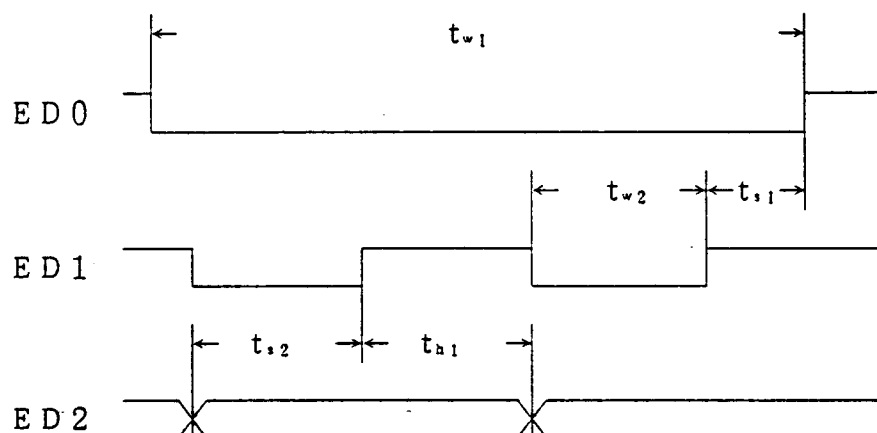
The phase difference of FH1

ML1 [D22]	L	H	L	H
ML2 [D23]	L	L	H	H
Phase diff.	0°	90°	180°	270°

## (6) タミ一項目

Inputs of the data [D14], [D15], [D17] are L level, and  
inputs of the data [D16], [D18], [D19], [D20], [D21] are H level.

## (7) Input characteristic of serial data



記号	適用	最小値	最大値
$t_{w1}$	ED0 pulse width	*	—
$t_{w2}$	ED1 pulse width	20ns	—
$t_{s1}$	ED1 rising setup time against the rising edge of ED0	20ns	—
$t_{s2}$	ED2 rising setup time against the rising edge of ED1	20ns	—
$t_{h1}$	ED2 hold time against the rising edge of ED1	20ns	—

\*  $t_{w1}$ ; Input period of effective data of ED1, ED2.

## 5. Electorical Characteristics

## 5-1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	
Supply voltage	$V_{DD3}, V_{DD4}, V_{DD5}$	-0.3 ~ 6.0	V	
Input voltage	$V_{I3}$	-0.3 ~ $V_{DD3} + 0.3$	V	
	$V_{I4}$	-0.3 ~ $V_{DD4} + 0.3$	V	
Output voltage	$V_{O3}$	-0.3 ~ $V_{DD3} + 0.3$	V	
	$V_{O4}$	-0.3 ~ $V_{DD4} + 0.3$	V	
	$V_{O5}$	-0.3 ~ $V_{DD5} + 0.3$	V	
Operation temperature	$T_{opr}$	-20 ~ +70	°C	
Storage temperature	$T_{stg}$	-55 ~ +150	°C	

## 5-2. DC Characteristics

( $V_{DD3}=3.0V\pm10\%$ ,  $V_{DD4}=4.5V\pm10\%$ ,  $V_{DD5}=5V\pm10\%$ ,  $T_{opr}=-20\sim+70^{\circ}C$ )

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Note
Input "Low" voltage	$V_{IL3}$				$0.2 \times V_{DD3}$	V	1
Input "High" voltage	$V_{IH3}$		$0.8 \times V_{DD3}$			V	
Input "Low" voltage	$V_{IL4}$				$0.2 \times V_{DD4}$	V	2
Input "High" voltage	$V_{IH4}$		$0.8 \times V_{DD4}$			V	
Input "High" current	$ I_{IH3-1} $	$V_I = V_{DD3}$			1.0	$\mu A$	1
Input "Low" current	$ I_{IL3-1} $	$V_I = 0V$			1.0	$\mu A$	
Input "High" current	$ I_{IH3-2} $	$V_I = V_{DD3}$	2.0		30	$\mu A$	2
Input "Low" current	$ I_{IL3-2} $	$V_I = 0V$			1.0	$\mu A$	
Input "High" current	$ I_{IH4-1} $	$V_I = V_{DD4}$			2.0	$\mu A$	3
Input "Low" current	$ I_{IL4-1} $	$V_I = 0V$	4.0		60	$\mu A$	
Output "High" voltage	$V_{OH3-1}$	$I_{OH} = -2mA$	$V_{DD3}-0.5$			V	4
Output "Low" voltage	$V_{OL3-1}$	$I_{OL} = 2mA$			0.4	V	
Output "High" voltage	$V_{OH3-2}$	$I_{OH} = -1mA$	$V_{DD3}-0.5$			V	5
Output "Low" voltage	$V_{OL3-2}$	$I_{OL} = 2mA$			0.4	V	
Output "High" voltage	$V_{OH3-3}$	$I_{OH} = -3mA$	$V_{DD3}-0.5$			V	6
Output "Low" voltage	$V_{OL3-3}$	$I_{OL} = 3mA$			0.4	V	
Output "High" voltage	$V_{OH4}$	$I_{OH} = -12mA$	$V_{DD4}-0.5$			V	7
Output "Low" voltage	$V_{OL4}$	$I_{OL} = 12mA$			0.4	V	
Output "High" voltage	$V_{OH5-1}$	$I_{OH} = -2mA$	$V_{DD5}-0.5$			V	8
Output "Low" voltage	$V_{OL5-1}$	$I_{OL} = 4mA$			0.4	V	
Output "High" voltage	$V_{OH5-2}$	$I_{OH} = -6mA$	$V_{DD5}-0.5$			V	9
Output "Low" voltage	$V_{OL5-2}$	$I_{OL} = 6mA$			0.4	V	
Output "High" voltage	$V_{OH5-3}$	$I_{OH} = -12mA$	$V_{DD5}-0.5$			V	10
Output "Low" voltage	$V_{OL5-3}$	$I_{OL} = 12mA$			0.4	V	

Note 1 : Applied to Inputs(IC3, OSCI3).

Note 2 : Applied to Input(ICD3).

Note 3 : Applied to Input(ICU4).

Note 4 : Applied to Output(OSC03).

(Output(OSC03) measures on conditions that input(OSCI3) level is 0V or  $V_{DD3}$ .)

Note 5 : Applied to Output(O3).

Note 6 : Applied to Output(O6MA3).

Note 7 : Applied to Output(O6MA55).

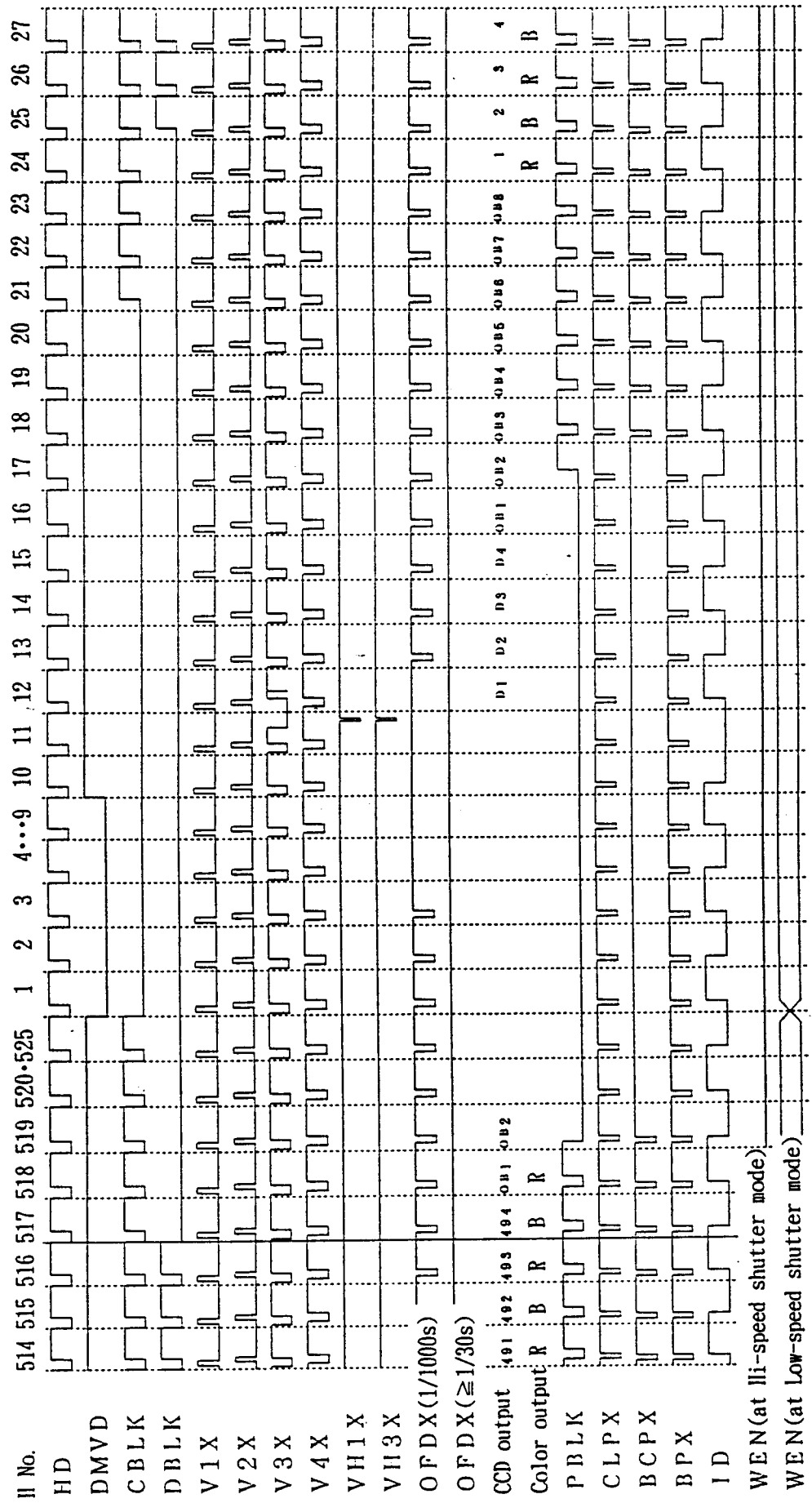
Note 8 : Applied to Output(O5).

Note 9 : Applied to Output(O6MA5).

Note 10 : Applied to Output(O6MA52).

### 6-1. Vertical pulse for driving CCD

1/30s Non-interlace 380K(724II), 350K(659II)

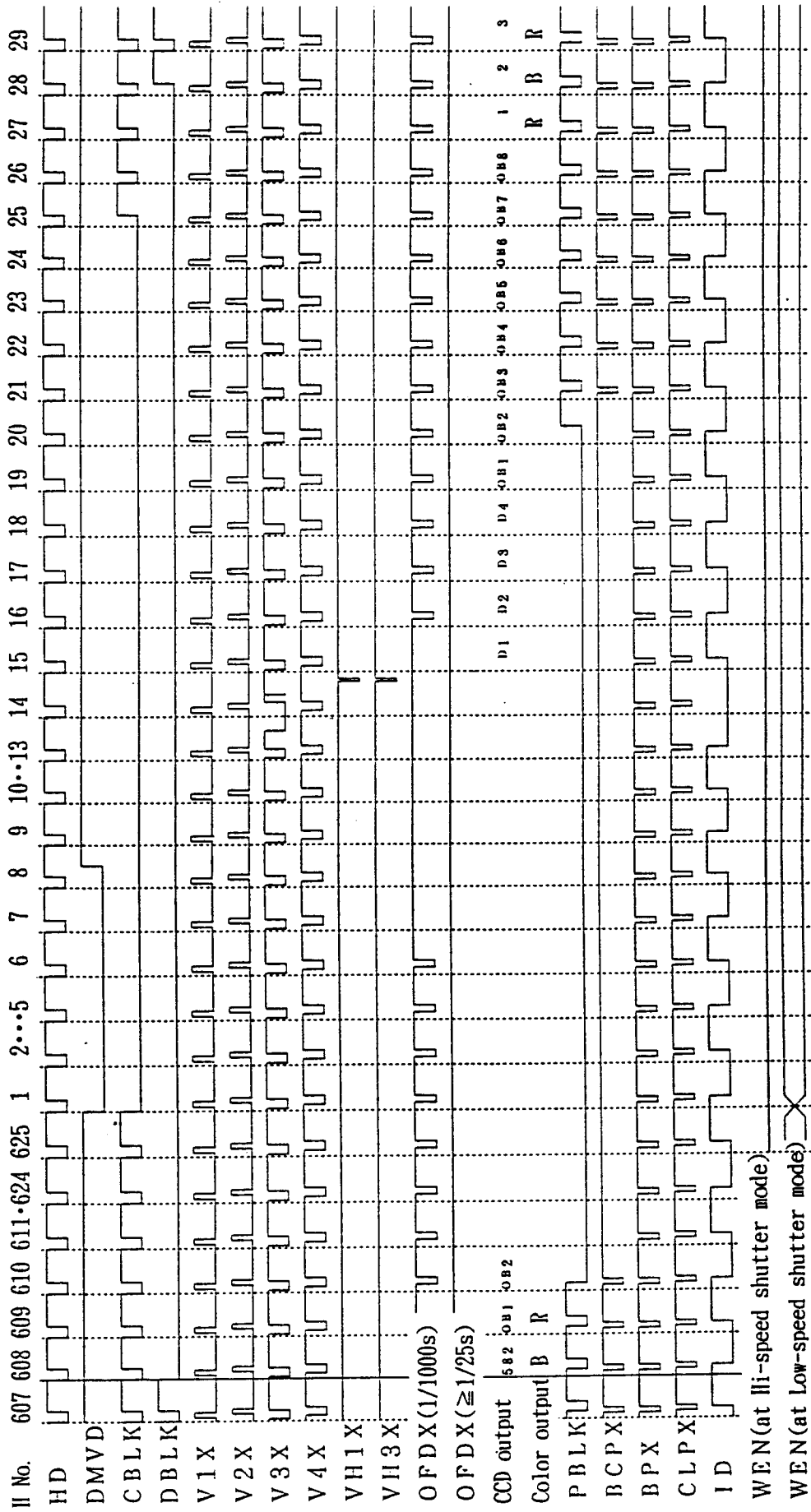


W E N (at lli-speed shutter mode)

WEN (at Low-speed shutter mode) :

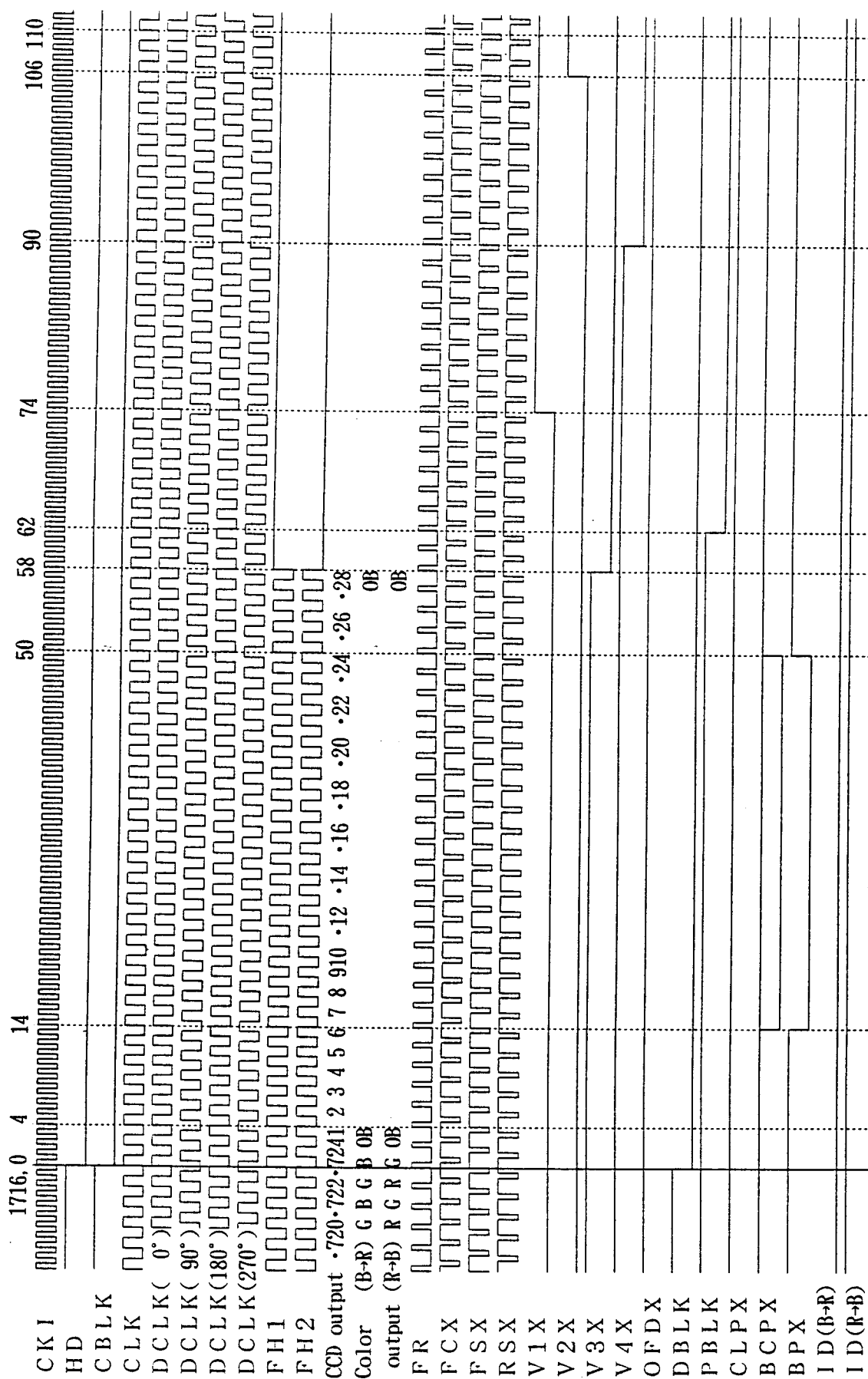
## Vertical pulse for driving CCD - 2

1/25s Non-interlace 450K(724H)

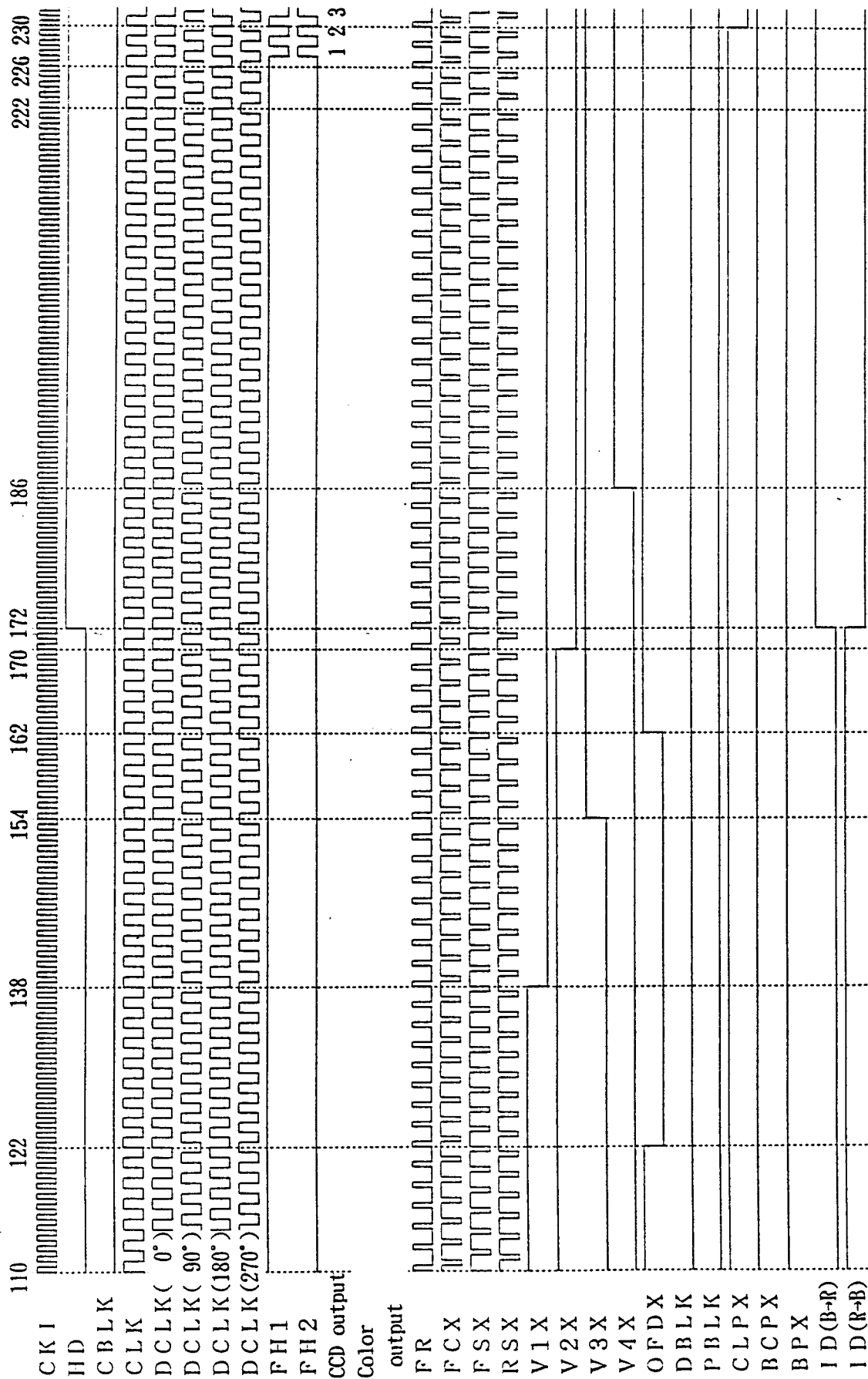




6-2. Horizontal pulse for driving CCD - 1  
380K(724H) 1/30s Non-interlace - 1

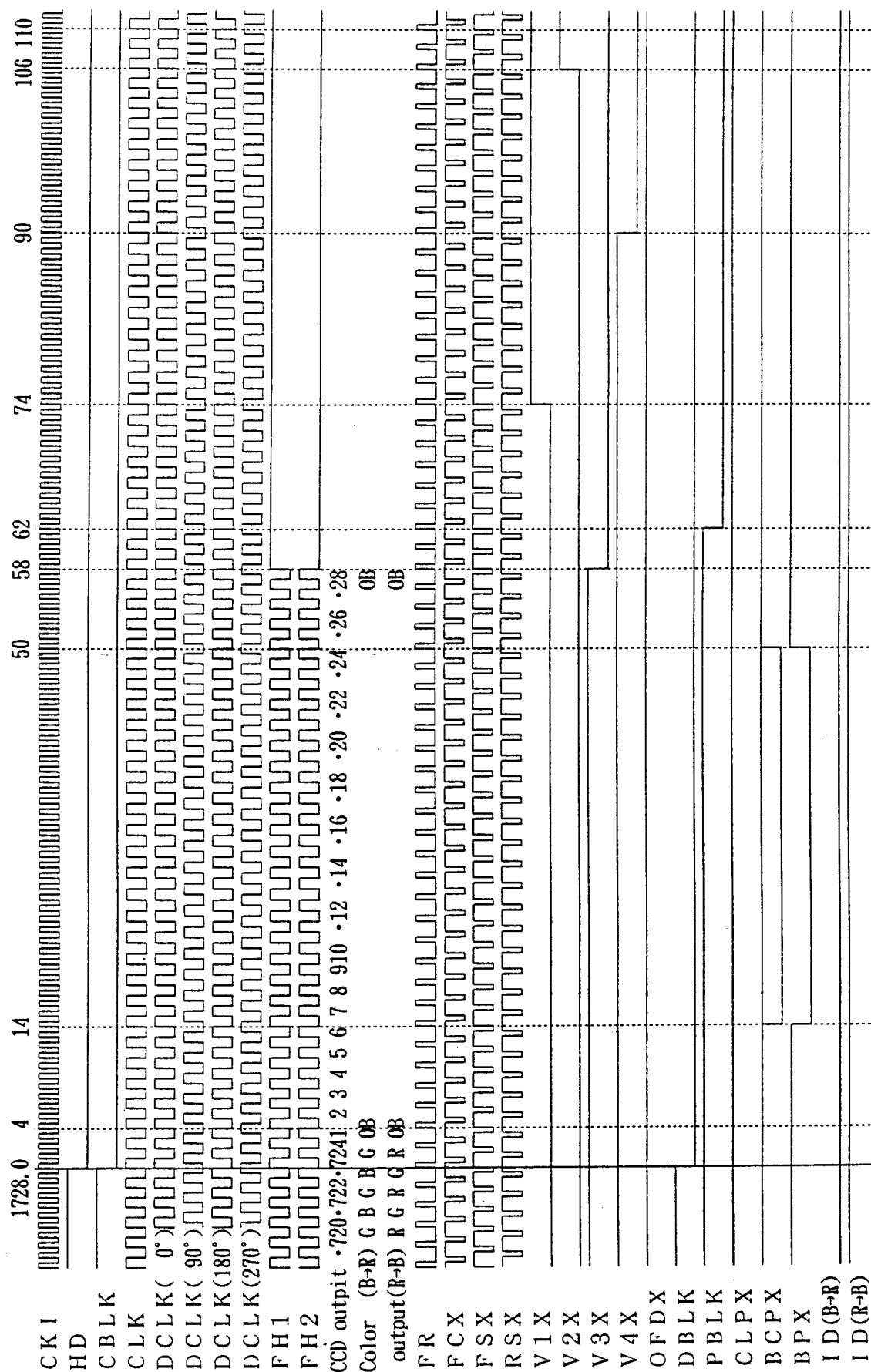


Horizontal pulse for driving CCD - 2  
380K(724H) 1/30s Non-interlace - 2

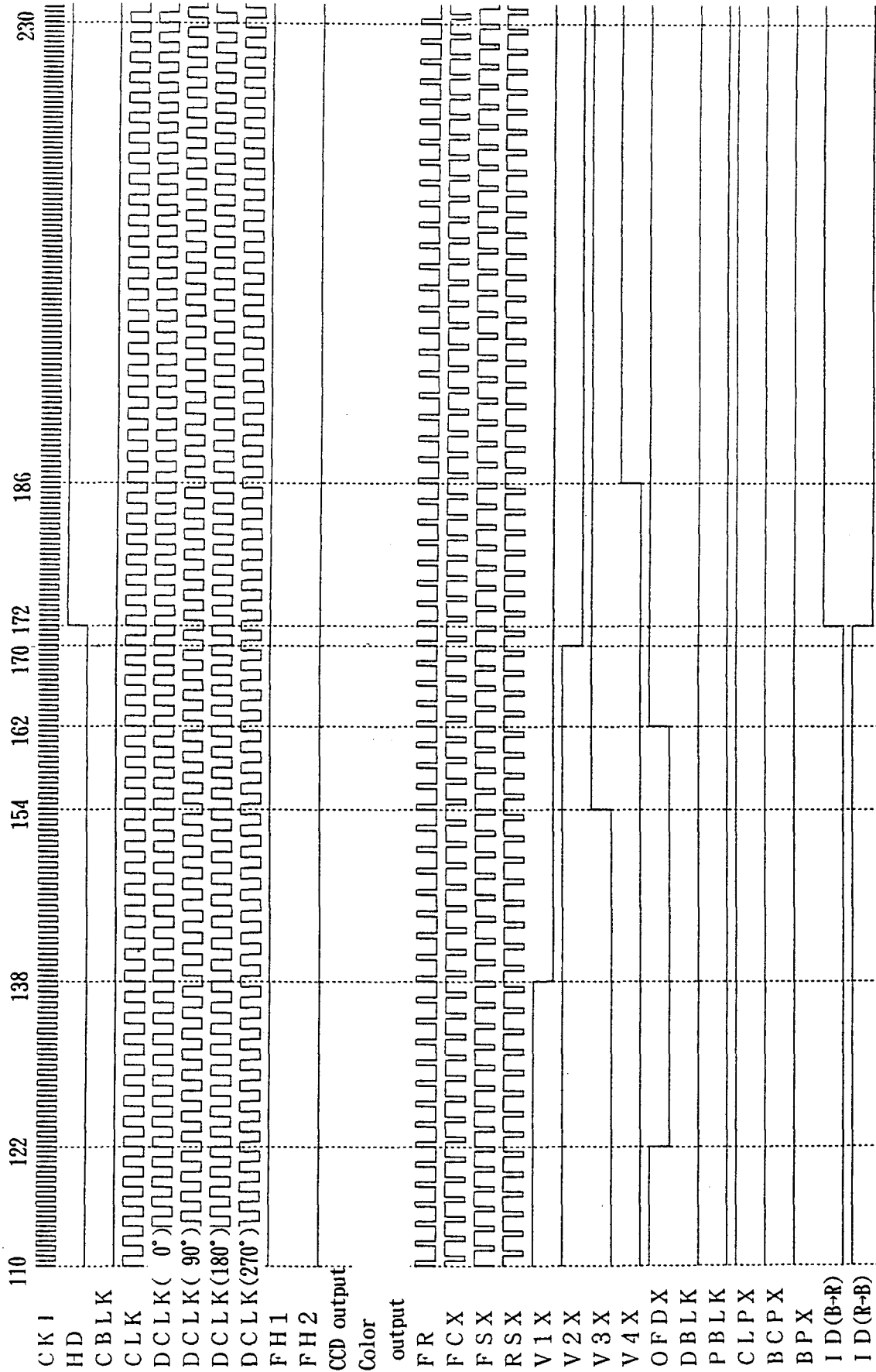




Horizontal pulse for driving CCD -- 4  
450K(724H) 1/25s Non-interlace - 1

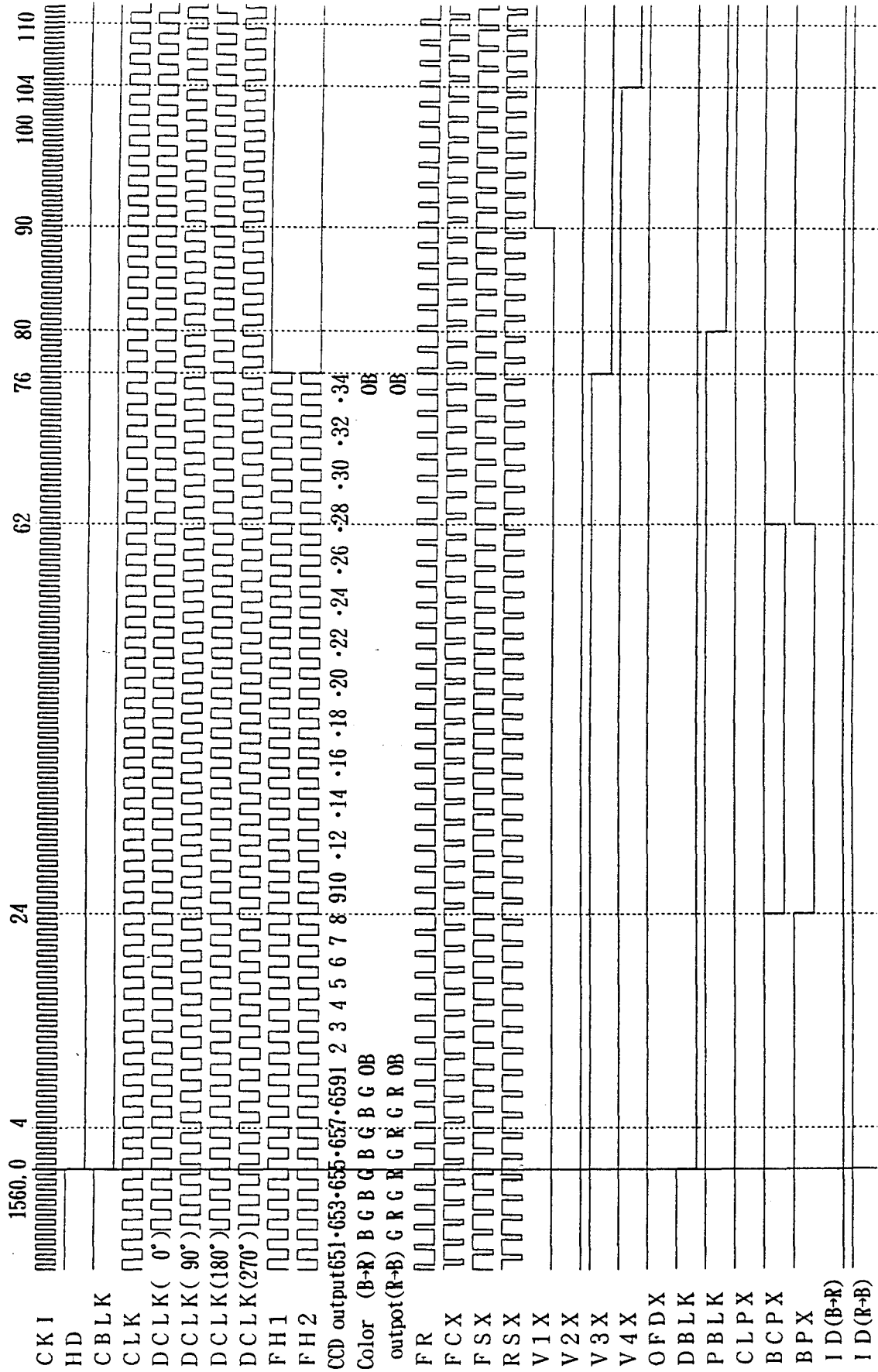


Horizontal pulse for driving CCD - 5  
450K(724H) 1/25s Non-interlace - 2

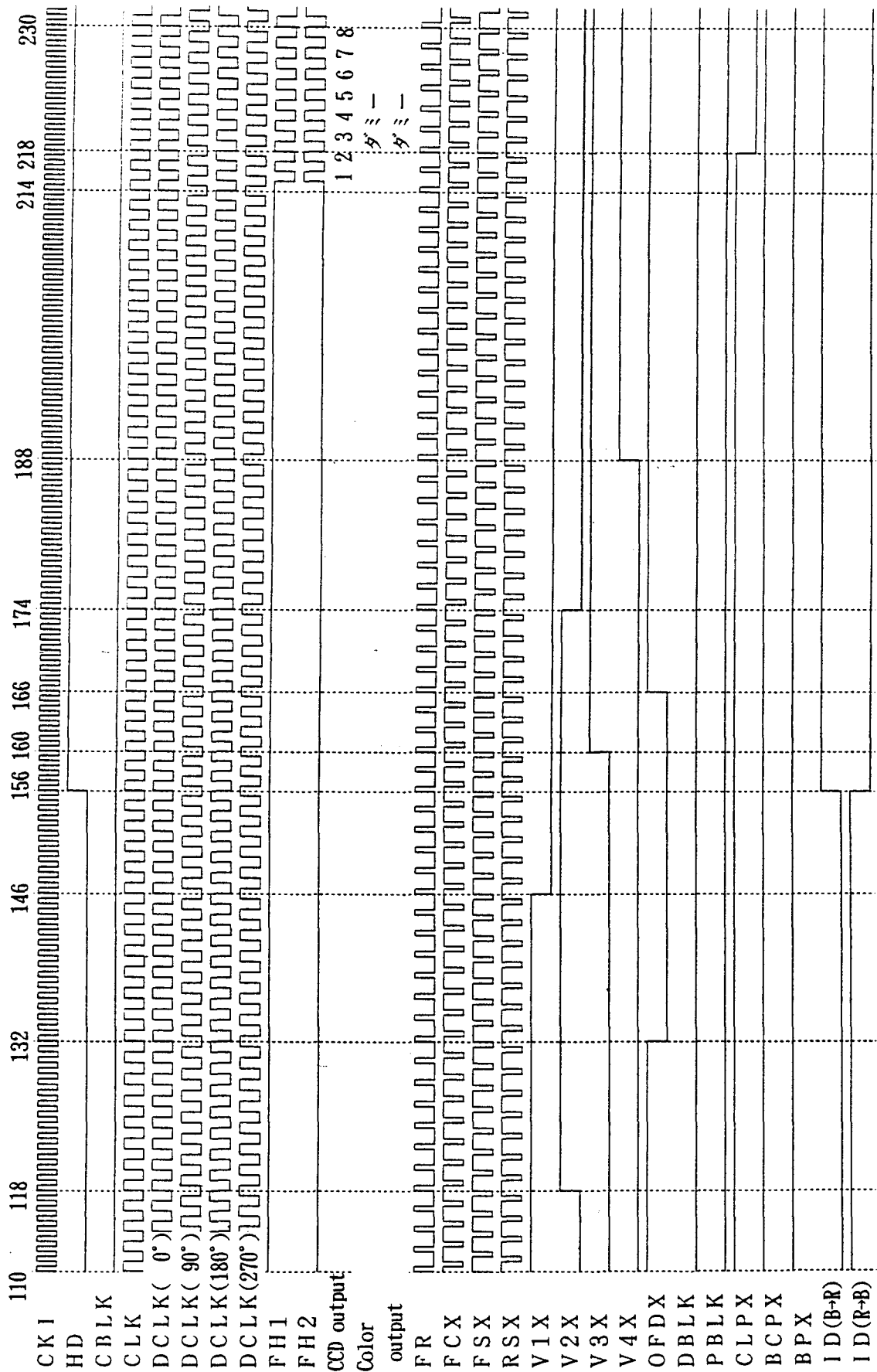


[illegible]

Horizontal pulse for driving CCD - 7  
350K(659H) 1/30s Non-interlace - 1

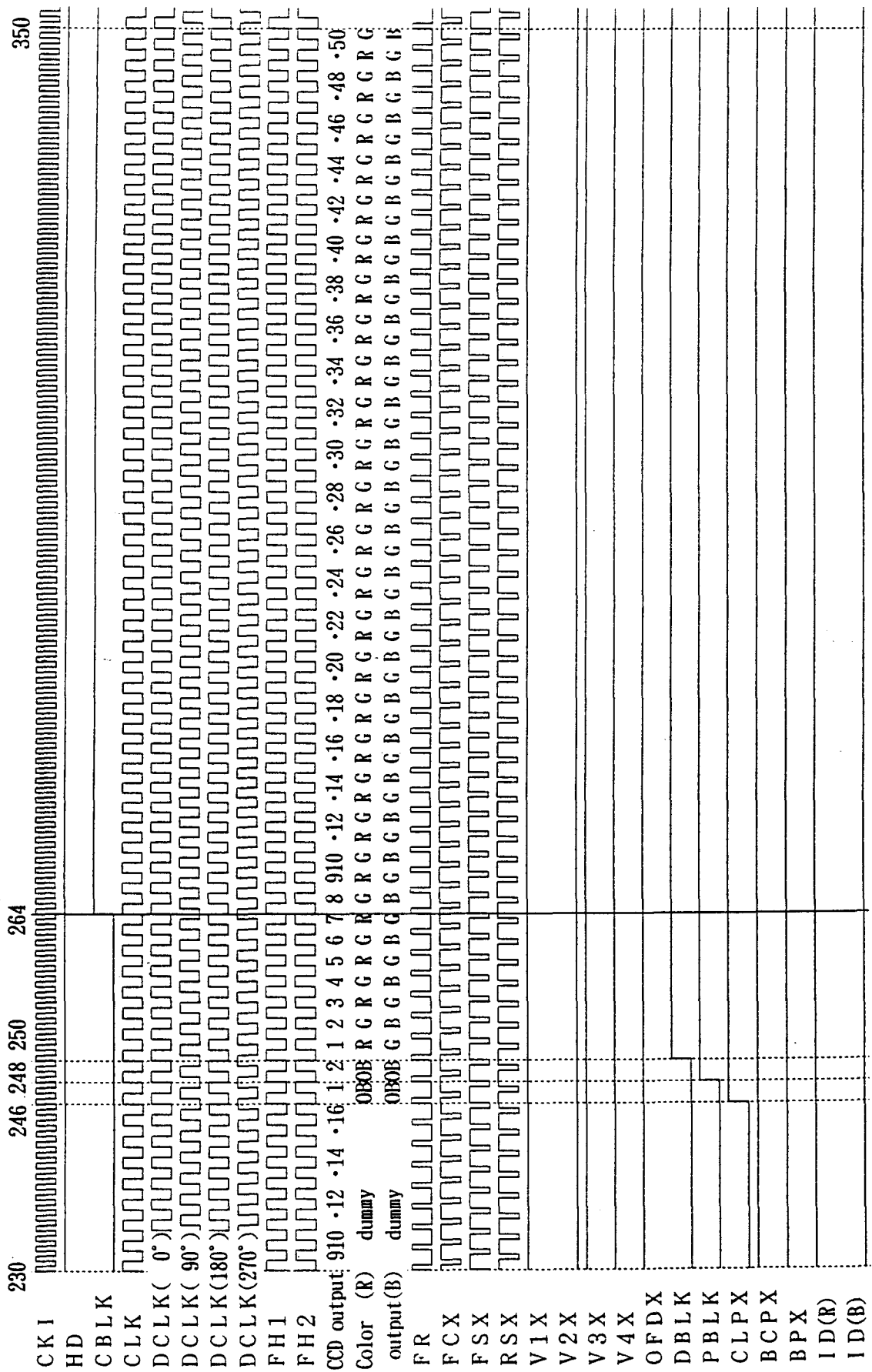


Horizontal pulse for driving CCD - 8  
350K(659H) 1/30s Non-interlace - 2



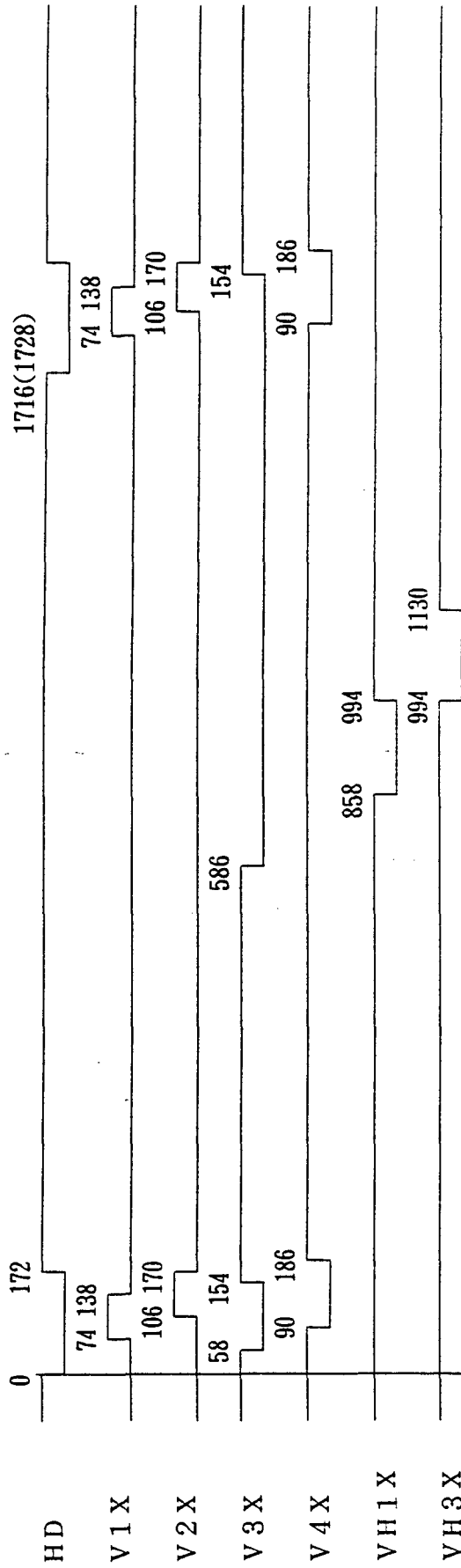


Horizontal pulse for driving CCD - 9  
350K(659H) 1/30s Non-interlace - 3



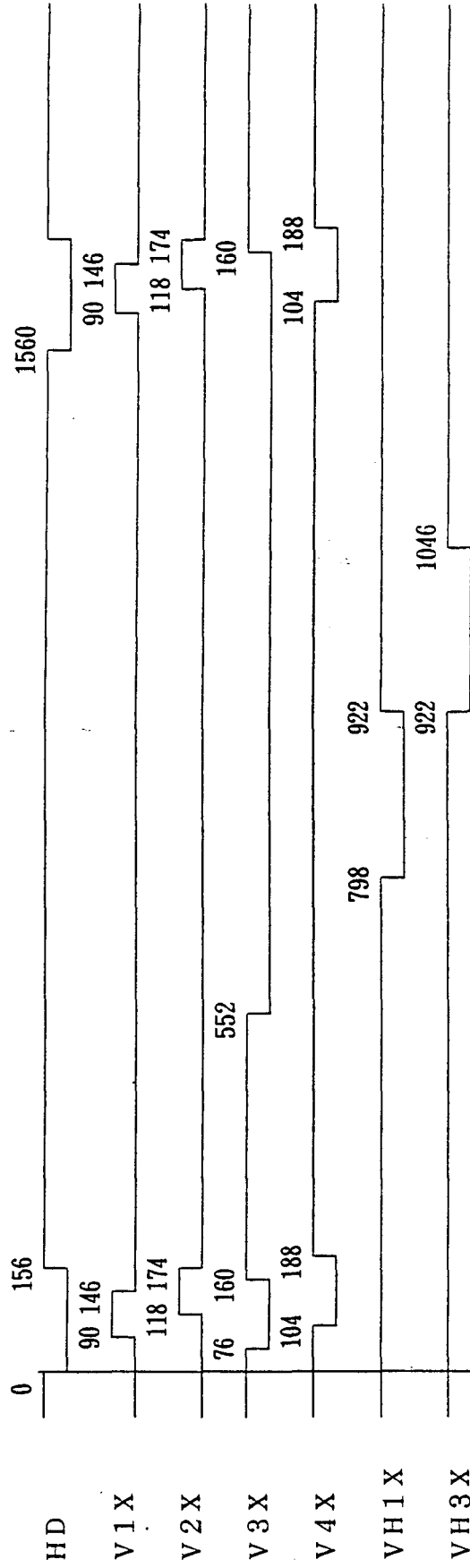
## 6-3. Read out pulse - 1

380K(724H) 1/30s Non-interlace, 450K(724H) 1/25s Non-interlace ( ) ; P A L

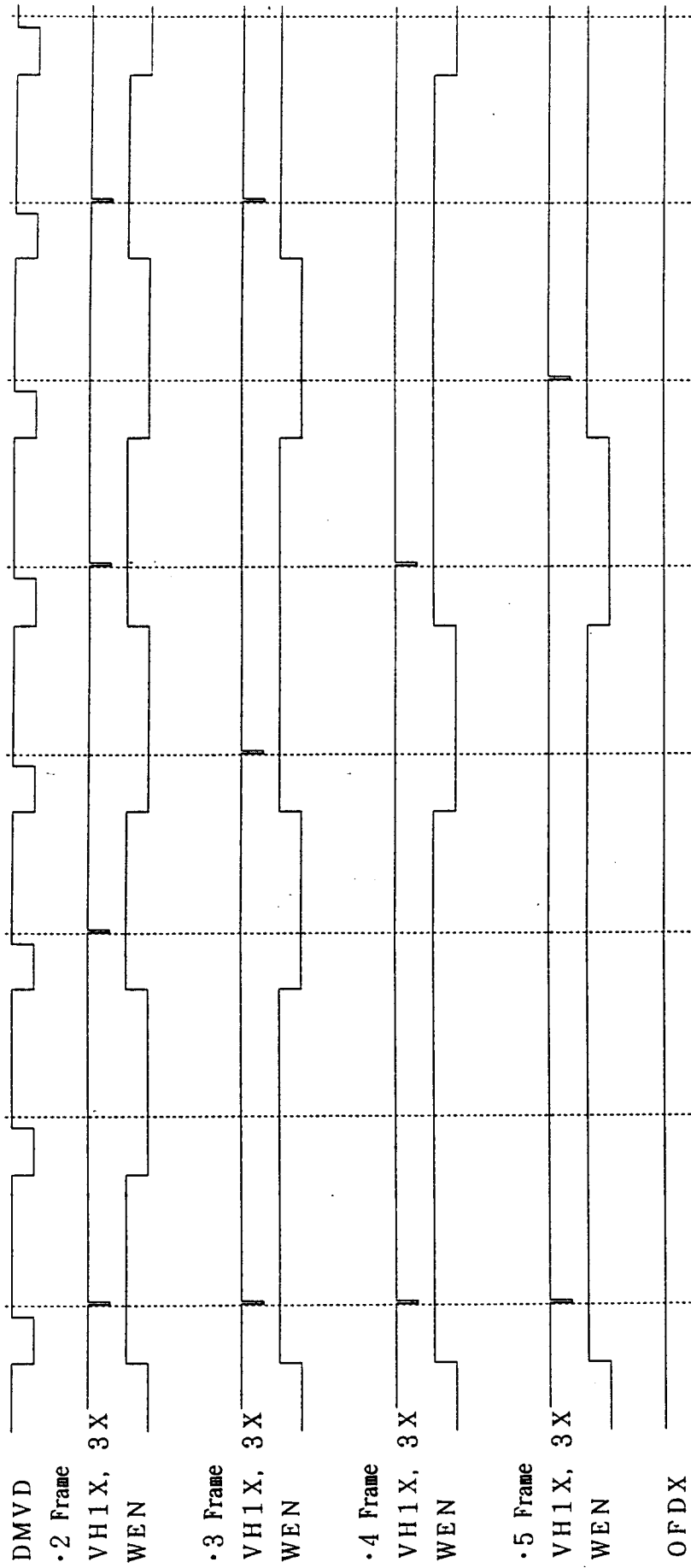


Read out pulse - 2

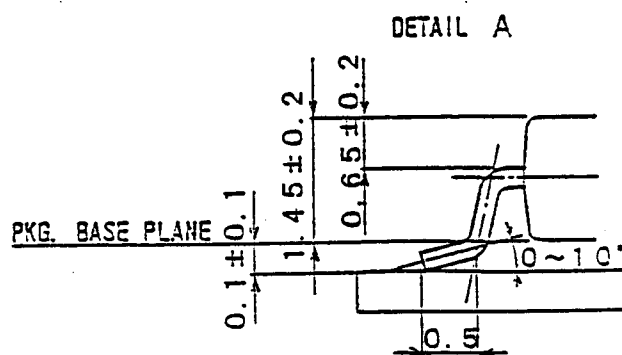
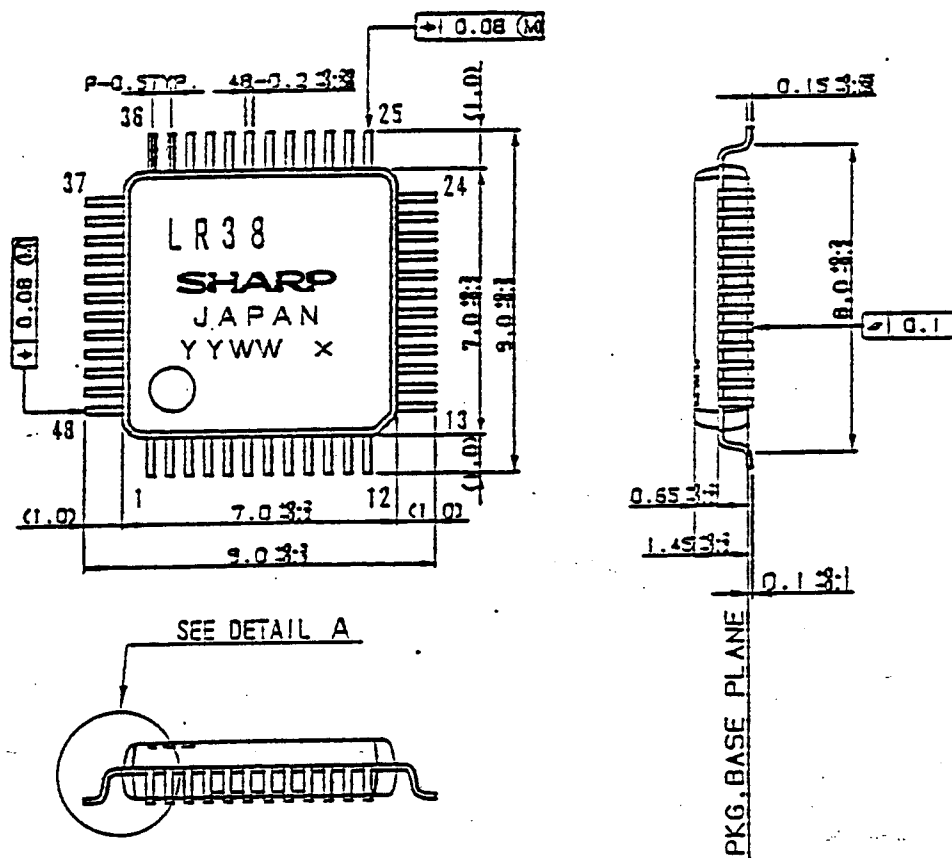
350K(659H) 1/30s Non-interlace



6-4. Low-speed shutter pulse



## 7. Package Outline



名称	リード仕上	TIN-LEAD	備考	プラスチックパッケージ材は、バリの含まないものとする。
NAME	QFP48-P-0707	LEAD FINISH	PLATING	NOTE Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1035	単位	mm	
		UNIT		

CCD sensor imaging area sensor pattern recognition timing generator vertical driver white balance