SHARP

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To ;

SPECIFICATIONS

Product Type Timing IC (270K/320K/410K/470K pixels CCD)

Model No. LR38278

※This specifications contains 42 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED
BY:
Y. KUSANO
Dept. General Manager

REVIEWED BY: A-Tokuno

PREPARED BY: F. Inoue

Engineering Dept. 3
Logic IC Engineering Center
Tenri Integrated Circuits Group
SHARP CORPORATION

LR38278

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  (1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
  - ·Office electronics
  - ·Instrumentation and measuring equipment
  - ·Machine tools
  - ·Audiovisual equipment
  - ·Home appliances
  - ·Communication equipment other than for trunk lines

  (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
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  - ·Traffic control systems
  - ·Gas leak detectors and automatic cutoff devices
  - ·Rescue and security equipment
  - ·Other safety devices and safety equipment, etc.

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  - ·Communications equipment for trunk lines
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  - ·Medical equipment related to life support, etc.

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- Please direct all queries regarding the products covered herein to a sales representative of the company.

LR38278

CONTENTS

1. General

The LR38278 is a CMOS gate array LSI. It generates timing pulses for drivinga CCD area sensor, and signals and processing pulses for video signals.

1-1. Features

* The package material is plastic.
* A p-type silicon circuit board is used.
* The package type is 48-pin QFP (0.5mm pin-pich)
* The process (structure) is CMOS.
* The delay time per 1 gate is 0.4ns.
* Not designed or rated as radiation hardened.

1-2. Functions

* Designed for 4-Voltage Power Supply CCD color area sensor with 270,000 or 320,000 pixels or 410,000 or 470,000 pixels .
* Switchable between NTSC and PAL mode.
* +3.3V and +5V power supply.
* External shutter control function with serial data input is possible.

2. Pin Assignment

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	IC3	SFC1	25	OSCI3	CKI
2	IC3	SFC2	26	OSCO3	CKO
3	O6MA32	MCK2	27	ICD3	TST2
4	O6MA32	MCK3	28	O6MA32	SGCK
5	IC3	SFS1	29	O6MA32	CDCK
6	IC3	SFS2	30	–	VDD3
7	–	GND	31	–	GND
8	–	VDD3	32	O6MA32	ADCK
9	ICD3	ED2	33	IC3	VD
10	ICD3	ED0	34	IC3	HP
11	ICD3	ED1	35	ICU3	SAD1
12	ICU5	SCCD	36	ICU5	SAD2
13	O5	V1X	37	O5	PBLK
14	O5	V2X	38	O6MA5	FS
15	O5	V3X	39	O6MA5	FCDS
16	O5	V4X	40	ICU5	TVMD
17	O5	OFDX	41	–	N.C.
18	–	VDD5	42	–	VDD5
19	–	GND	43	–	GND
20	O5	VH1X	44	O6MA52	FH1
21	O5	VH3X	45	–	VDD5
22	ICD5	TST1	46	O6MA52	FH2
23	O6MA52	FR	47	–	N.C.
24	–	N.C.	48	ICD5	TST3

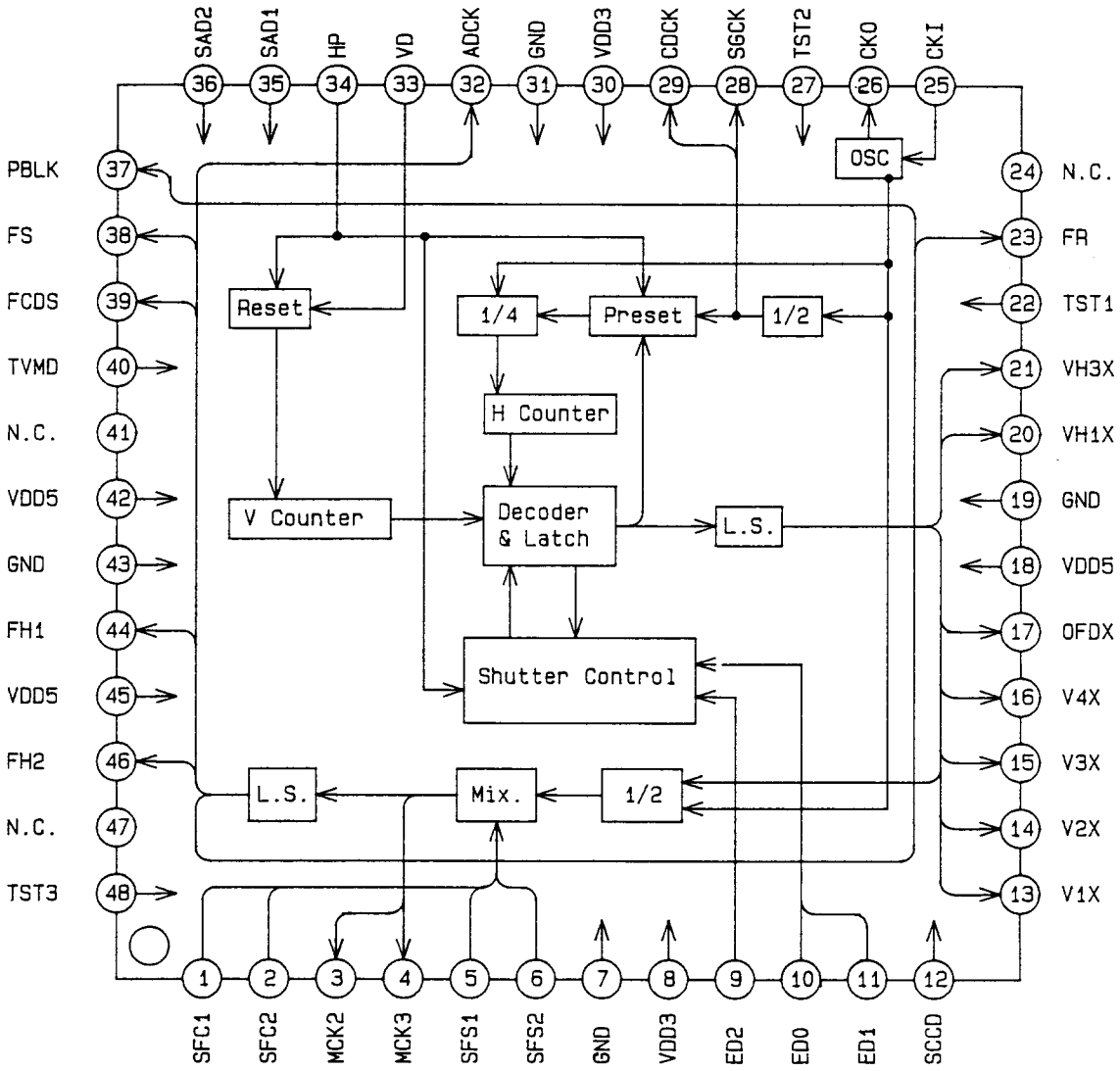
IC3 : Input (CMOS level)
ICU3 : Input (CMOS level with pull-up resister)
ICD3 : Input (CMOS level with pull-down resister)
ICU5 : Input (CMOS level with pull-up resister)
ICD5 : Input (CMOS level with pull-down resister)
O5 : Output
O6MA5 : Output
O6MA52 : Output
O6MA32 : Output
OSCI3 : Input pin for oscillation
OSCO3 : Output pin for oscillation

2. Pin Assignment

PIN NO.	I／O	SIGNAL	PIN NO.	I／O	SIGNAL
1	IC3	SFC1	25	OSCI3	CKI
2	IC3	SFC2	26	OSCO3	CKO
3	O6MA32	MCK2	27	ICD3	TST2
4	O6MA32	MCK3	28	O6MA32	SGCK
5	IC3	SFS1	29	O6MA32	CDCK
6	IC3	SFS2	30	−	VDD3
7	−	GND	31	−	GND
8	−	VDD3	32	O6MA32	ADCK
9	ICD3	ED2	33	IC3	VD
10	ICD3	ED0	34	IC3	HP
11	ICD3	ED1	35	ICU3	SAD1
12	ICU5	SCCD	36	ICU5	SAD2
13	O5	V1X	37	O5	PBLK
14	O5	V2X	38	O6MA5	FS
15	O5	V3X	39	O6MA5	FCDS
16	O5	V4X	40	ICU5	TVMD
17	O5	OFDX	41	−	N.C.
18	−	VDD5	42	−	VDD5
19	−	GND	43	−	GND
20	O5	VH1X	44	O6MA52	FH1
21	O5	VH3X	45	−	VDD5
22	ICD5	TST1	46	O6MA52	FH2
23	O6MA52	FR	47	−	N.C.
24	−	N.C.	48	ICD3	TST3

IC3 : Input (CMOS level)
ICU3 : Input (CMOS level with pull-up resister)
ICD3 : Input (CMOS level with pull-down resister)
ICU5 : Input (CMOS level with pull-up resister)
ICD5 : Input (CMOS level with pull-down resister)
O5 : Output
O6MA5 : Output
O6MA52 : Output
O6MA32 : Output
OSCI3 : Input pin for oscillation
OSCO3 : Output pin for oscillation

3. Block Diagram



4. Pin Description

No.	Symbol	I/O	Pol.	Pin Name	Description
1	SFC1	IC3	–	FCDS phase control input 1	An input pin to set the rising edge of FCDS(pin38) pulse output. It inputs the signal from MCK2(pin3) output through the RC integral circuit.
2	SFC2	IC3	–	FCDS phase control input 2	An input pin to set the falling phase of FCDS(pin 38) pulse output. It inputs the signal from MCK3(pin4) output through the RC integral circuit.
4	MCK2	06MA 32	⎍	Clock output 2	A pin to output 1/2 dividing pulse of reference clock CKI(pin 25). It is the same phase with FH1 (pin 44).
5	MCK3	06MA 32	⎍	Clock output 3	A pin to output 1/2 dividing pulse of reference clock CKI(pin 25). It is delayed by approximately 90° in phase with respect MCK2(pin 3).
5	SFS1	IC3	–	FS phase control input 1	An input pin to set the rising edge of FS(pin 39) pulse output. It inputs the signal from MCK2(pin 4) output through the RC integral circuit.
6	SFS2	IC3	–	FS phase control input 2	An input pin to set the falling edge of FS(pin 39) pulse output. It inputs the signal from MCK3(pin 5) output through the RC integral circuit.
7	GND	-	–	Ground	A grounding pin.
8	VDD3	-	–	Power supply	Supply +3 V power.
9	ED2	ICD3	–	Strobe pulse input	An input pin for the strobe pulse to control the shutter speed. For details, see shutter control.
10	ED0	ICD3	–	Sift register Clock input	An input pin for the clock of shift register to control the shutter speed. For details, see shutter control.
11	ED1	ICD3	–	Serial Shutter Data input	An input pin for the data of serial shutter code to control the shutter speed. For details, see shutter control.
12	SCCD	ICU3	–	CCD select input	An input pin to select CCD. H level or open ;410K, 470K pixels CCD L Level ;270K, 320K pixels CCD
13	V1X	05	⎍	Ver. transfer pulse output #1	A vertical transfer pulse for CCD. Connect to the 1AX pin of vertical driver IC.
14	V2X	05	⎍	Ver. transfer pulse output #1	A vertical transfer pulse for CCD. Connect to the 2AX pin of vertical driver IC.
15	V3X	05	⎍	Ver. transfer pulse output #3	A vertical transfer pulse for CCD. Connect to the 3AX pin of verical driver IC.
16	V4X	05	⎍	Ver. transfer pulse output #4	A vertical transfer pulse for CCD. Connect to the 4AX pin of vertical driver IC.

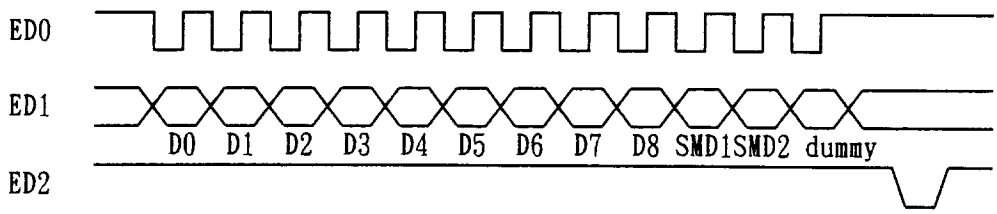
No.	Symbol	I/O	Pol.	Pin Name	Description
17	OFDX	O5	⊓	Electronic shutter pulse output 1	A pulse that sweeps the charge of the photodiode for electrical shutter. Connect to OFD of CCD through the invert, level shift and DC offset circuit. Held at H level at normal mode.
18	VDD5	-	–	Power supply	Supply +5 V power.
19	GND	-	–	Ground	A grounding pin.
20	VH1X	O5	⊓	Read-out pulse output	A pulse that transfers the charge of the photodiode to the vertical shift resister. Connect to the 1BX pin of vertical driver IC.
21	VH3X	O5	–	Read-out pulse output	A pulse that transfers the charge of the photodiode to the vertical shift resister. Connect to the 3BX pin of vertical driver IC.
22	TST1	ICD5	–	Test terminal 1	A test pin. Set open or to L level in the normal mode.
23	FR	O6MA 52	⊓	Reset pulse output	A reset pulse for CCD. To be connected to ϕR of CCD through the D.C. offset circuit.
24	NC	-	–	(No-connect)	Non-connection.
25	CKI	OSCI3	⊓⊓	Clock input	An input pin for reference clock oscillation. The frequencies are as follows : at NTSC mode : 28.63636MHz (1820fH) at PAL mode : 28.37500MHz (1816fH) fH=Hor. frequency
26	CKO	OSCO3	⊓	Clock output	An output pin for reference clock oscillation. The output is the inverse CKI(pin 25).
27	TST2	ICD3	–	Test terminal 2	A test pin. Set open or to L level in the normal mode.
28	SGCK	O6MA 32	–	SSG clock output	A pulse for clock of SSG circuit. The frequencies are as follows : at NTSC mode : 14.31818MHz (910fH) at CCIR mode : 14.18750MHz (908fH)
29	CDCK	O6MA 32	–	DSP clock output	A pulse for clock of DSP-IC. The frequencies are as follows :
30	VDD3	-	–	Power supply	Supply +5 V power.
31	GND	-	–	Ground	A grounding pin.

SCCD	L	H or open
NTSC mode	9.5035MHz (1820/3fH)	14.31818MHz (910fH)
PAL mode	9.4375MHz (1816/3fH)	14.18750MHz (908fH)

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Pol.</th><th>Pin Name</th><th>Description</th></tr>
<tr><td>32</td><td>ADCK</td><td>O6MA
32</td><td>–</td><td>AD clock
output</td><td>A pulse for clock of A/D converter.
The frequencies are as follows :
<table>
<tr><th>SCCD</th><th>L</th><th>H or open</th></tr>
<tr><td>NTSC mode</td><td>9.5035MHz
(1820/3fH)</td><td>14.31818MHz
(910fH)</td></tr>
<tr><td>PAL mode</td><td>9.4375MHz
(1816/3fH)</td><td>14.18750MHz
(908fH)</td></tr>
</table>
The phase of ADCK is selected by SAD1(pin35) and SAD2(pin36) .</td></tr>
<tr><td>33</td><td>VD</td><td>IC3</td><td>⎍</td><td>Ver. drive
pulse</td><td>The pulse occurs at the start of every fields.
To be connected to the DSP-IC.</td></tr>
<tr><td>34</td><td>HP</td><td>IC3</td><td>⎍</td><td>Hor. drive
pulse</td><td>The pulse occurs at the start of lines.
To be connected to the DSP-IC.</td></tr>
<tr><td>35</td><td>SAD1</td><td>ICU3</td><td>–</td><td rowspan="2">ADCK phase
control input</td><td rowspan="2">Pins to control the phase of ADCK.
<table>
<tr><td>SAD1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>SAD2 L</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>ADCK(SCCD=H)</td><td>0°</td><td>delayed
90°</td><td>delayed
180°</td><td>delayed
270°</td></tr>
<tr><td>ADCK(SCCD=L)</td><td>delayed
180°</td><td>delayed
240°</td><td>0°</td><td>delayed
60°</td></tr>
</table></td></tr>
<tr><td>36</td><td>SAD2</td><td>ICU5</td><td>–</td></tr>
<tr><td>37</td><td>PBLK</td><td>05</td><td>⎎</td><td>Pre-blanking
pulse output</td><td>A pulse that correspondes to the cease period of the horizontal transfer pulse.</td></tr>
<tr><td>38</td><td>FS</td><td>O6MA5</td><td>⎍</td><td>CDS pulse 2</td><td>A pulse to sample-hold the signal from CCD.
Generated by SFS1(pin 5) and SFS2(pin 6).</td></tr>
<tr><td>39</td><td>FCDS</td><td>O6MA5</td><td>⎍</td><td>CDS pulse 1</td><td>A pulse to clamp the feed-through level from CCD.
Generated by SFC1(pin 1) and SFC2(pin 2).</td></tr>
<tr><td>40</td><td>TVMD</td><td>ICU5</td><td>–</td><td>TV mode select</td><td>An input pin to select TV standards.
L level ; NTSC mode
H level or open : PAL mode</td></tr>
<tr><td>41</td><td>NC</td><td>-</td><td>–</td><td>(No-connect)</td><td>Non-connection.</td></tr>
<tr><td>42</td><td>VDD5</td><td>-</td><td>–</td><td>Power supply</td><td>Supply +5 V power.</td></tr>
<tr><td>43</td><td>GND</td><td>-</td><td>–</td><td>Ground</td><td>A grounding pin.</td></tr>
<tr><td>44</td><td>FH1</td><td>O6MA
53</td><td>⎍⎍</td><td>Hor. transfer
pulse 1</td><td>A horizontal transfer pulse for CCD.
To be connected to ϕH1 of CCD.</td></tr>
<tr><td>45</td><td>VDD5</td><td>-</td><td>–</td><td>Power supply</td><td>Supply +5 V power.</td></tr>
<tr><td>46</td><td>FH2</td><td>O6MA
53</td><td>⎍⎍</td><td>Hor. transfer
pulse 2</td><td>A horizontal transfer pulse for CCD.
In SSCD=L, FH2 is continueous.
To be connected to ϕH2 of CCD.</td></tr>
<tr><td>47</td><td>NC</td><td>-</td><td>–</td><td>(No-connect)</td><td>Non-connection.</td></tr>
<tr><td>48</td><td>TST3</td><td>ICD3</td><td>–</td><td>Test terminal 3</td><td>A test pin. Set open or to L level in the normal mode.</td></tr>
</table>

4-2. Shutter Speed Contorol.

(1) Timing of Serial Data input



The data of shutter speed is lasched by the rising edge of HP, wich horoizontal line number is in VH1X output.

(2) Table of the serial shutter data

Serial Data													Exposure Period(H)	
D0	D1	D2	D3	D4	D5	D6	D7	D8	SMD1	SMD2	dummy	n	NTSC	PAL
×	×	×	×	×	×	×	×	×	H	H	×	–	262H, 263H	312H, 312H
×	×	×	×	×	×	×	×	×	L	L	×	–	157H+A	260H+B
×	×	×	×	×	×	×	×	×	H	L	×	–	INHIBIT	INHIBIT
L	L	L	L	L	L	L	L	L	L	H	×	–	INHIBIT	INHIBIT
H	L	L	L	L	L	L	L	L	L	H	×	1	261H+A	311H+B
L	H	L	L	L	L	L	L	L	L	H	×	2	260H+A	310H+B
H	H	L	L	L	L	L	L	L	L	H	×	3	259H+A	309H+B
L	L	H	L	L	L	L	L	L	L	H	×	4	258H+A	308H+B
H	L	H	L	L	L	L	L	L	L	H	×	5	257H+A	307H+B
L	H	H	L	L	L	L	L	L	L	H	×	6	256H+A	306H+B
H	H	H	L	L	L	L	L	L	L	H	×	7	255H+A	305H+B
L	L	L	H	L	L	L	L	L	L	H	×	8	254H+A	304H+B
H	L	L	H	L	L	L	L	L	L	H	×	9	253H+A	303H+B
L	H	L	H	L	L	L	L	L	L	H	×	10	252H+A	302H+B
H	H	L	H	L	L	L	L	L	L	H	×	11	251H+A	301H+B
L	L	H	H	L	L	L	L	L	L	H	×	12	250H+A	300H+B
H	L	H	H	L	L	L	L	L	L	H	×	13	249H+A	299H+B
L	H	H	H	L	L	L	L	L	L	H	×	14	248H+A	298H+B
H	H	H	H	L	L	L	L	L	L	H	×	15	247H+A	297H+B
L	L	L	L	H	L	L	L	L	L	H	×	16	246H+A	296H+B
H	L	L	L	H	L	L	L	L	L	H	×	17	245H+A	295H+B
≀	≀	≀	≀	≀	≀	≀	≀	≀	L	H	×	≀	≀	≀
L	L	H	L	H	H	H	H	L	L	H	×	244	18H+A	68H+B
H	L	H	L	H	H	H	H	L	L	H	×	245	17H+A	67H+B
L	H	H	L	H	H	H	H	L	L	H	×	246	16H+A	66H+B
H	H	H	L	H	H	H	H	L	L	H	×	247	15H+A	65H+B
L	L	L	H	H	H	H	H	L	L	H	×	248	14H+A	64H+B
H	L	L	H	H	H	H	H	L	L	H	×	249	13H+A	63H+B
L	H	L	H	H	H	H	H	L	L	H	×	250	12H+A	62H+B
H	H	L	H	H	H	H	H	L	L	H	×	251	11H+A	61H+B
L	L	H	H	H	H	H	H	L	L	H	×	252	10H+A	60H+B
H	L	H	H	H	H	H	H	L	L	H	×	253	9H+A	59H+B

Serial Data												n	Exposure Period(H)	
D0	D1	D2	D3	D4	D5	D6	D7	D8	SMD1	SMD2	dummy		NTSC	PAL
L	H	H	H	H	H	H	H	L	L	H	×	254	8H+A	58H+B
H	H	H	H	H	H	H	H	L	L	H	×	255	7H+A	57H+B
L	L	L	L	L	L	L	L	H	L	H	×	256	6.76H	56H+B
H	L	L	L	L	L	L	L	H	L	H	×	257	6H+A	55H+B
L	H	L	L	L	L	L	L	H	L	H	×	258	5.76H	54H+B
H	H	L	L	L	L	L	L	H	L	H	×	259	5H+A	53H+B
L	L	H	L	L	L	L	L	H	L	H	×	260	4.76H	52H+B
H	L	H	L	L	L	L	L	H	L	H	×	261	4H+A	51H+B
L	H	H	L	L	L	L	L	H	L	H	×	262	3.92H	50H+B
H	H	H	L	L	L	L	L	H	L	H	×	263	3.58H	49H+B
L	L	L	H	L	L	L	L	H	L	H	×	264	3H+A	48H+B
H	L	L	H	L	L	L	L	H	L	H	×	265	2.92H	47H+B
L	H	L	H	L	L	L	L	H	L	H	×	266	2.58H	46H+B
H	H	L	H	L	L	L	L	H	L	H	×	267	2H+A	45H+B
L	L	H	H	L	L	L	L	H	L	H	×	268	2.05H	44H+B
H	L	H	H	L	L	L	L	H	L	H	×	269	1.83H	43H+B
L	H	H	H	L	L	L	L	H	L	H	×	270	1.63H	42H+B
H	H	H	H	L	L	L	L	H	L	H	×	271	1.45H	41H+B
L	L	L	L	H	L	L	L	H	L	H	×	272	1H+A	40H+B
H	L	L	L	H	L	L	L	H	L	H	×	273	1,27H	39H+B
L	H	L	L	H	L	L	L	H	L	H	×	274	0.99H	38H+B
H	H	L	L	H	L	L	L	H	L	H	×	275	0.87H	37H+B
L	L	H	L	H	L	L	L	H	L	H	×	276	0.76H	36H+B
H	L	H	L	H	L	L	L	H	L	H	×	277	0.67H	35H+B
L	H	H	L	H	L	L	L	H	L	H	×	278	0.58H	34H+B
H	H	H	L	H	L	L	L	H	L	H	×	279	0.51H	33H+B
L	L	L	H	H	L	L	L	H	L	H	×	280	0.45H	32H+B
H	L	L	H	H	L	L	L	H	L	H	×	281	0.39H	31H+B
L	H	L	H	H	L	L	L	H	L	H	×	282	0.34H	30H+B
H	H	L	H	H	L	L	L	H	L	H	×	283	0.31H	29H+B
L	L	H	H	H	L	L	L	H	L	H	×	284	0.28H	28H+B
H	L	H	H	H	L	L	L	H	L	H	×	285	0.25H	27H+B
L	H	H	H	H	L	L	L	H	L	H	×	286	0.22H	26H+B
H	H	H	H	H	L	L	L	H	L	H	×	287	0.20H	25H+B
L	L	L	L	L	H	L	L	H	L	H	×	288	0.17H	24H+B
H	L	L	L	L	H	L	L	H	L	H	×	289	0.16H	23H+B
L	H	L	L	L	H	L	L	H	L	H	×	290	INHIBIT	22H+B
H	H	L	L	L	H	L	L	H	L	H	×	291	INHIBIT	21H+B
L	L	H	L	L	H	L	L	H	L	H	×	292	INHIBIT	20H+B
H	L	H	L	L	H	L	L	H	L	H	×	293	INHIBIT	19H+B
L	H	H	L	L	H	L	L	H	L	H	×	294	INHIBIT	18H+B
H	H	H	L	L	H	L	L	H	L	H	×	295	INHIBIT	17H+B
L	L	L	H	L	H	L	L	H	L	H	×	296	INHIBIT	16H+B
H	L	L	H	L	H	L	L	H	L	H	×	297	INHIBIT	15H+B
L	H	L	H	L	H	L	L	H	L	H	×	298	INHIBIT	14H+B

Serial Dat													Exposure P	
D0	D1	D2	D3	D4	D5	D6	D7	D8	SMD1	SMD2	dummy	n	NTSC	PAL
H	H	L	H	L	H	L	L	H	L	H	×	299	INHIBIT	13H+B
L	L	H	H	L	H	L	L	H	L	H	×	300	INHIBIT	12H+B
H	L	H	H	L	H	L	L	H	L	H	×	301	INHIBIT	11H+B
L	H	H	H	L	H	L	L	H	L	H	×	302	INHIBIT	10H+B
H	H	H	H	L	H	L	L	H	L	H	×	303	INHIBIT	9H+B
L	L	L	L	H	H	L	L	H	L	H	×	304	INHIBIT	8H+B
H	L	L	L	H	H	L	L	H	L	H	×	305	INHIBIT	7H+B
L	H	L	L	H	H	L	L	H	L	H	×	306	INHIBIT	6.76H
H	H	L	L	H	H	L	L	H	L	H	×	307	INHIBIT	6H+B
L	L	H	L	H	H	L	L	H	L	H	×	308	INHIBIT	5.76H
H	L	H	L	H	H	L	L	H	L	H	×	309	INHIBIT	5H+B
L	H	H	L	H	H	L	L	H	L	H	×	310	INHIBIT	4.76H
H	H	H	L	H	H	L	L	H	L	H	×	311	INHIBIT	4H+B
L	L	L	H	H	H	L	L	H	L	H	×	312	INHIBIT	3.92H
H	L	L	H	H	H	L	L	H	L	H	×	313	INHIBIT	3.58H
L	H	L	H	H	H	L	L	H	L	H	×	314	INHIBIT	3H+B
H	H	L	H	H	H	L	L	H	L	H	×	315	INHIBIT	2.92H
L	L	H	H	H	H	L	L	H	L	H	×	316	INHIBIT	2.58H
H	L	H	H	H	H	L	L	H	L	H	×	317	INHIBIT	2H+B
L	H	H	H	H	H	L	L	H	L	H	×	318	INHIBIT	2.05H
H	H	H	H	H	H	L	L	H	L	H	×	319	INHIBIT	1.83H
L	L	L	L	L	L	H	L	H	L	H	×	320	INHIBIT	1.63H
H	L	L	L	L	L	H	L	H	L	H	×	321	INHIBIT	1.54H
L	H	L	L	L	L	H	L	H	L	H	×	322	INHIBIT	1H+B
H	H	L	L	L	L	H	L	H	L	H	×	323	INHIBIT	1.13H
L	L	H	L	L	L	H	L	H	L	H	×	324	INHIBIT	0.99H
H	L	H	L	L	L	H	L	H	L	H	×	325	INHIBIT	0.87H
L	H	H	L	L	L	H	L	H	L	H	×	326	INHIBIT	0.76H
H	H	H	L	L	L	H	L	H	L	H	×	327	INHIBIT	0.67H
L	L	L	H	L	L	H	L	H	L	H	×	328	INHIBIT	0.58H
H	L	L	H	L	L	H	L	H	L	H	×	329	INHIBIT	0.51H
L	H	L	H	L	L	H	L	H	L	H	×	330	INHIBIT	0.45H
H	H	L	H	L	L	H	L	H	L	H	×	331	INHIBIT	0.39H
L	L	H	H	L	L	H	L	H	L	H	×	332	INHIBIT	0.35H
H	L	H	H	L	L	H	L	H	L	H	×	333	INHIBIT	0.31H
L	H	H	H	L	L	H	L	H	L	H	×	334	INHIBIT	0.28H
H	H	H	H	L	L	H	L	H	L	H	×	335	INHIBIT	0.24H
L	L	L	L	H	L	H	L	H	L	H	×	336	INHIBIT	0.22H
H	L	L	L	H	L	H	L	H	L	H	×	337	INHIBIT	0.20H
L	H	L	L	H	L	H	L	H	L	H	×	338	INHIBIT	0.17H
H	H	L	L	H	L	H	L	H	L	H	×	339	INHIBIT	0.16H
L	L	H	L	H	L	H	L	H	L	H	×	340	INHIBIT	INHIBIT
H	L	H	L	H	L	H	L	H	L	H	×	341	INHIBIT	INHIBIT
∫	∫	∫	∫	∫	∫	∫	∫	∫	L	H	×	∫	INHIBIT	INHIBIT
H	H	H	H	H	H	H	H	H	L	H	×	511	INHIBIT	INHIBIT

A = B ≒ 0.29H

5. Electorical Characteristics

5-1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD3}, V_{DD5}	−0.3 ~ 6.0	V
Input voltage	V_{I3}	−0.3 ~ V_{DD3}+0.3	V
Input voltage	V_{I5}	−0.3 ~ V_{DD5}+0.3	V
Output voltage	V_{O3}	−0.3 ~ V_{DD3}+0.3	V
Output voltage	V_{O5}	−0.3 ~ V_{DD5}+0.3	V
Operation temperature	Topr	−20 ~ +70	℃
Storage tempetature	Tstg	−55 ~ +150	℃

5-2. DC Characteristics (V_{DD3}=+3.3V±10%, V_{DD5}=+5V±10%, Topr=-20~+70℃)

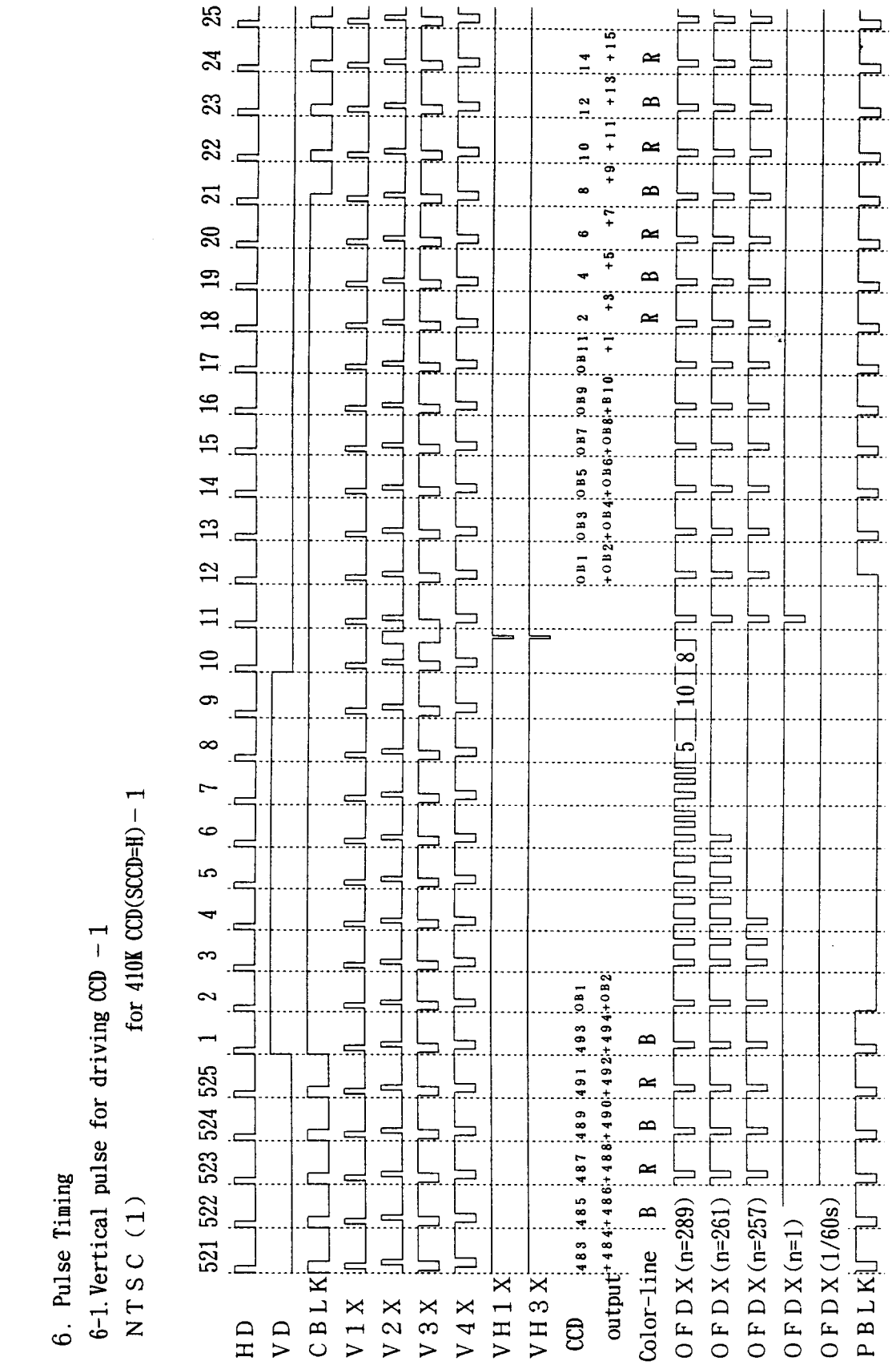
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Note
Input "High" voltage	V_{IH3}		0.7×V_{DD5}			V	1,2,3
Input "Low" voltage	V_{IL3}				0.3×V_{DD5}	V	
Input "High" voltage	V_{IH5}		3.5			V	4,5
Input "Low" voltage	V_{IL5}				1.5	V	
Input "High" current	$\|I_{IH3-1}\|$	V_I = V_{DD3}			1.0	μA	1
	$\|I_{IH3-2}\|$	V_I = V_{DD3}	4.0		30	μA	2
	$\|I_{IH3-3}\|$	V_I = V_{DD3}			2.0	μA	3
Input "Low" current	$\|I_{IL3-1}\|$	V_I = 0 V			1.0	μA	1
	$\|I_{IL3-2}\|$	V_I = 0 V			2.0	μA	2
	$\|I_{IL3-3}\|$	V_I = 0 V	4.0		30	μA	3
Input "High" current	$\|I_{IH5-1}\|$	V_I = V_{DD5}			2.0	μA	4
	$\|I_{IH5-2}\|$	V_I = V_{DD5}	8.0		60	μA	5
Input "Low" current	$\|I_{IL5-1}\|$	V_I = 0 V	8.0		60	μA	4
	$\|I_{IL5-2}\|$	V_I = 0 V			2.0	μA	5
Output "High" voltage	V_{OH3-1}	I_{OH}= −2 mA	4.0			V	6
Output "Low" voltage	V_{OL3-1}	I_{OL}= 2 mA			0.4	V	
Output "High" voltage	V_{OH3-2}	I_{OH}= −6 mA	4.0			V	7
Output "Low" voltage	V_{OL3-2}	I_{OL}= 6 mA			0.4	V	
Output "High" voltage	V_{OH5-1}	I_{OH}= −2 mA	4.0			V	8
Output "Low" voltage	V_{OL5-1}	I_{OL}= 4 mA			0.4	V	
Output "High" voltage	V_{OH5-2}	I_{OH}= −6 mA	4.0			V	9
Output "Low" voltage	V_{OL5-2}	I_{OL}= 6 mA			0.4	V	
Output "High" voltage	V_{OH5-3}	I_{OH}= −12 mA	4.0			V	10
Output "Low" voltage	V_{OL5-3}	I_{OL}= 12 mA			0.4	V	

Note 1 : Applied to Inputs (IC3, OSCI3)
Note 2 : Applied to Input (ICD3).
Note 3 : Applied to Input (ICU3).
Note 4 : Applied to Input (ICU5).
Note 5 : Applied to Input (ICD5).
Note 6 : Applied to Output (OSCO3).
(Output(OSCO3) measures on conditions that input(OSCI3) level is 0V or V_{DD3}.)
Note 7 : Applied to Output(O6MA32).
Note 8 : Applied to Output(O5).
Note 9 : Applied to Output(O6MA5).
Note 10 : Applied to Output(O6MA52).

6. Pulse Timing

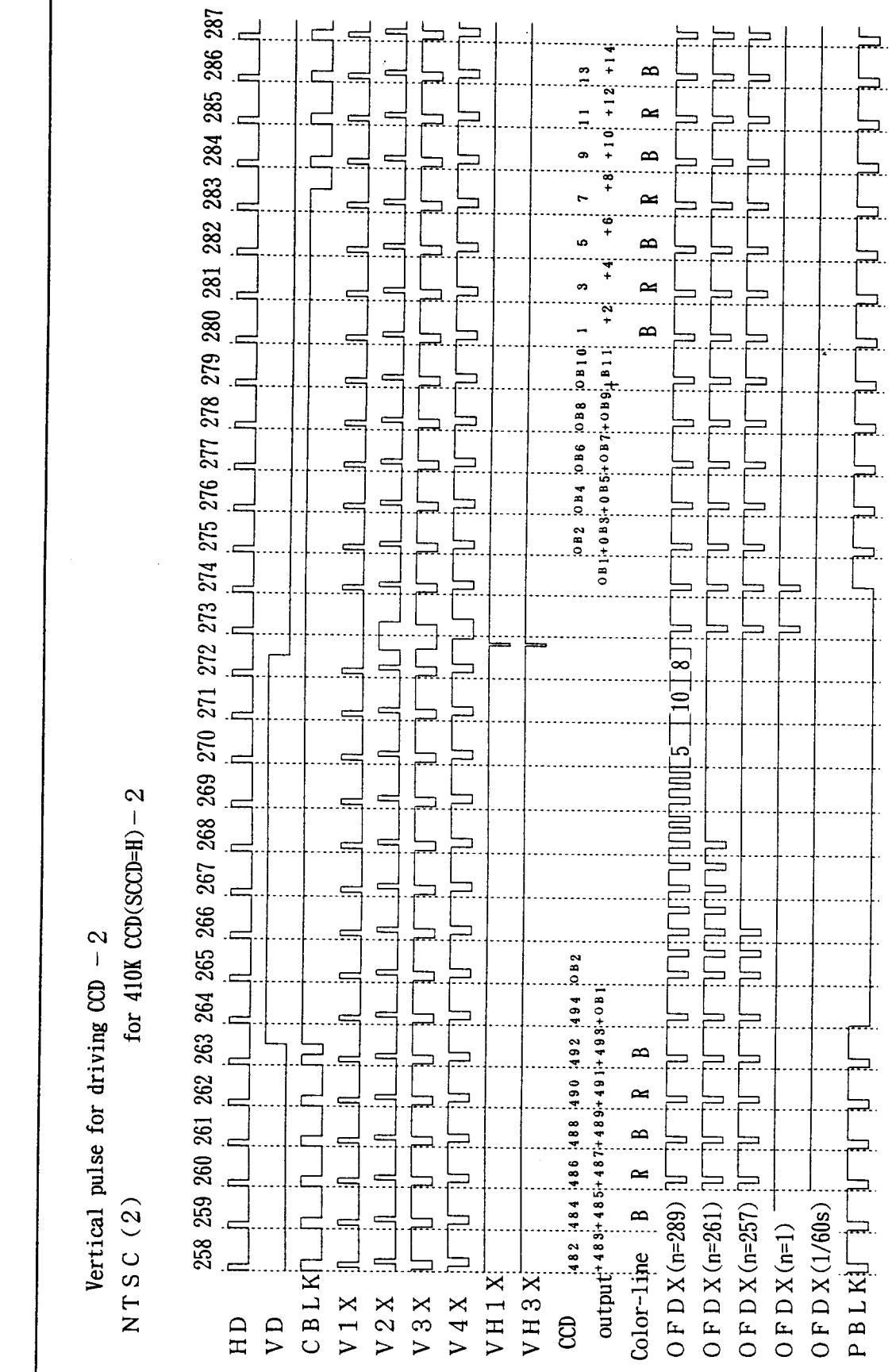
6-1. Vertical pulse for driving CCD – 1

NTSC (1) for 410K CCD(SCCD=H) – 1



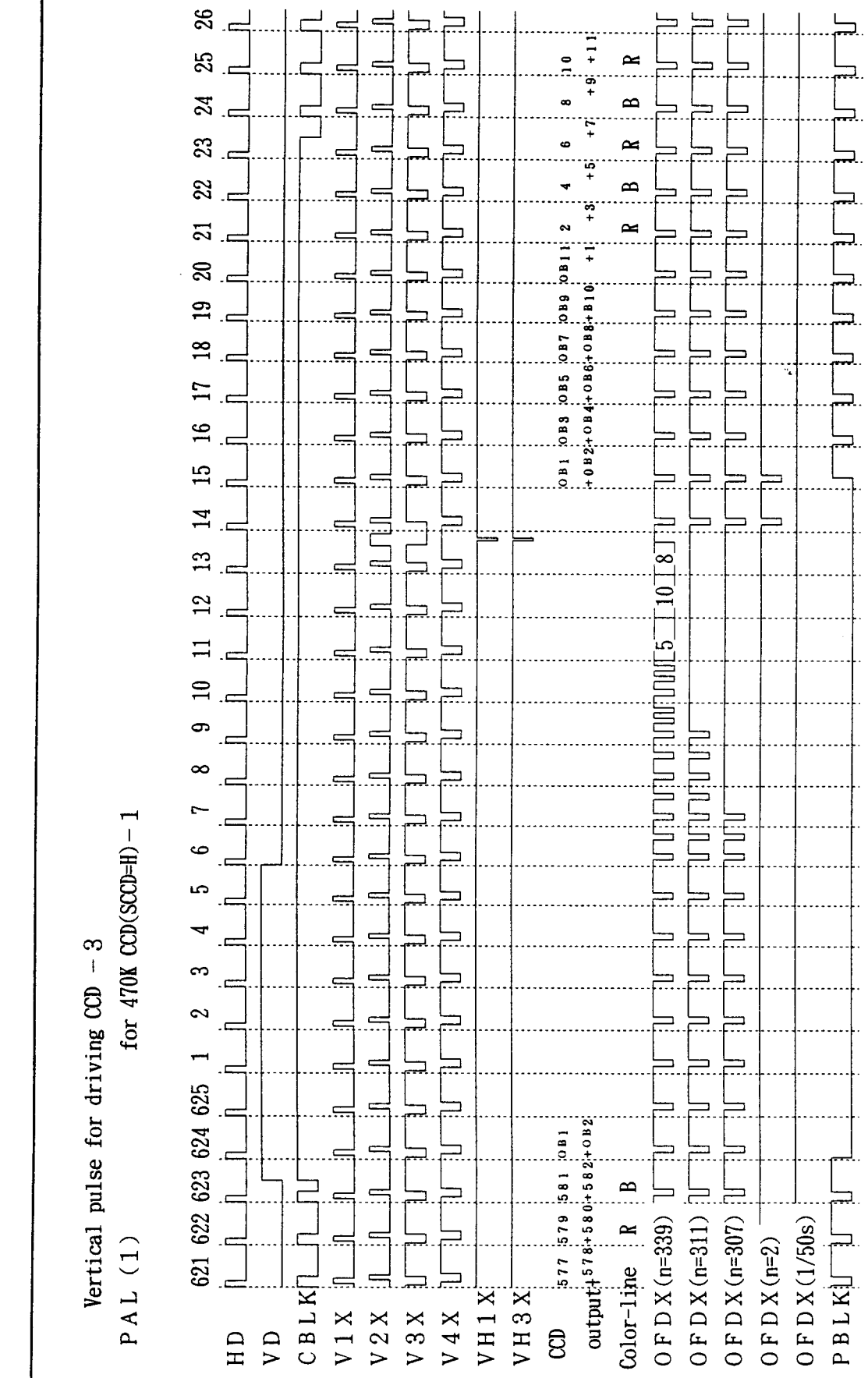
Vertical pulse for driving CCD – 2

NTSC (2) for 410K CCD(SCCD=H) – 2



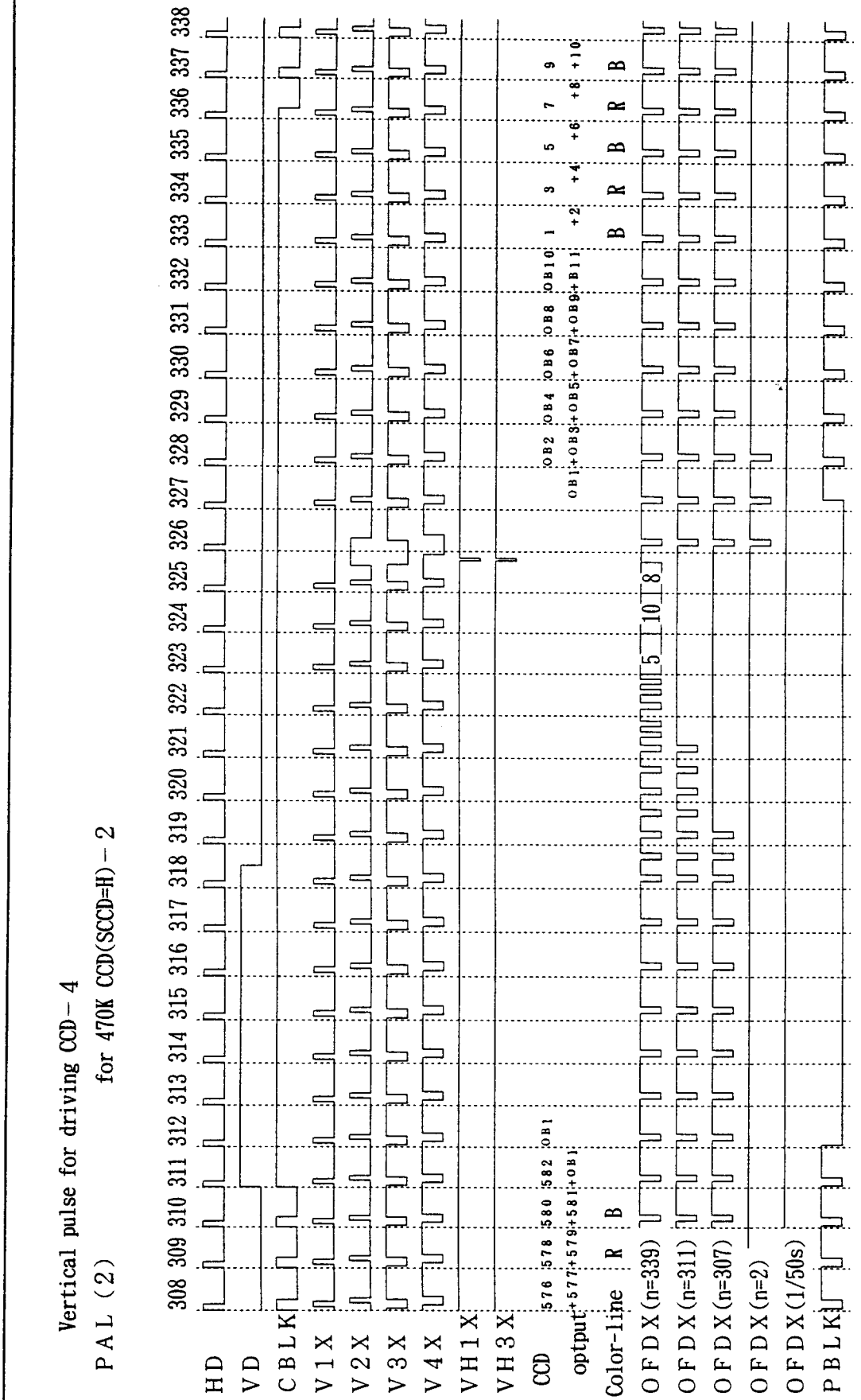
Vertical pulse for driving CCD – 3

PAL (1) for 470K CCD(SCCD=H) – 1



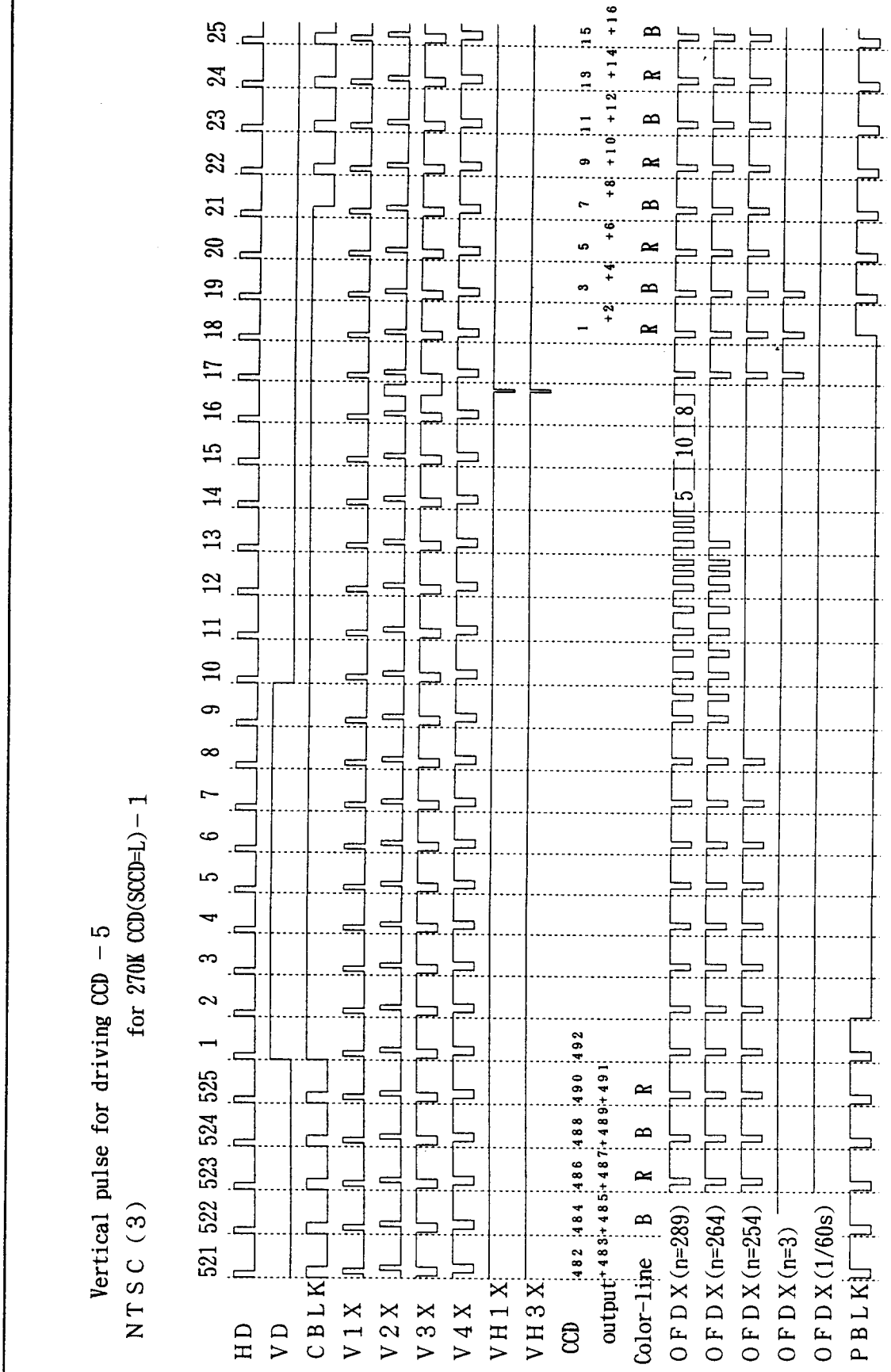
Vertical pulse for driving CCD－4

PAL (2)　　for 470K CCD(SCCD=H)－2



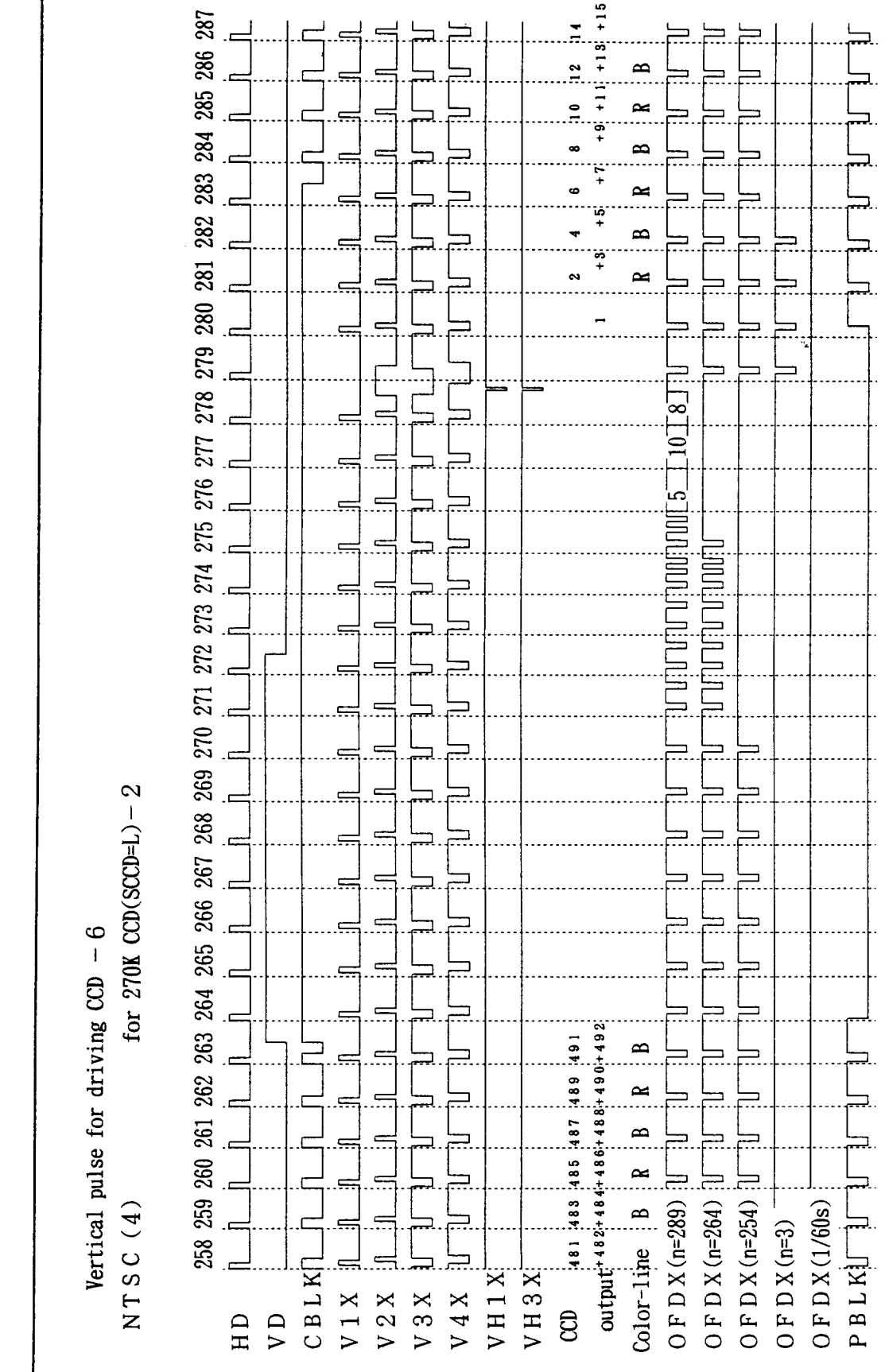
Vertical pulse for driving CCD – 5

NTSC (3) for 270K CCD(SCCD=L) – 1



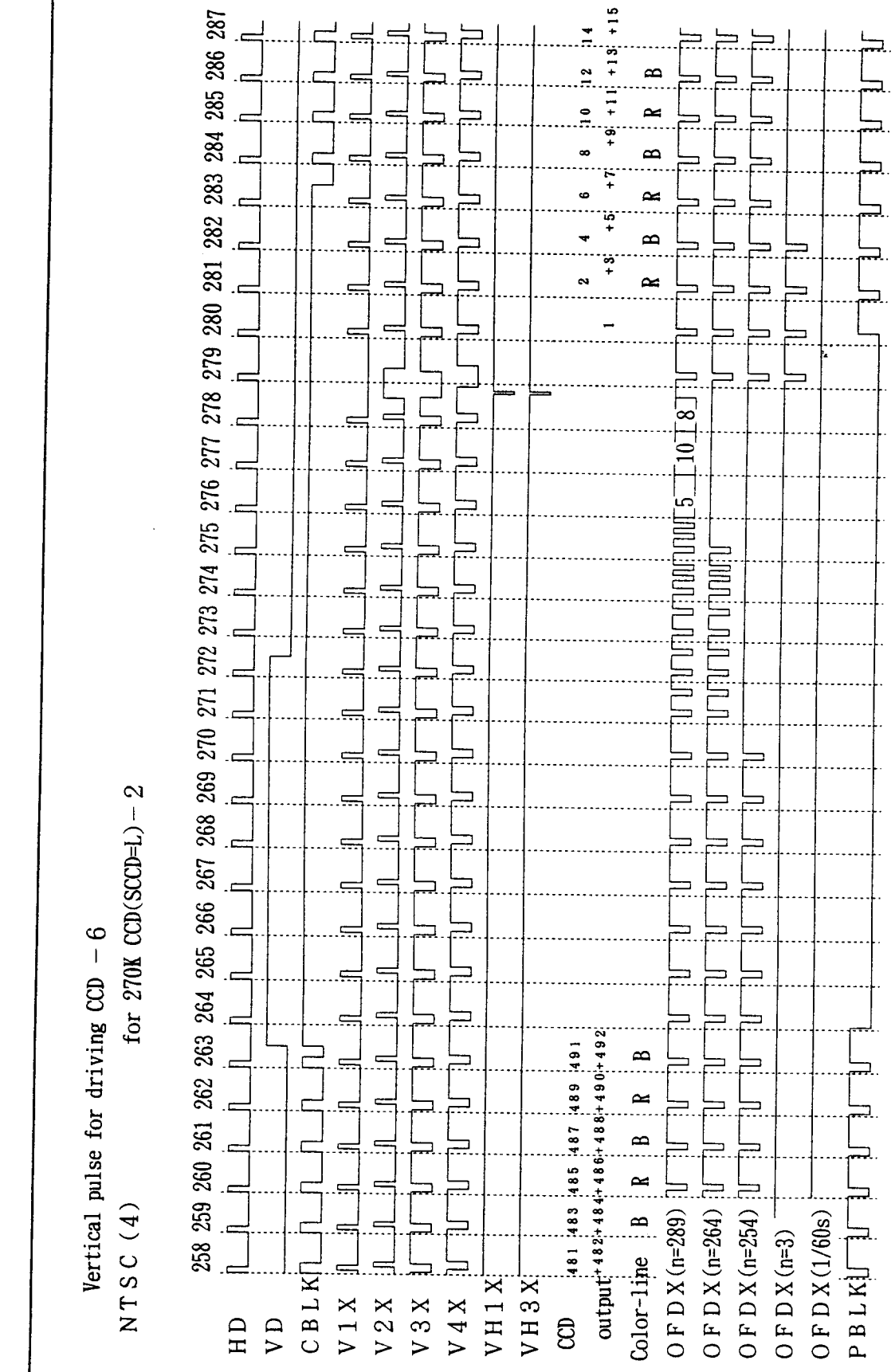
Vertical pulse for driving CCD – 6

NTSC (4) for 270K CCD(SCCD=L) – 2



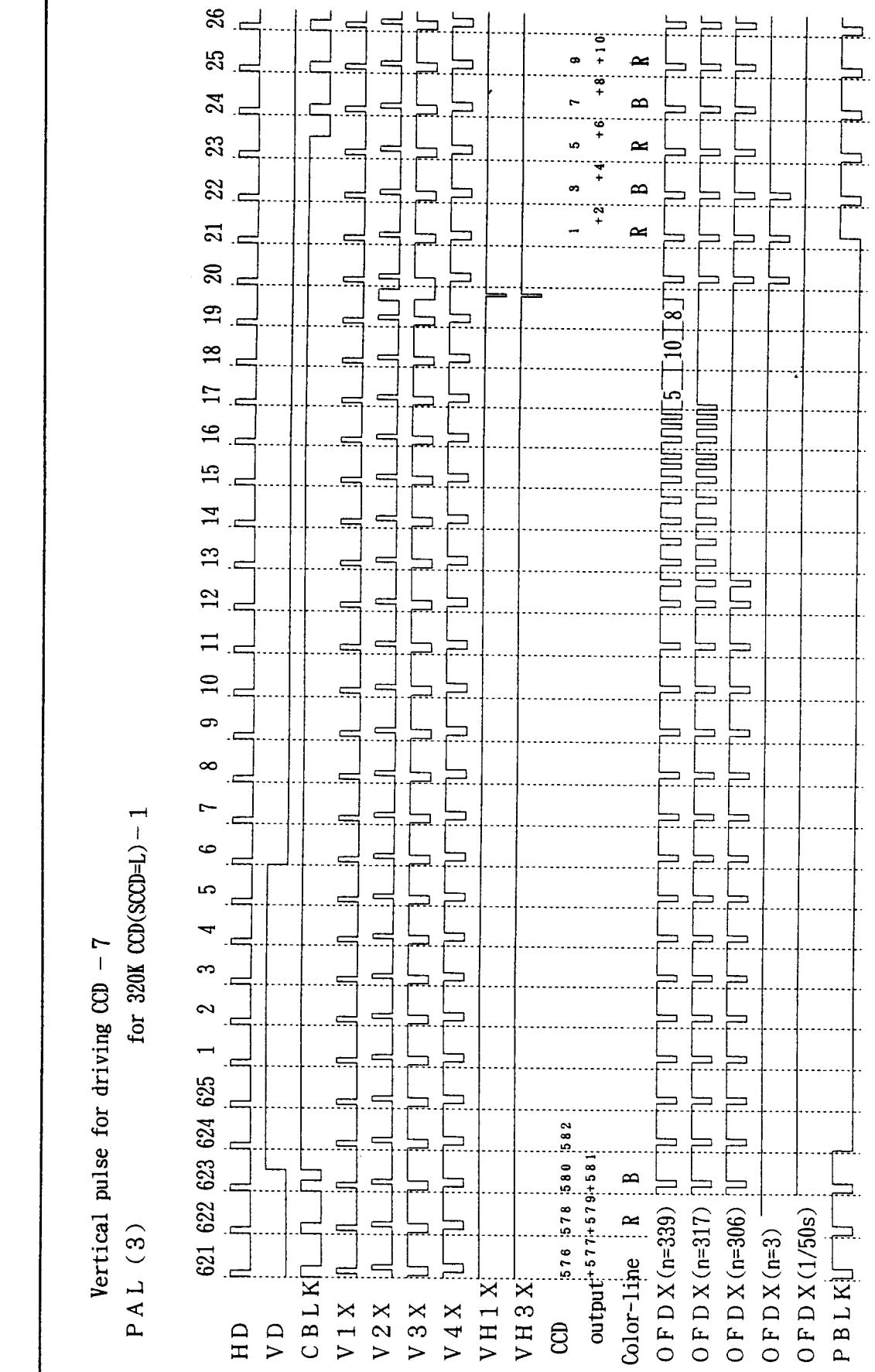
Vertical pulse for driving CCD – 6

NTSC (4) for 270K CCD(SCCD=L) – 2



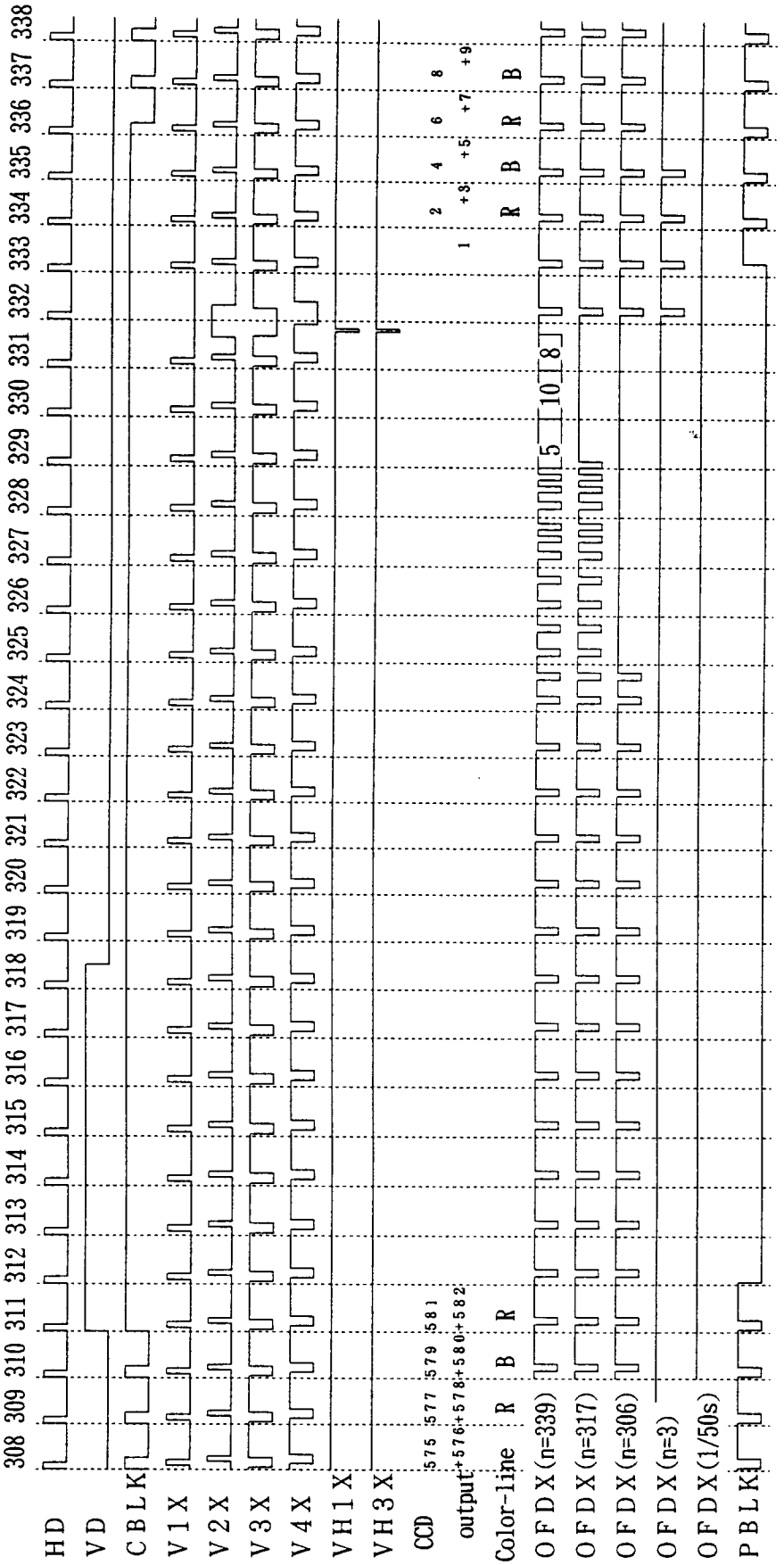
Vertical pulse for driving CCD – 7

PAL (3) for 320K CCD(SCCD=L) – 1



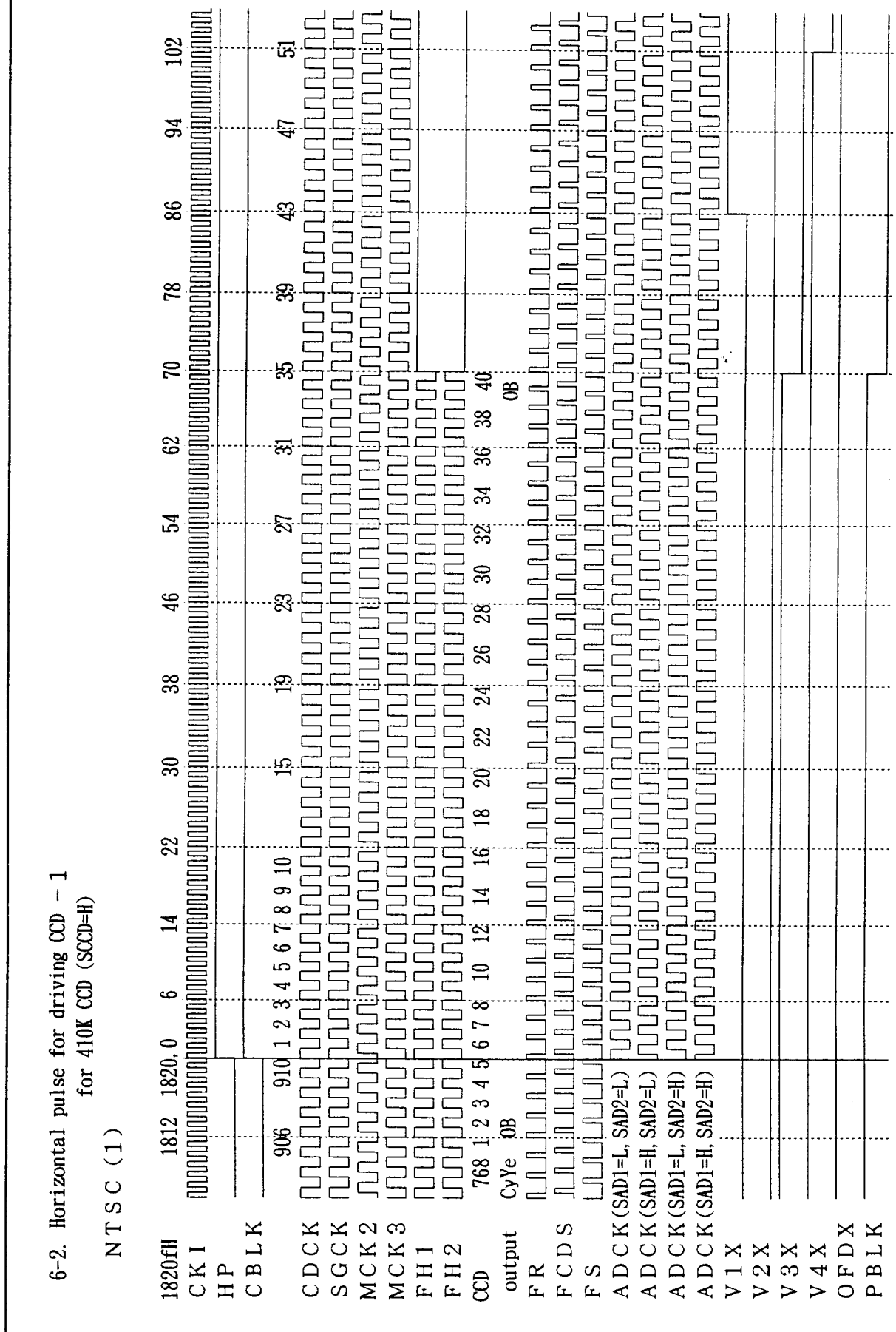
Vertical pulse for driving CCD – 8

PAL (4) for 320K CCD(SCCD=L) – 2



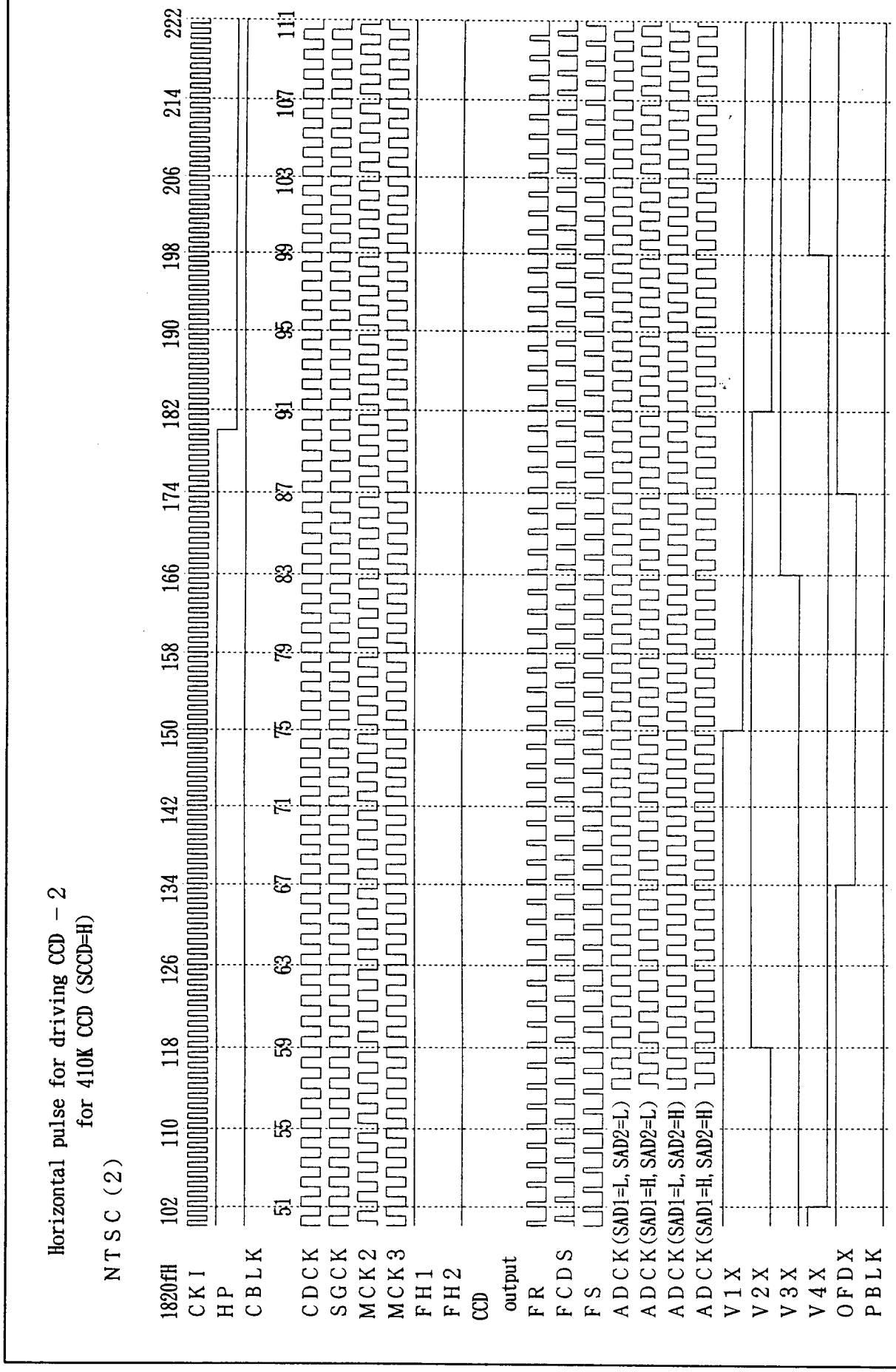
6-2. Horizontal pulse for driving CCD – 1
for 410K CCD (SCCD=H)

NTSC (1)



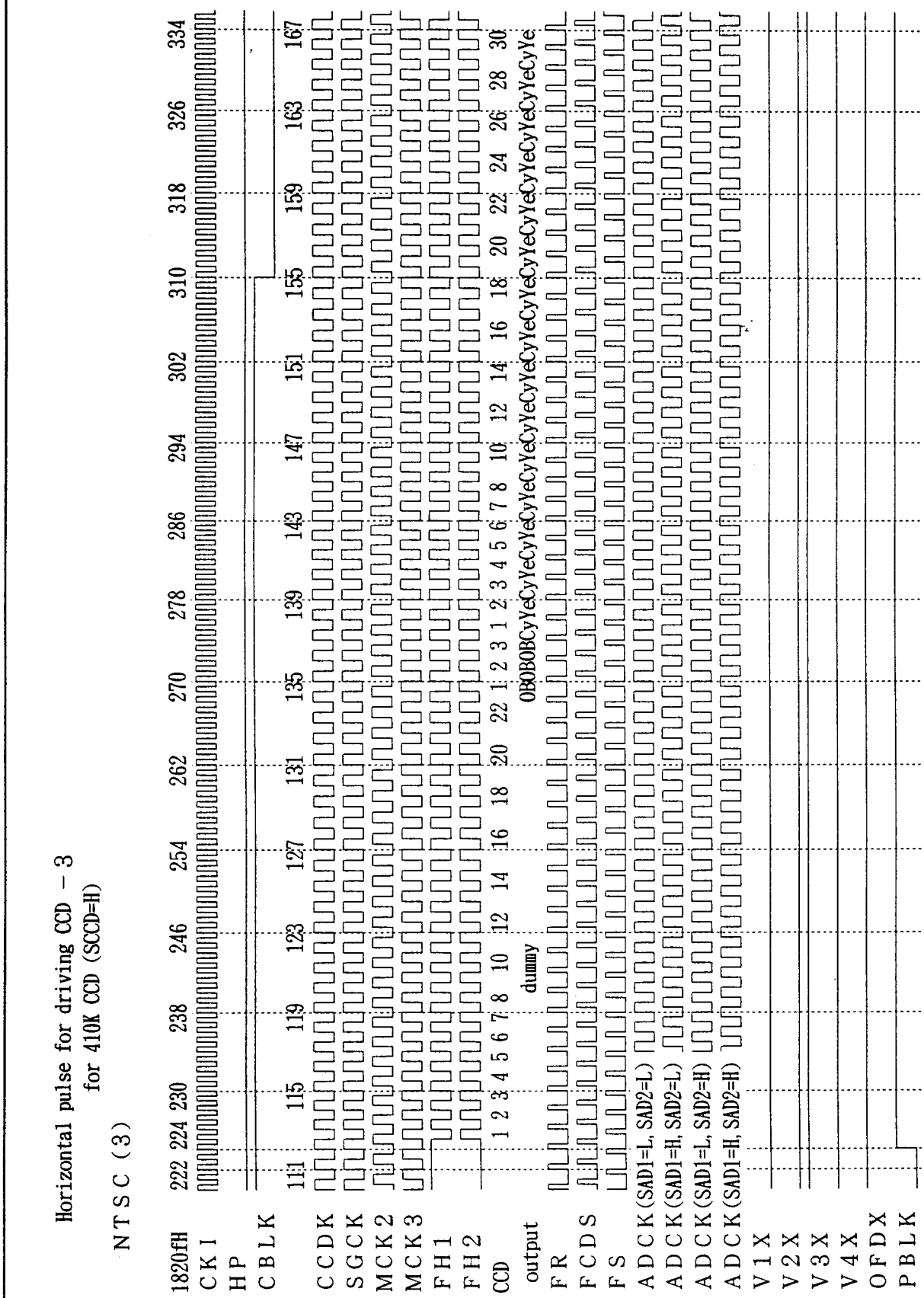
Horizontal pulse for driving CCD – 2
for 410K CCD (SCCD=H)

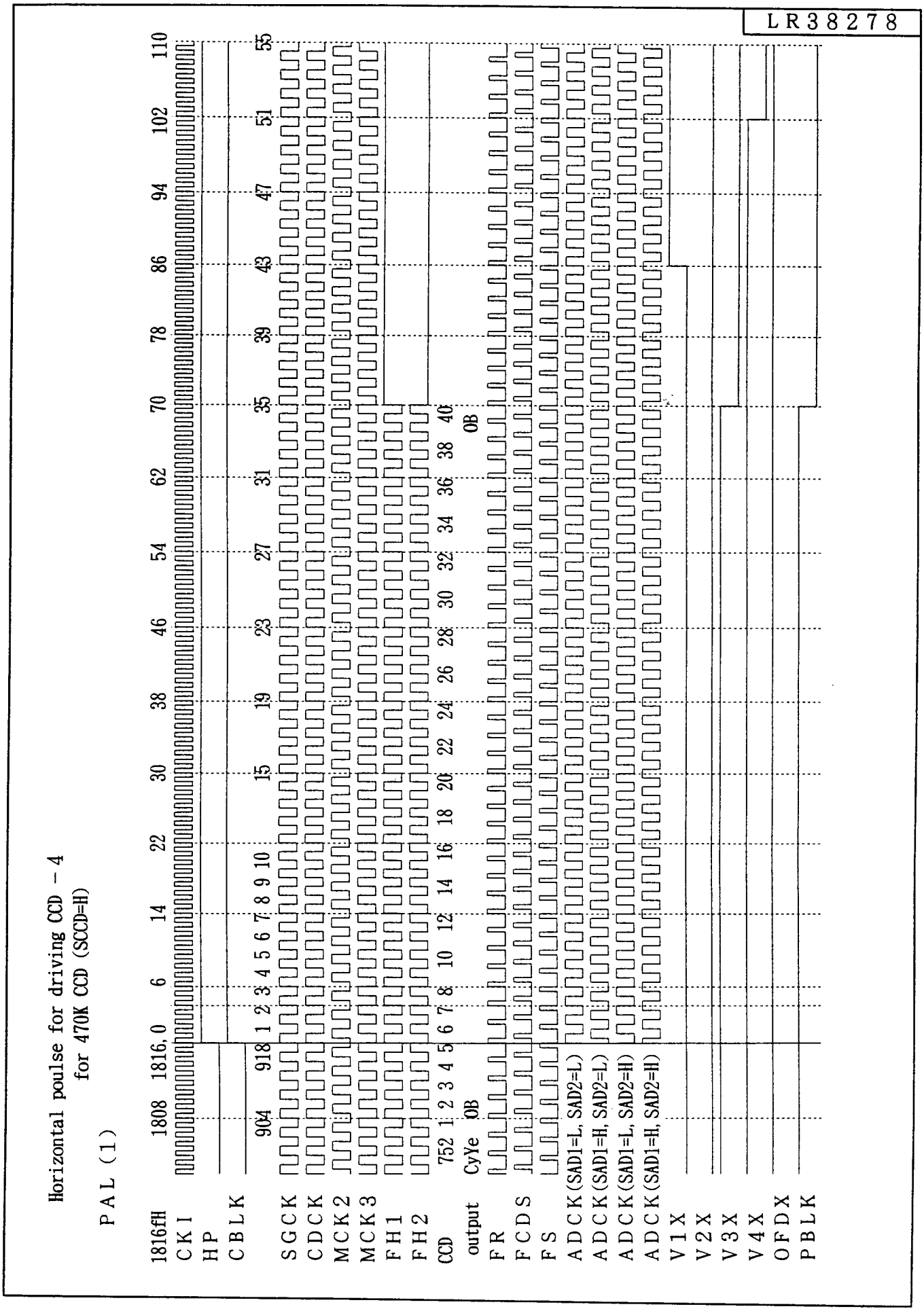
NTSC (2)



Horizontal pulse for driving CCD – 3
for 410K CCD (SCCD=H)

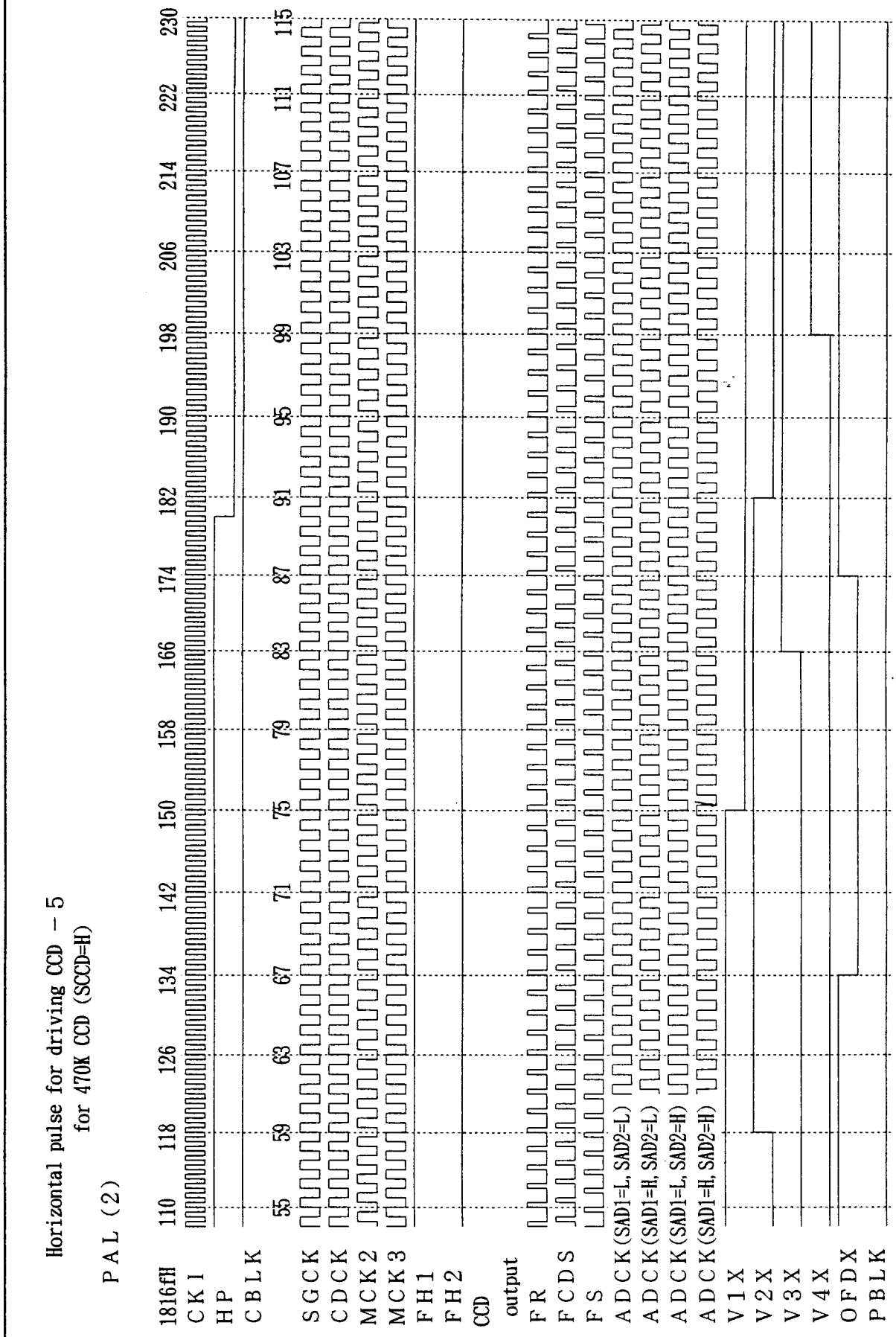
NTSC (3)

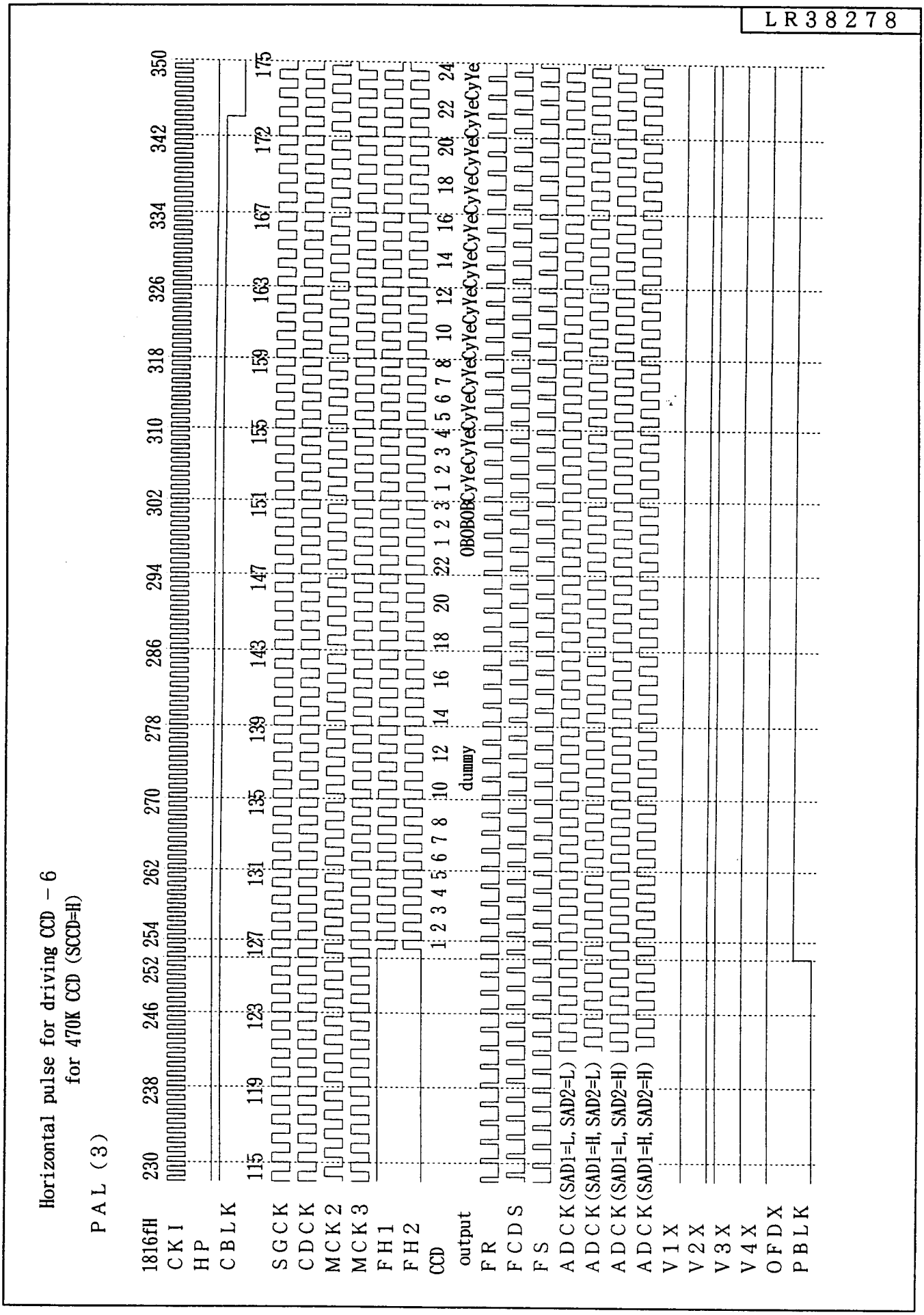



LR38278
Horizontal poulse for driving CCD – 4
for 470K CCD (SCCD=H)
PAL (1)
1816fH
CKI
HP
CBLK
SGCK
CDCK
MCK2
MCK3
FH1
FH2
CCD output
FR
FCDS
FS
ADCK(SAD1=L, SAD2=L)
ADCK(SAD1=H, SAD2=L)
ADCK(SAD1=L, SAD2=H)
ADCK(SAD1=H, SAD2=H)
V1X
V2X
V3X
V4X
OFDX
PBLK
1808 1816, 0 6 14 22 30 38 46 54 62 70 78 86 94 102 110
904 918 1 2 3 4 5 6 7 8 9 10 15 19 23 27 31 35 39 43 47 51 55
752 1 2 3 4 5 6 7 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40
OB CyYe OB OB

Horizontal pulse for driving CCD – 5
for 470K CCD (SCCD=H)

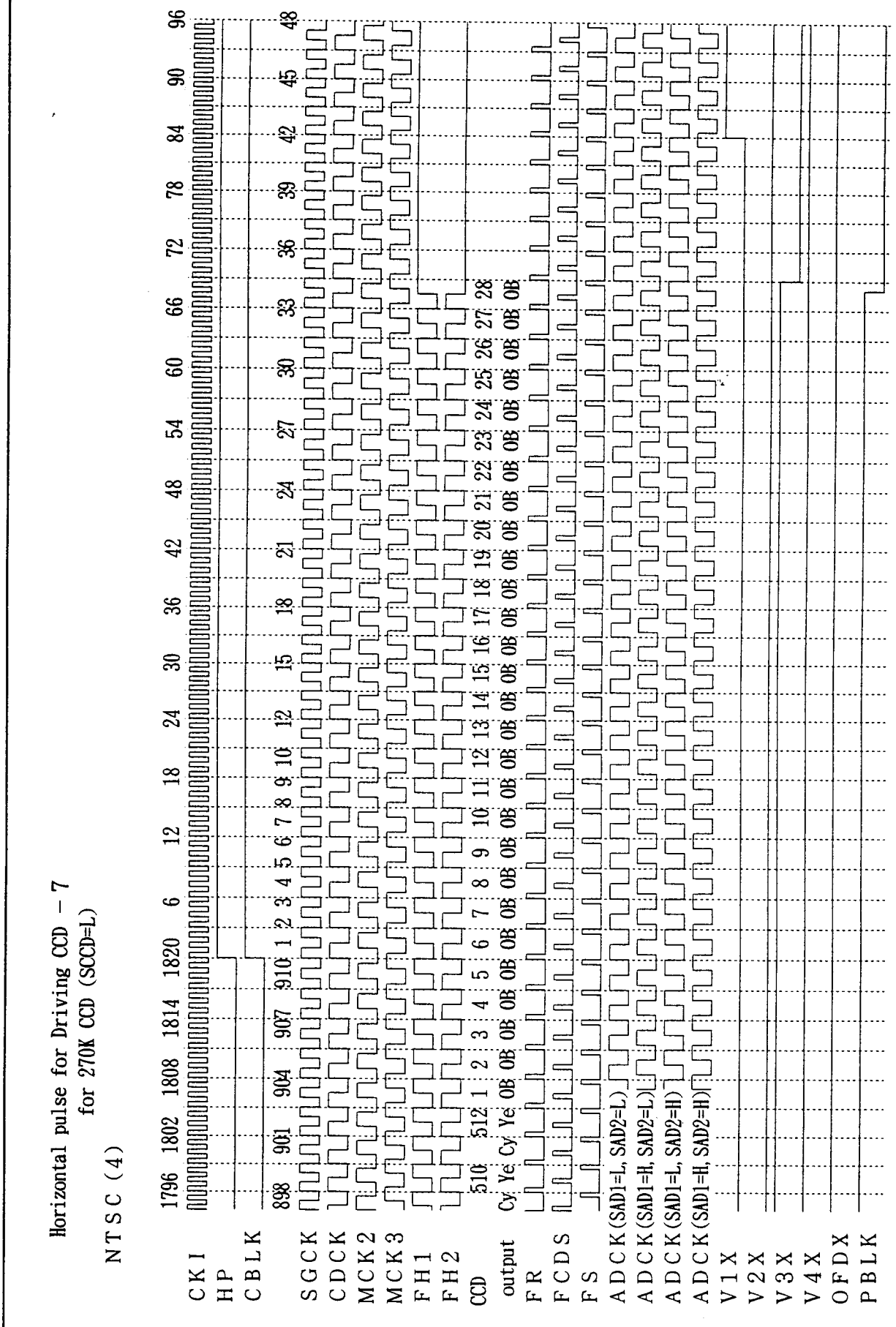
PAL (2)




LR38278
Horizontal pulse for driving CCD – 6
for 470K CCD (SCCD=H)
PAL (3)
1816fH
CKI
HP
CBLK
SGCK
CDCK
MCK2
MCK3
FH1
FH2
CCD output
FRP
FCDS
FS
ADCK(SAD1=L, SAD2=L)
ADCK(SAD1=H, SAD2=L)
ADCK(SAD1=L, SAD2=H)
ADCK(SAD1=H, SAD2=H)
V1X
V2X
V3X
V4X
OFDX
PBLK
dummy
OBOBOBCyYeCyYeCyYeCyYeCyYeCyYeCyYeCyYeCyYeCyYe

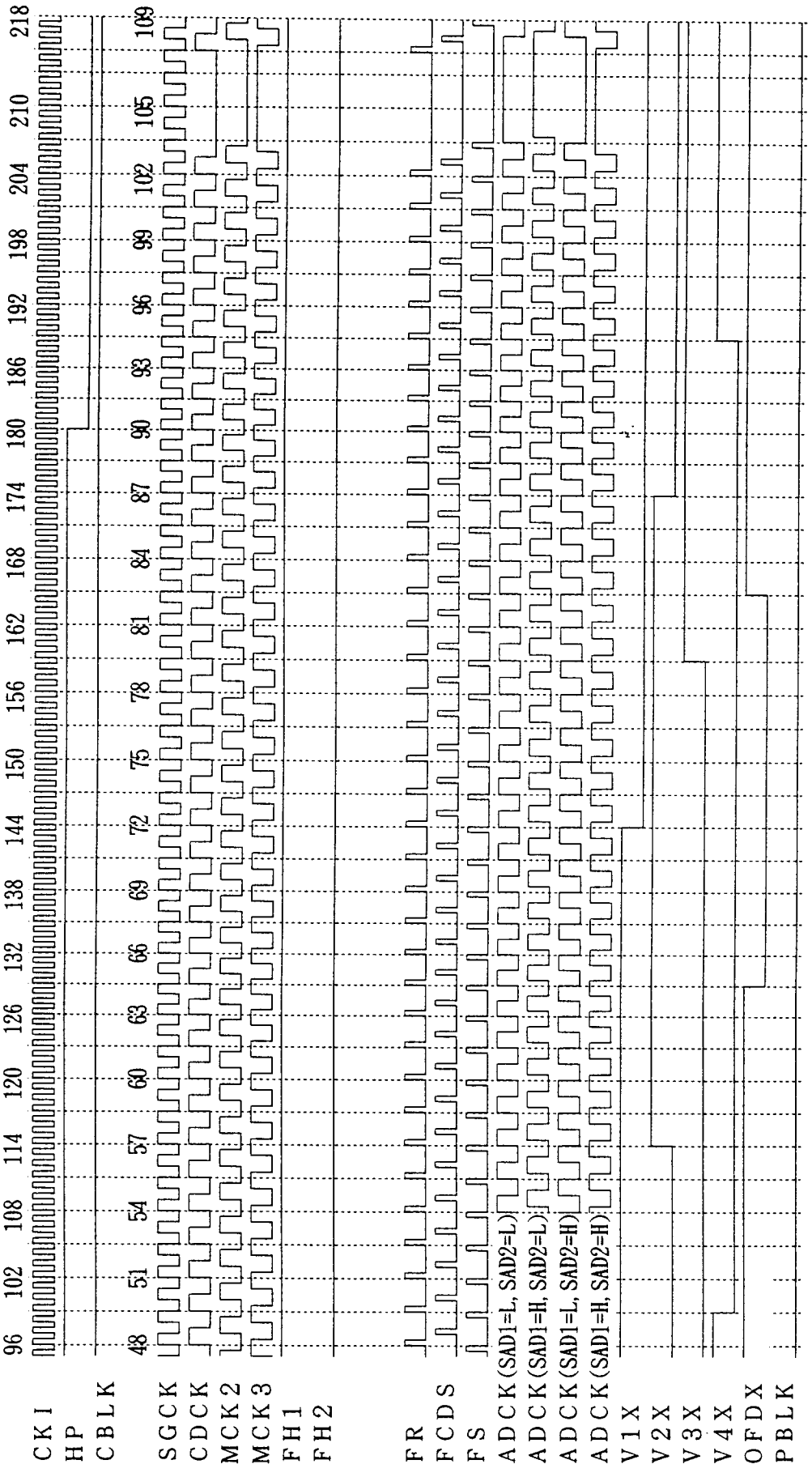
Horizontal pulse for Driving CCD – 7
for 270K CCD (SCCD=L)

NTSC (4)



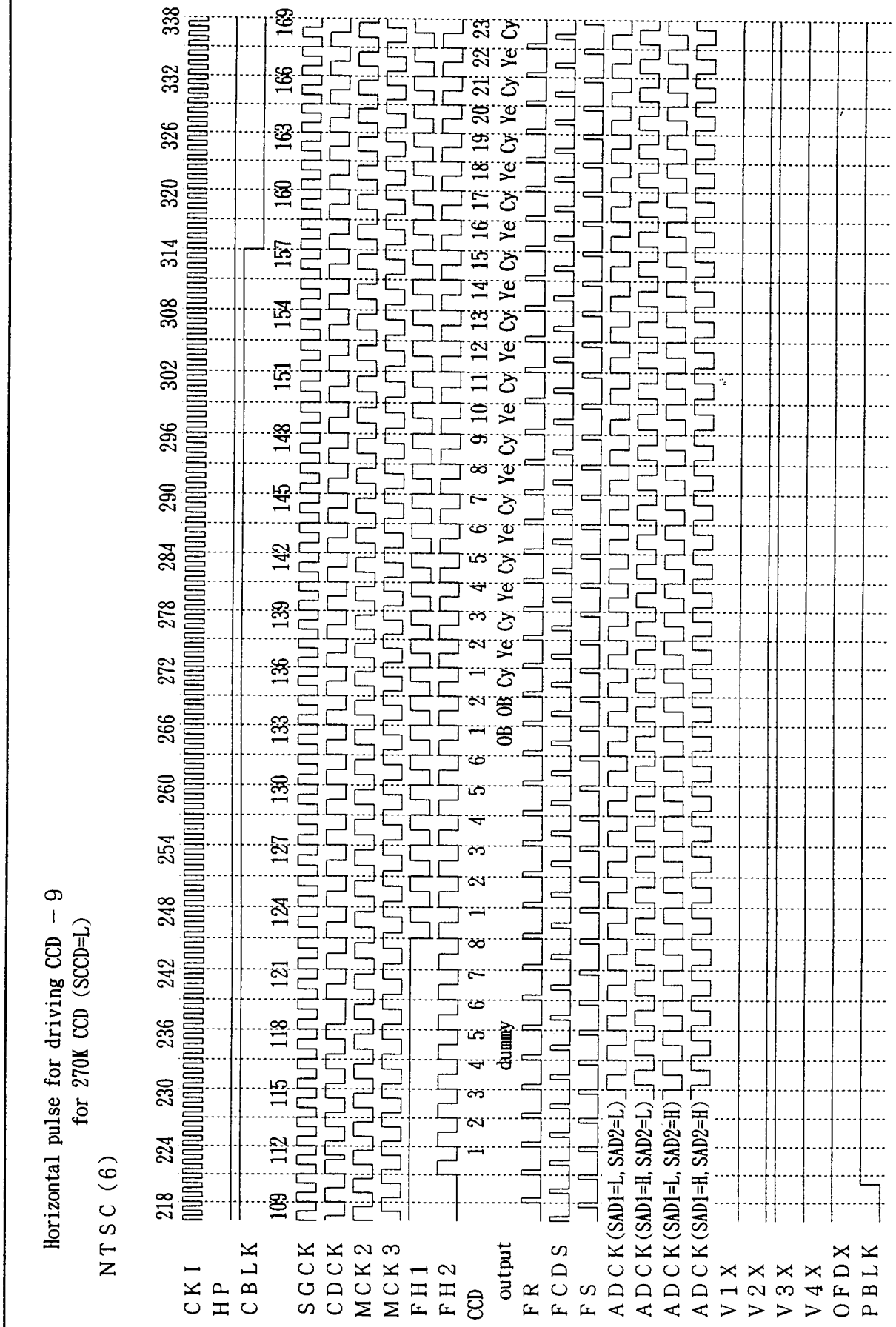
Horizontal pulse for driving CCD – 8
for 270K CCD (SCCD=L)

NTSC (5)



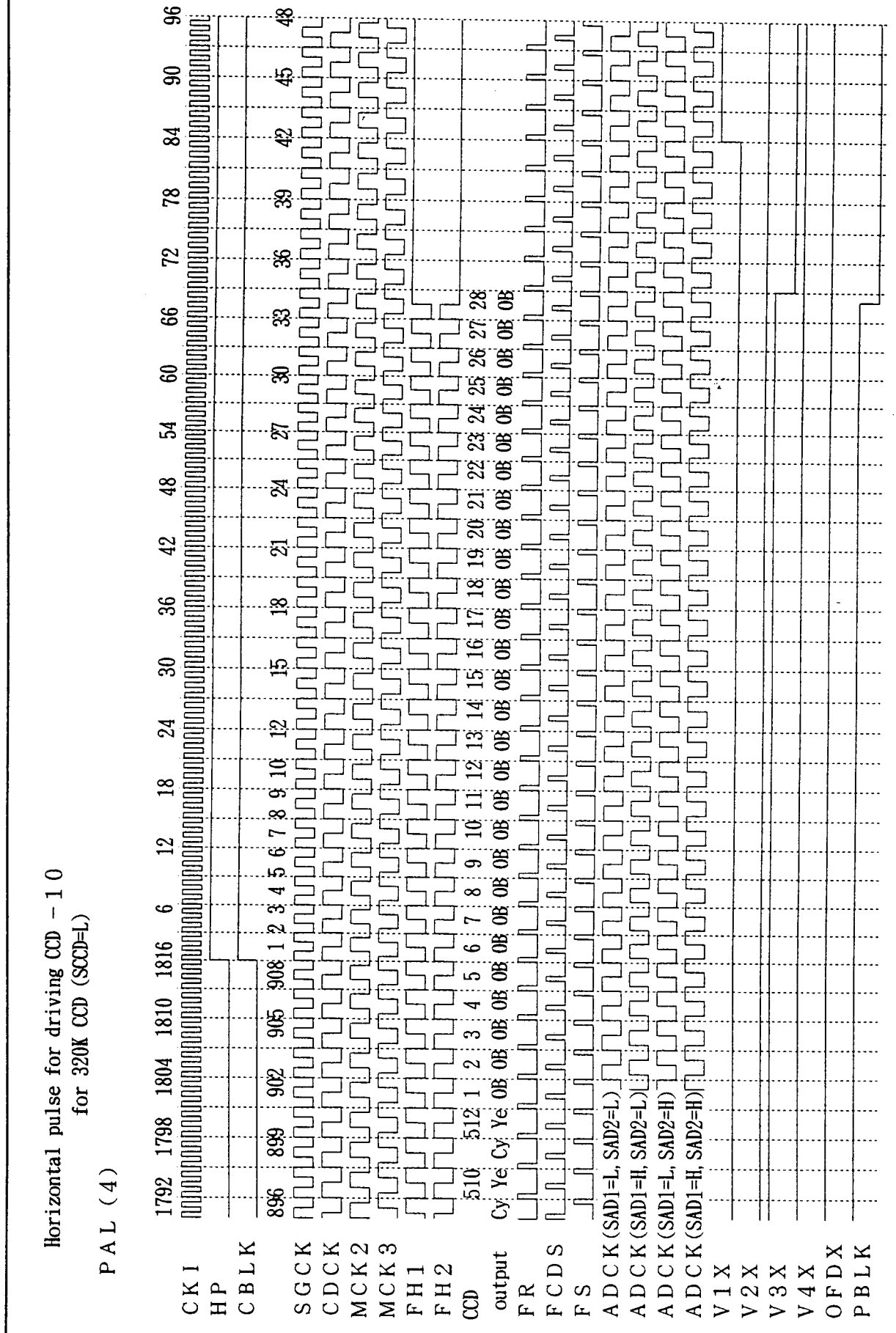
Horizontal pulse for driving CCD – 9
for 270K CCD (SCCD=L)

NTSC (6)



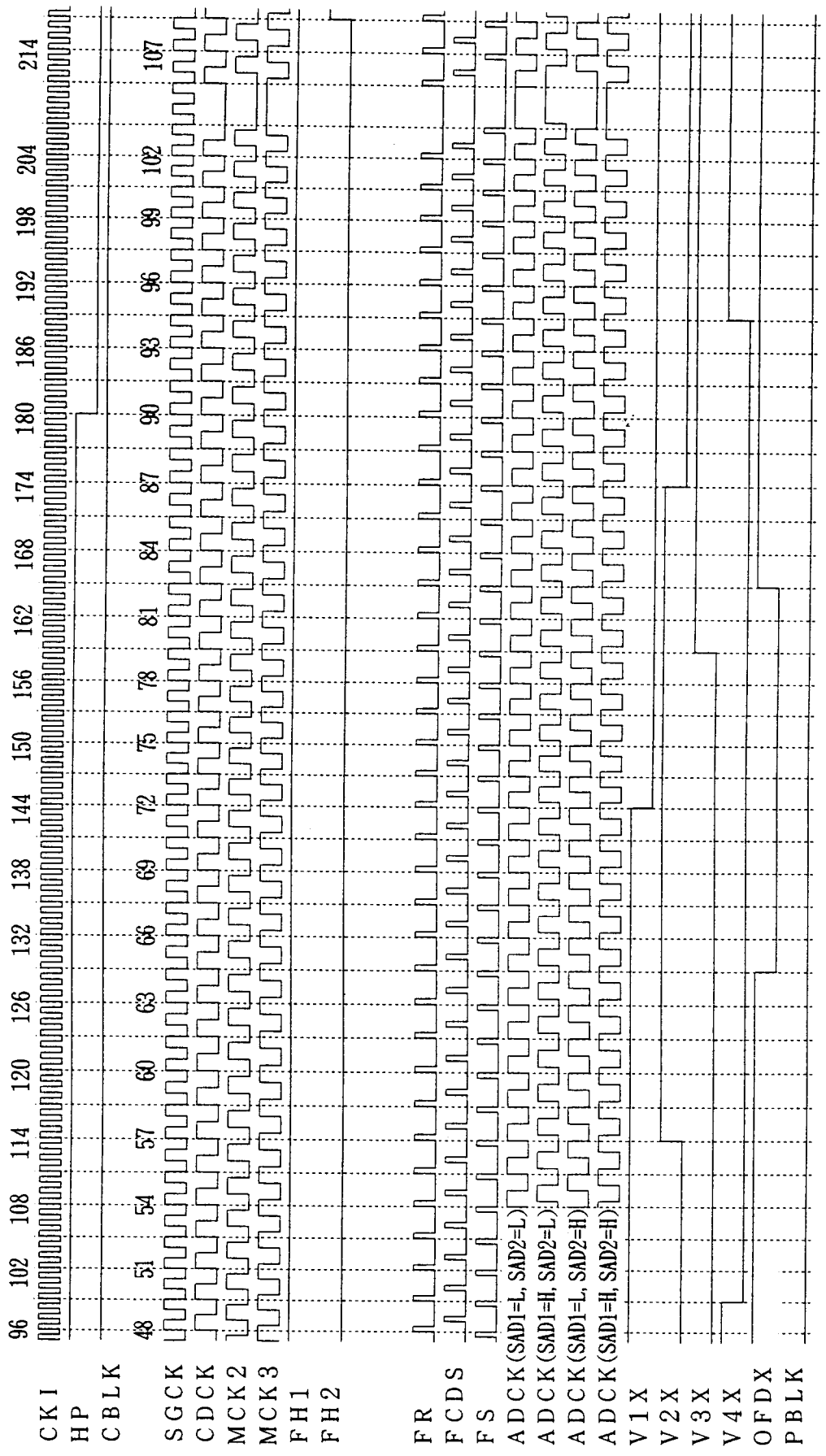
Horizontal pulse for driving CCD – 1 0
for 320K CCD (SCCD=L)

PAL (4)



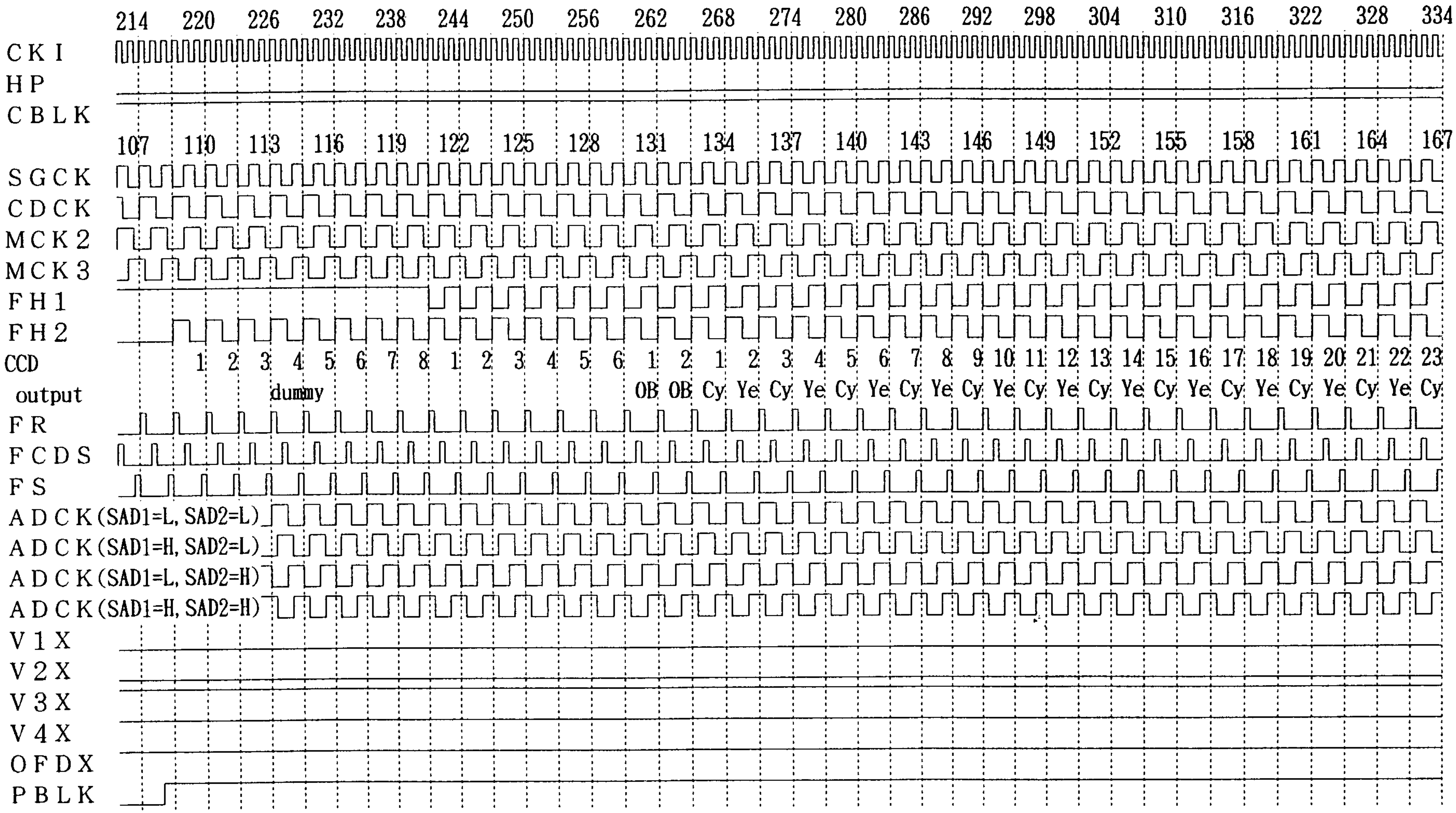
Horizontal pulse for driving CCD – 1 1
for 320K CCD (SCCD=L)

PAL (5)



Horizontal pulse for driving CCD －12
for 320K CCD (SCCD=L)
SAD1, SAD2=L

PAL (6)

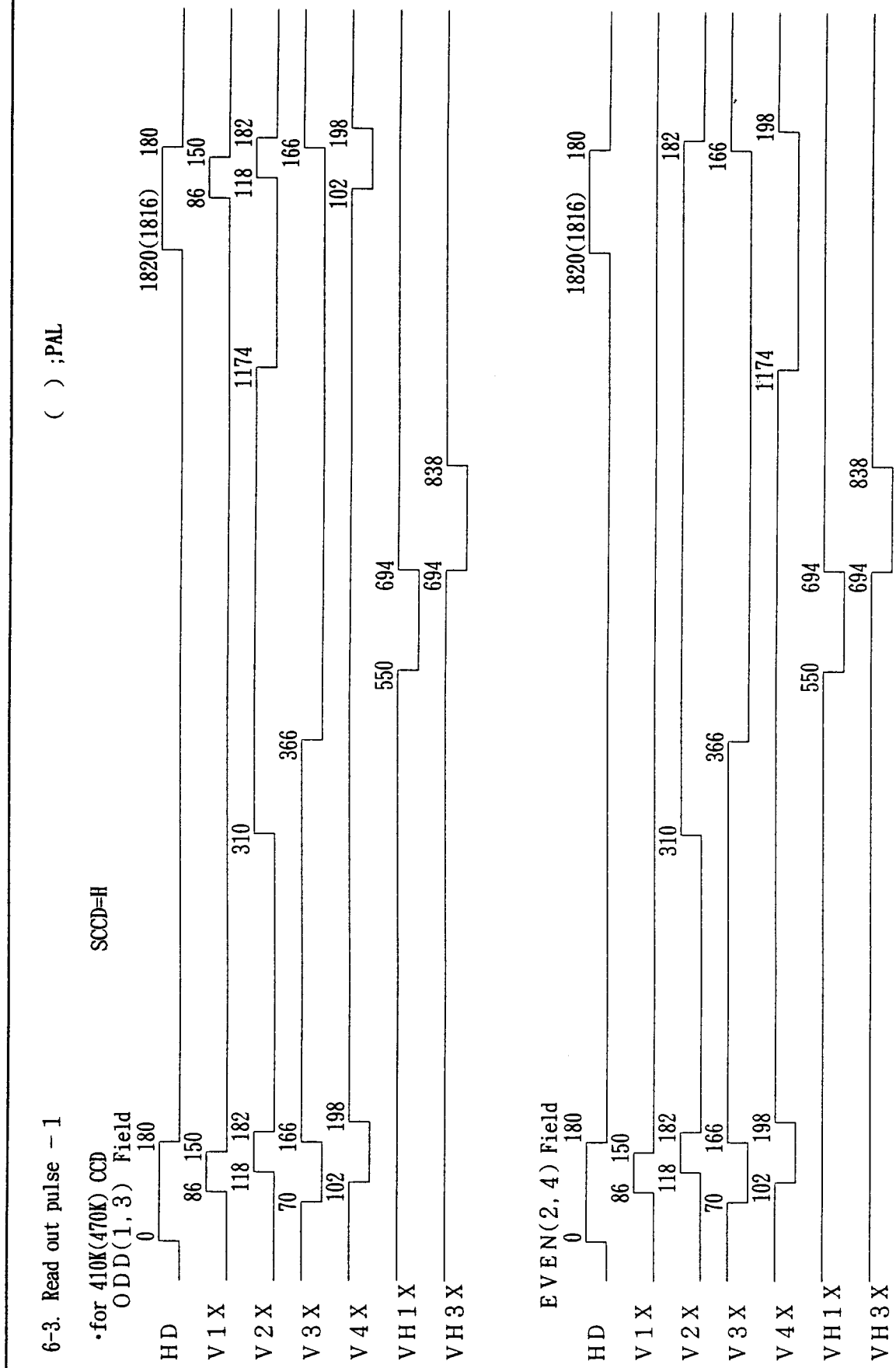


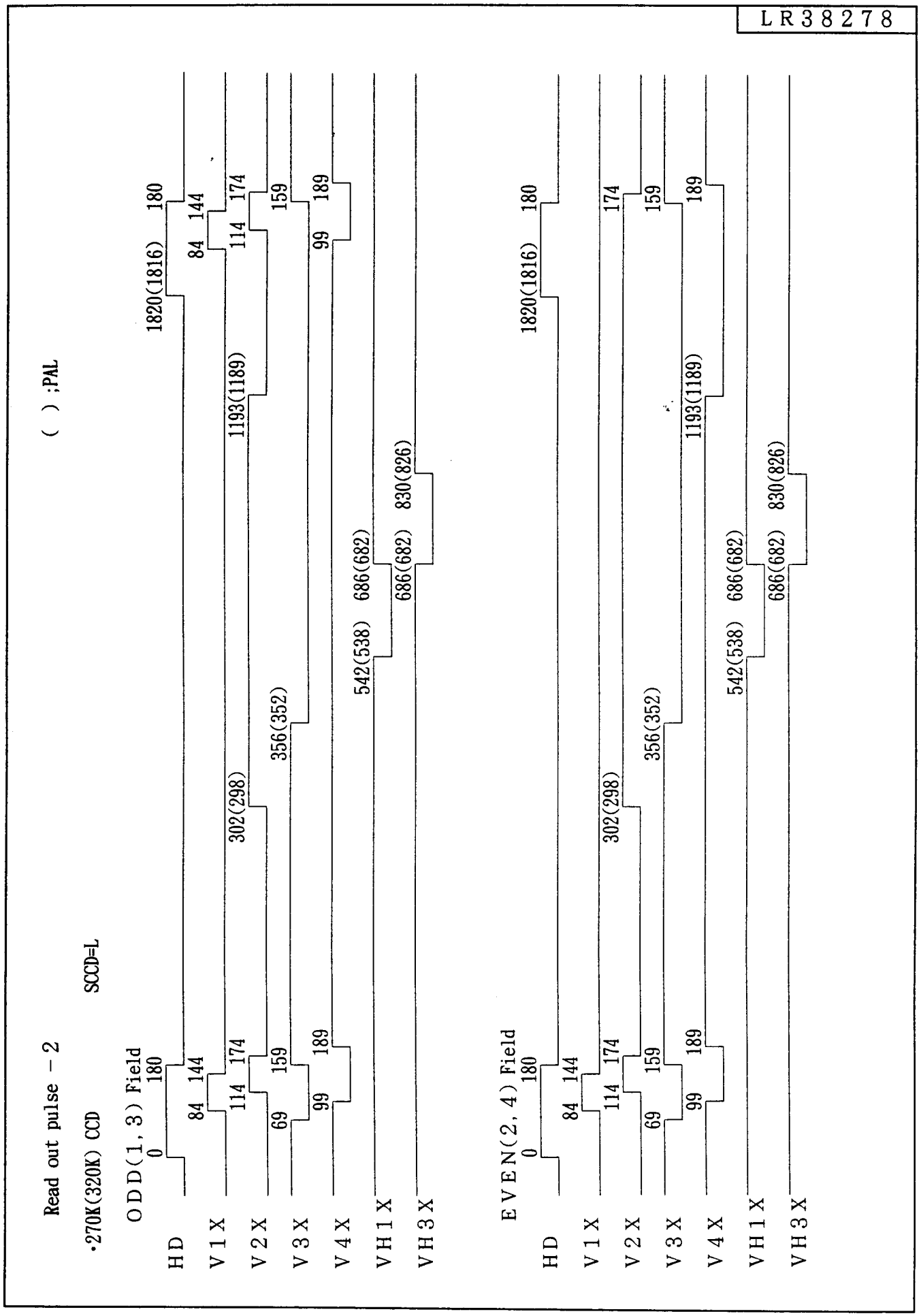
6-3. Read out pulse – 1

( ) ;PAL

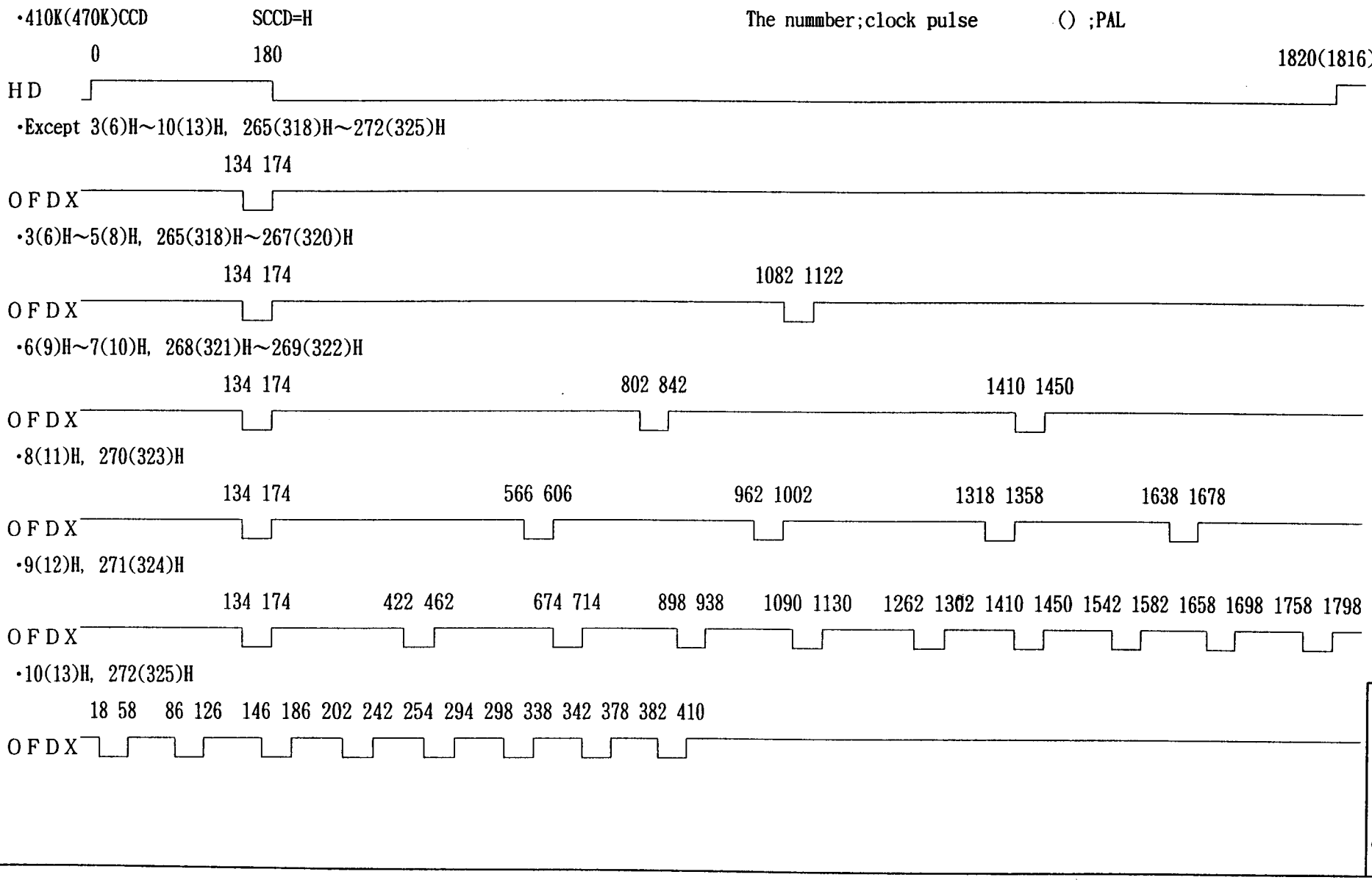
SCCD=H

・for 410K(470K) CCD

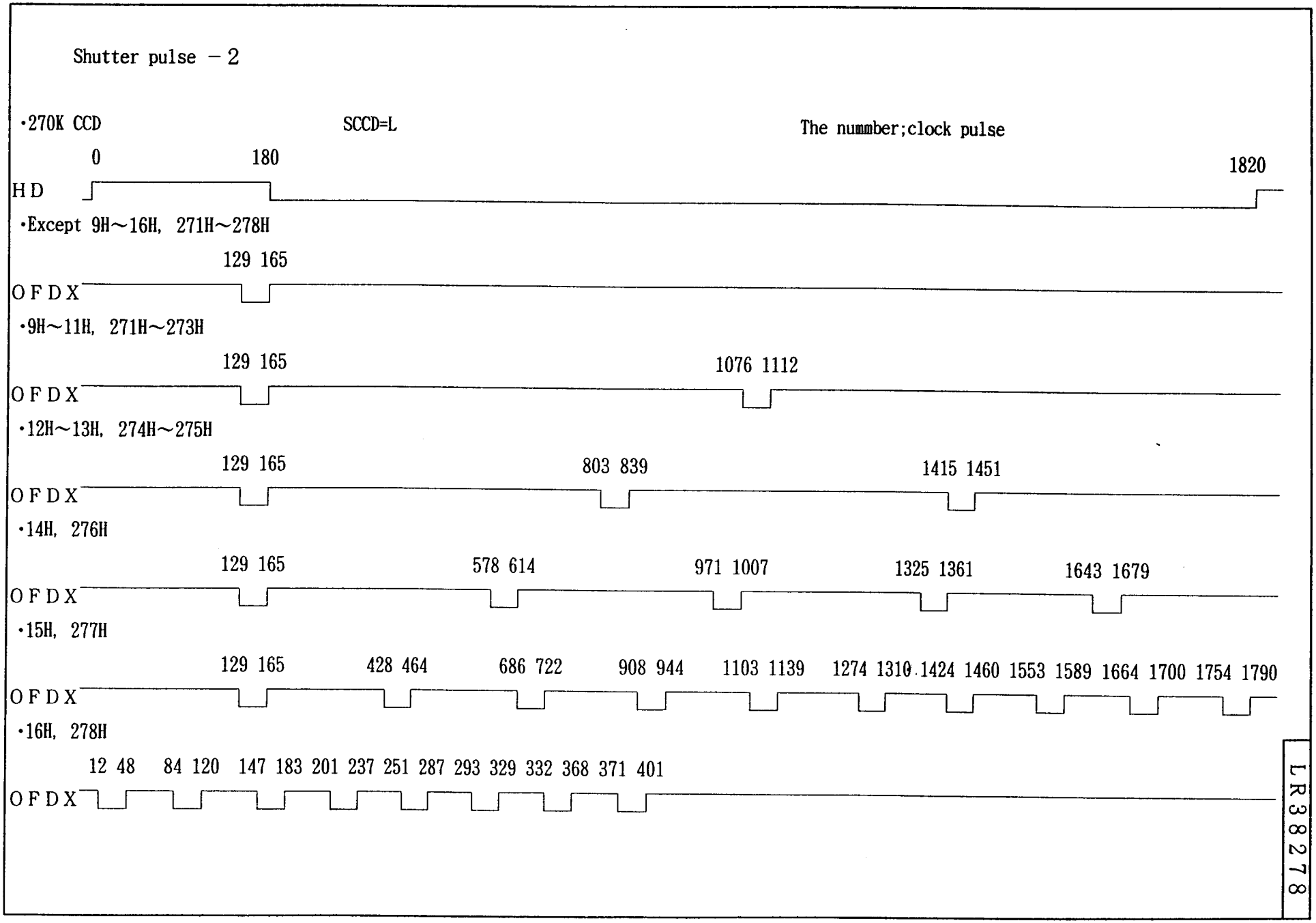



LR38278
Read out pulse – 2
( ) ;PAL
•270K(320K) CCD
SCCD=L
ODD(1, 3) Field
EVEN(2, 4) Field
HD
V1X
V2X
V3X
V4X
VH1X
VH3X
0
180
84
144
114
174
69
159
99
189
542(538)
686(682)
830(826)
1820(1816)
302(298)
356(352)
1193(1189)

6-4. Shutter pulse －1



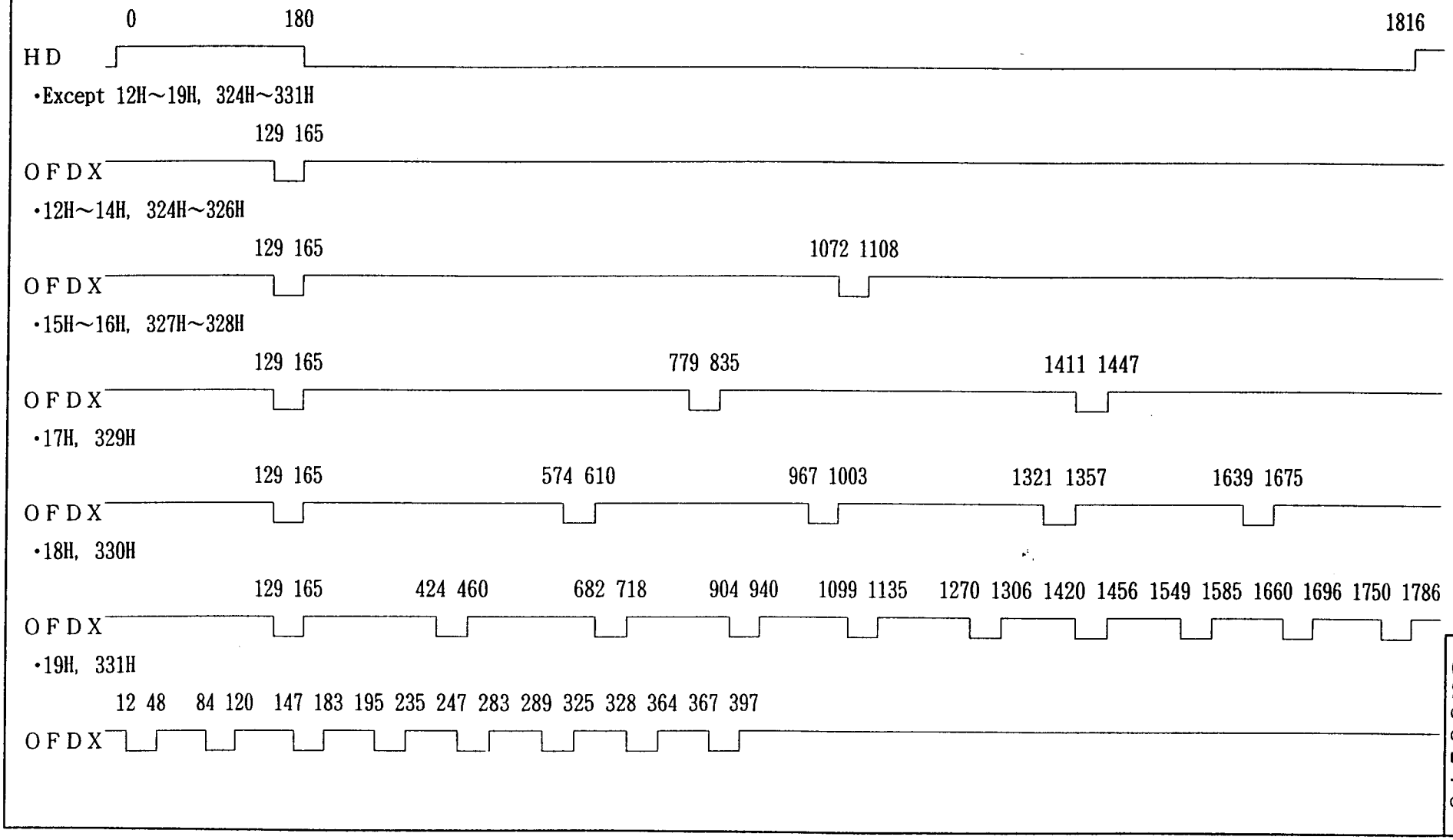
Shutter pulse − 2



LR38278

Shutter pulse − 3

•320K CCD　　SCCD=L　　The nummber;clock pulse



7 Package and packing specification

1. Package Outline Specification

Refer to drawing No.AA1035

2. Markings

2－1. Marking contents

(1) Product name : LR38278

(2) Company name : SHARP

(3) Date code

(Example) YY WW ×

- × → Denotes the production ref.code.
- WW → Denotes the production week. (01, 02, 03, ・・・・・52, 53)
- YY → Denotes the production year. (Lower two digits of the year.)

Indicates the product was manufactured in the WWth week of 19YY.

(4) The marking of "JAPAN" indicates the country of origin.

2－2. Marking layout

Refer to drawing No.AA1035

(This layout do not define the dimensions of marking character and marking position.)

3. Packing Specification

3－1. Packing materials

Material Name	Material Specification	Purpose
Tray	Conductive plastic (80devices/tray)	Fixing of device
Upper cover tray	Conductive plastic (1tray/case)	Fixing of device
Laminated aluminum bag	Aluminum polyethylene (1bag/case)	Drying of device
Desiccant	Silica gel	Drying of device
P P band	polypropylene (3 pcs/case)	Device tray fixing
Inner case	Card board (800devices/case)	Packaging of device
Label	Paper	Indicates part number, quantity and date of manufacture
Outer case	Cardboard	Outer packing of device case

(Devices shall be placed into a tray in the same direction.)

3－2. Outline dimension of tray

Refer to attached drawing

4. Precausion For Unpacking

(1) Unpacking should be done on the stand as well as human body treated with anti-ESD.

(2) Conductive treatment or anti-ESD treatment is given to a dray. Use the equivalent tray, if it is changed to another one.

5. Surface Mount Conditions

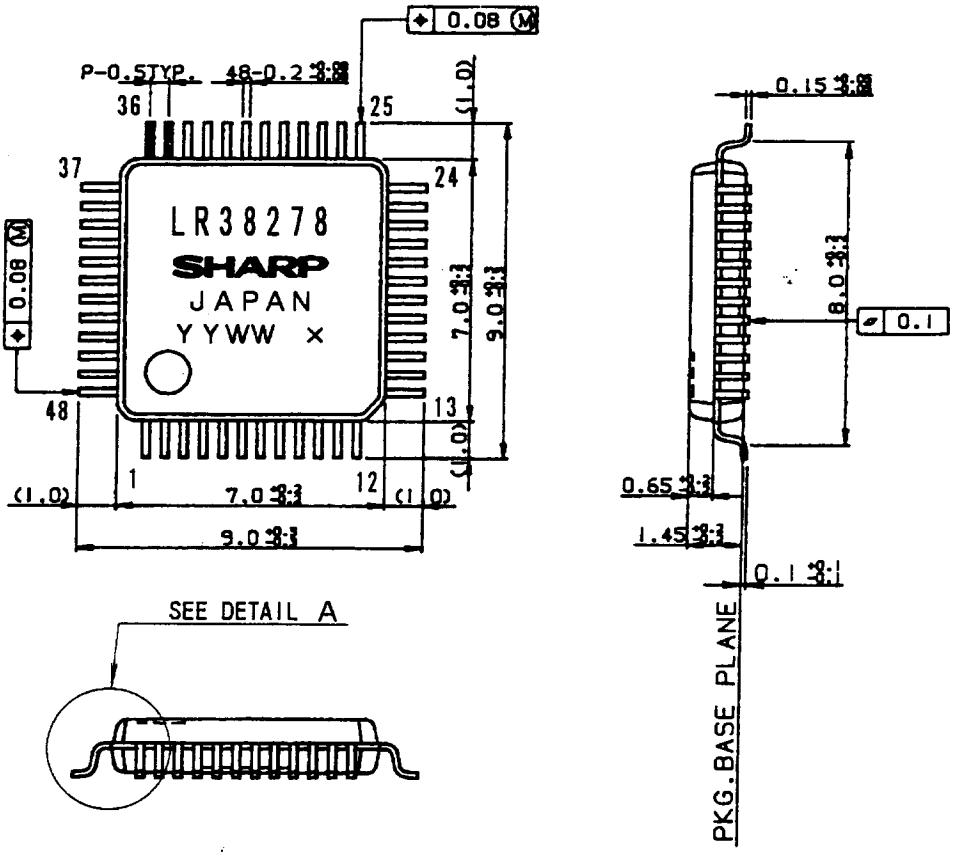
Please perform the following conditions when mounting ICs not to deteriorate IC quality.

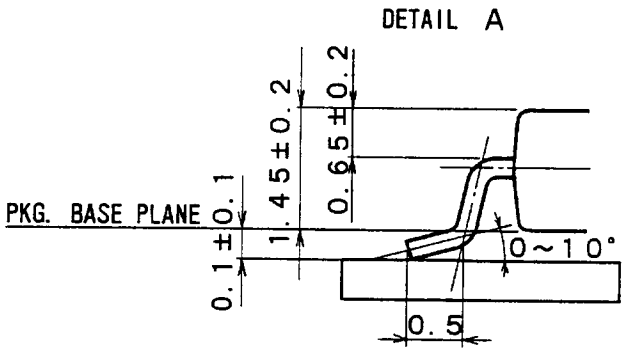
5－1.Soldering conditions(The following conditions are valid only for one time soldering.)

Mounting Method	Temperature and Duration	Measurement Point
Reflow soldering (air)	Peak temperature of 240℃, duration less than 15 seconds above 230℃, temperature increase rate of 1～4℃/second	IC surface
Vapor phase solderring	215℃ or less, duration less than 40 seconds above 200℃	Steam
Manual soldering (soldering iron)	260℃ or less, duration less than 10 seconds	IC outer lead surface

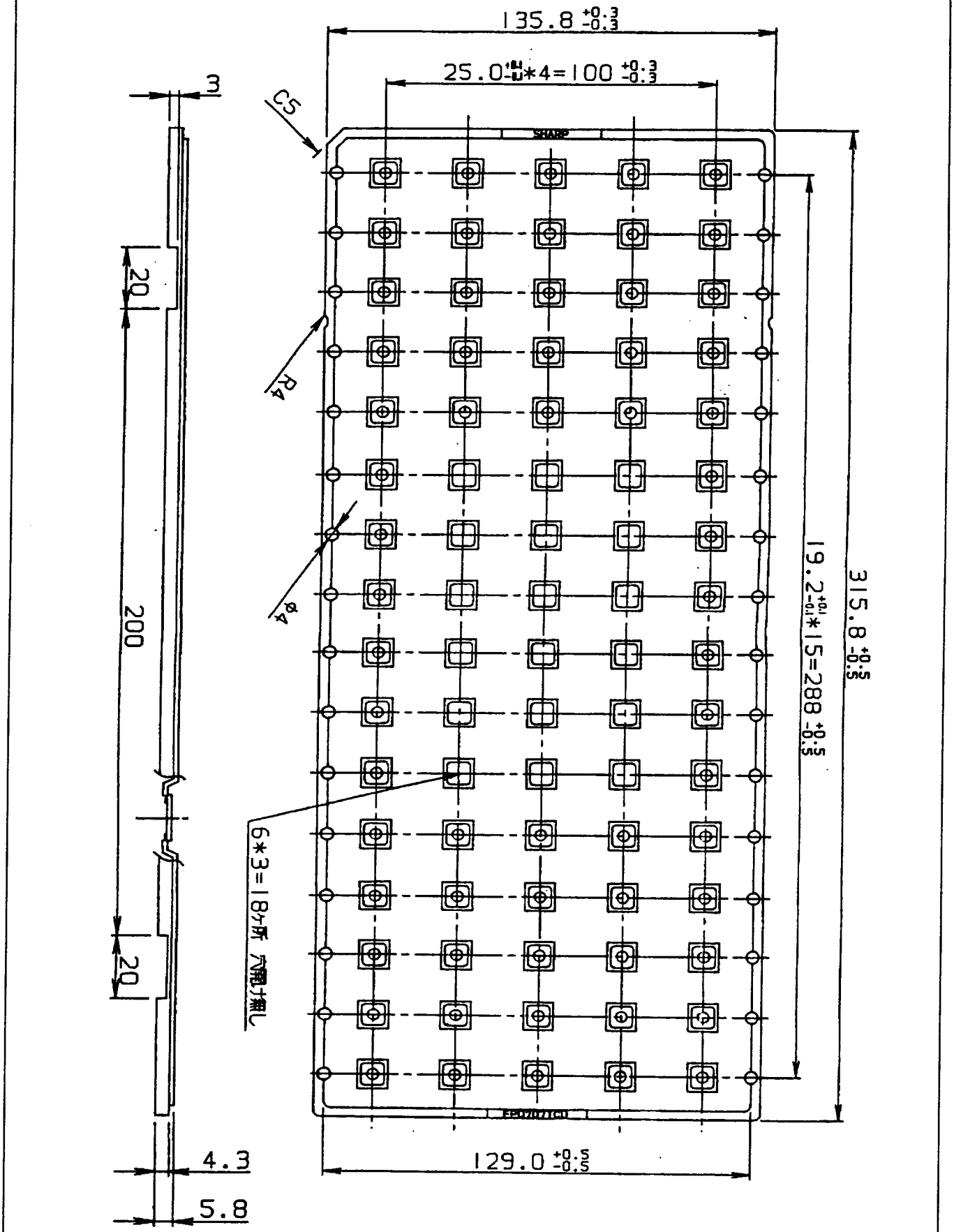
5－2. Conditions for removal of residual flux

(1) Ultrasonic washing power : 25 Watts/liter or less
(2) Washing time : Total 1 minute maximum
(3) Solvent temperature : 15～40℃





名称 NAME	QFP48-P-0707	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 NOTE プラスチックパッケージ外形寸法は、バリを含まないものとする。 Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1035	単位 UNIT	mm	



名称 NAME	FP0707TCD			備考 NOTE
DRAWING NO.	CV536	単位 UNIT	mm	