SHARP

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To ;

SPECIFICATIONS

Product Type Timing IC (Low Power 270K/320K pixels CCD)

Model No. LR38277

※This specifications contains 43 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

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LR38277

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  (1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
  - ·Office electronics
  - ·Instrumentation and measuring equipment
  - ·Machine tools
  - ·Audiovisual equipment
  - ·Home appliances
  - ·Communication equipment other than for trunk lines

  (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
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  - ·Mainframe computers
  - ·Traffic control systems
  - ·Gas leak detectors and automatic cutoff devices
  - ·Rescue and security equipment
  - ·Other safety devices and safety equipment, etc.

  (3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
  - ·Aerospace equipment
  - ·Communications equipment for trunk lines
  - ·Control equipment for the nuclear power industry
  - ·Medical equipment related to life support, etc.

  (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

- Please direct all queries regarding the products covered herein to a sales representative of the company.

CONTENTS

1. General

The LR38277 is a CMOS gate array LSI. It generates timing pulses for driving CCD area sensor, and signals and processing pulses for video signals.

1-1. Features

* The package material is plastic.
* A p-type silicon circuit board is used.
* The package type is 48-pin QFP (0.5mm pin-pitch)
* The process (structure) is CMOS.
* The delay time per 1 gate is 0.4ns.
* Not designed or rated as radiation hardened.

1-2. Functions

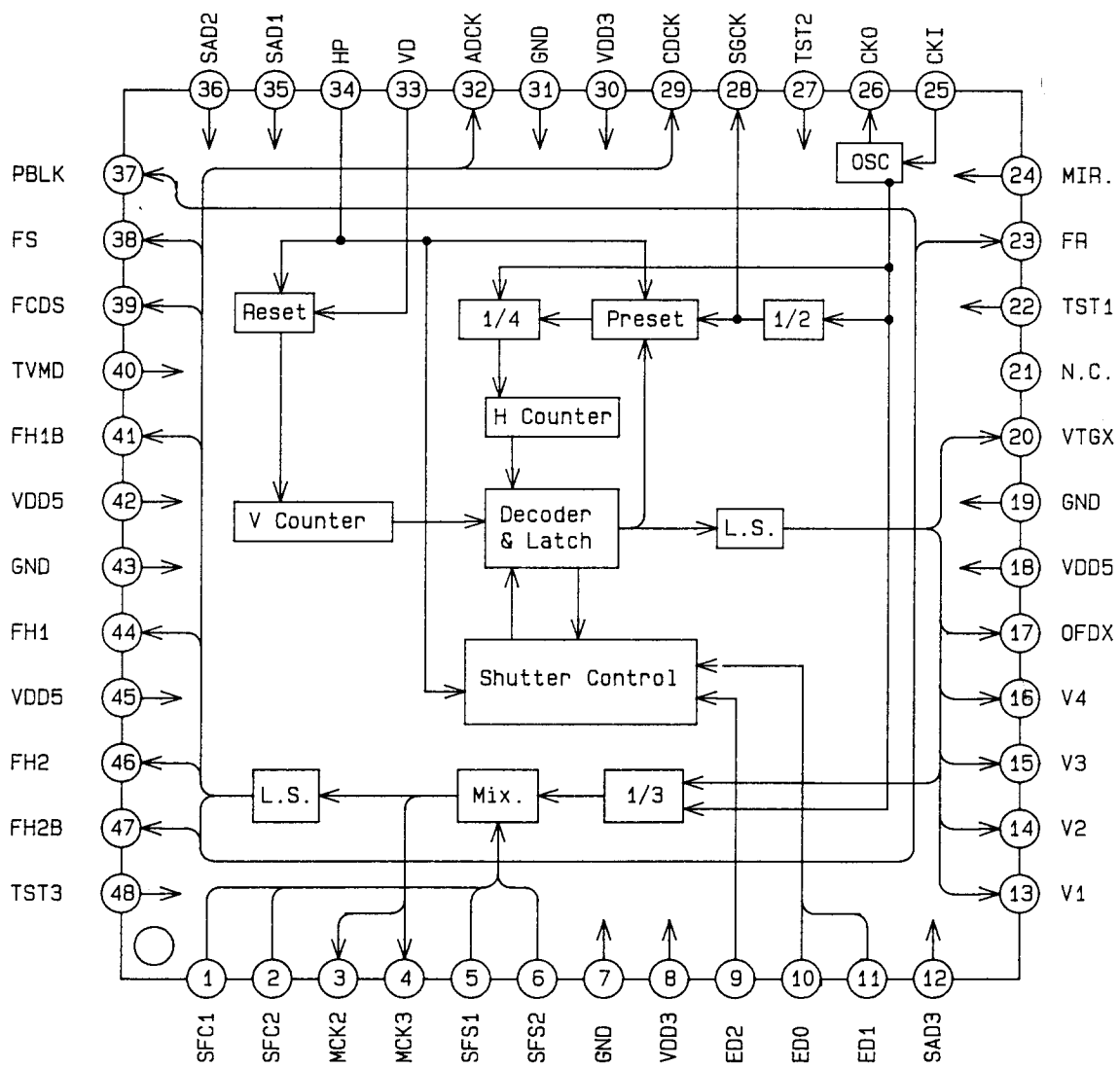
* Designed for Two-Power Supply CCD color area sensor with 270,000 or 320,000 pixels using with DSP-IC (LR38263).
* Switchable between NTSC and PAL mode.
* Mirror image control function is possible.
* +3.3V and +5V power supply.
* External shutter control function with serial data input is possible.

2. Pin Assignment

PIN NO.	I／O	SIGNAL	PIN NO.	I／O	SIGNAL
1	IC3	SFC1	25	OSCI3	CKI
2	IC3	SFC2	26	OSCO3	CKO
3	O6MA32	MCK2	27	ICD3	TST2
4	O6MA32	MCK3	28	O6MA32	SGCK
5	IC3	SFS1	29	O6MA32	CDCK
6	IC3	SFS2	30	–	VDD3
7	–	GND	31	–	GND
8	–	VDD3	32	O6MA32	ADCK
9	ICD3	ED2	33	IC3	VD
10	ICD3	ED0	34	IC3	HP
11	ICD3	ED1	35	ICU3	SAD1
12	ICU5	SAD3	36	ICU5	SAD2
13	O6MA52	V1	37	O5	PBLK
14	O6MA52	V2	38	O6MA5	FS
15	O6MA52	V3	39	O6MA5	FCDS
16	O6MA52	V4	40	ICU5	TVMD
17	O6MA5	OFDX	41	O6MA52	FH1B
18	–	VDD5	42	–	VDD5
19	–	GND	43	–	GND
20	O6MA5	VTGX	44	O6MA52	FH1
21	–	N.C.	45	–	VDD5
22	ICD5	TST1	46	O6MA52	FH2
23	O6MA52	FR	47	O6MA52	FH2B
24	ICD3	MIR	48	ICD3	TST3

IC3 : Input (CMOS level)
ICU3 : Input (CMOS level with pull-up resister)
ICD3 : Input (CMOS level with pull-down resister)
ICU5 : Input (CMOS level with pull-up resister)
ICD5 : Input (CMOS level with pull-down resister)
O6MA5 : Output
O6MA52 : Output
O6MA32 : Output
OSCI3 : Input pin for oscillation
OSCO3 : Output pin for oscillation

3. Block Diagram



4. Pin Description

No.	Symbol	I/O	Pol.	Pin Name	Description
1	SFC1	IC3	–	FCDS phase control input 1	An input pin to set the rising edge of FCDS(pin39) pulse output. To be connected to the signal from MCK2(pin3) output through the RC integral circuit.
2	SFC2	IC3	–	FCDS phase control input 2	An input pin to set the falling phase of FCDS(pin 39) pulse output. To be connected to the signal from MCK3(pin4) output through the RC integral circuit.
4	MCK2	O6MA 32	⨍⨍	Clock output 2	A pin to output 1/2 dividing pulse of reference clock CKI(pin 25). It is the same phase with FH1 (pin 44).
5	MCK3	O6MA 32	⨍⨍	Clock output 3	A pin to output 1/2 dividing pulse of reference clock CKI(pin 25). It is delayed by approximately 90° in phase with respect MCK2(pin 3).
5	SFS1	IC3	–	FS phase control input 1	An input pin to set the rising edge of FS(pin 38) pulse output. To be connected to the signal from MCK2(pin 4) output through the RC integral circuit.
6	SFS2	IC3	–	FS phase control input 2	An input pin to set the falling edge of FS(pin 38) pulse output. To be connected to the signal from MCK3(pin 5) output through the RC integral circuit.
7	GND	-	–	Ground	A grounding pin.
8	VDD3	-	–	Power supply	Supply +3.3V power.
9	ED2	ICD3	–	Strobe pulse input	An input pin for the strobe pulse to control the shutter speed. For details, see shutter control.
10	ED0	ICD3	–	Sift register Clock input	An input pin for the clock of shift register to control the shutter speed. For details, see shutter control.
11	ED1	ICD3	–	Serial Shutter Data input	An input pin for the data of serial shutter code to control the shutter speed. For details, see shutter control.
12	SAD3	ICU5	–	ADCK phase control input	Pins to control the phase of ADCK.
13	V1	O6MA 52	⨍	Ver. transfer pulse output #1	A vertical transfer pulse for CCD. To be connected to ϕV1 pin of CCD.
14	V2	O6MA 52	⨍	Ver. transfer pulse output #1	A vertical transfer pulse for CCD. To be connected to ϕV2 pin of CCD.
15	V3	O6MA 52	⨏	Ver. transfer pulse output #3	A vertical transfer pulse for CCD. To be connected to ϕV3 pin of CCD.
16	V4	O6MA 52	⨏	Ver. transfer pulse output #4	A vertical transfer pulse for CCD. To be connected to ϕV4 pin of CCD.

No.	Symbol	I/O	Pol.	Pin Name	Description
17	OFDX	O6MA5	⊓	Electronic shutter pulse output 1	A pulse that sweeps the charge of the photodiode for electrical shutter. Connect to OFD of CCD through the invert, level shift and DC offset circuit. Held at H level at normal mode.
18	VDD5	-	–	Power supply	Supply +5 V power.
19	GND	-	–	Ground	A grounding pin.
20	VTGX	O6MA5	⊓	Read-out pulse output	A pulse that transfers the charge of the photodiode to the vertical shift resister. Connect to VTG pin of CCD through the invert and level shift.
21	NC	–	–	(No-connect)	Non-connection.
22	TST1	ICD5	–	Test terminal 1	A test pin. Set open or to L level in the normal mode.
23	FR	O6MA 52	⊓	Reset pulse output	A reset pulse for CCD. To be connected to ϕR of CCD through the D.C. offset circuit.
24	NC	-	–	(No-connect)	Non-connection.
25	CKI	OSCI3	⊓⊓	Clock input	An input pin for reference clock oscillation. The frequencies are as follows : at NTSC mode : 28.63636MHz (1820fH) at PAL mode : 28.37500MHz (1816fH) fH=Hor. frequency
26	CKO	OSCO3	⊓⊓	Clock output	An output pin for reference clock oscillation. The output is the inverse CKI(pin 25).
27	TST2	ICD3	–	Test terminal 2	A test pin. Set open or to L level in the normal mode.
28	SGCK	O6MA 32	–	SSG clock output	A pulse for clock of SSG circuit. The frequencies are as follows : at NTSC mode : 14.31818MHz (910fH) at CCIR mode : 14.18750MHz (908fH)
29	CDCK	O6MA 32	–	DSP clock output	A pulse for clock of DSP-IC. The frequencies are as follows :
30	VDD3	-	–	Power supply	Supply +5 V power.
31	GND	-	–	Ground	A grounding pin.

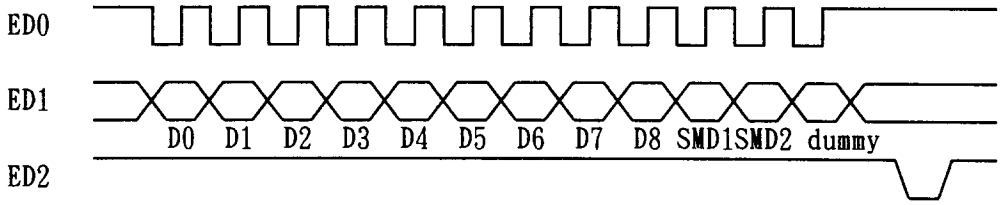
SCCD	L	H or open
NTSC mode	9.5035MHz (1820/3fH)	14.31818MHz (910fH)
PAL mode	9.4375MHz (1816/3fH)	14.18750MHz (908fH)

No.	Symbol	I/O	Pol.	Pin Name	Description
32	ADCK	O6MA 32	–	AD clock output	A pulse for clock of A/D converter. The frequencies are as follows : NTSC mode; 9.5035MHz (1820/3fH) PAL mode ; 9.4375MHz (1816/3fH) The phase of ADCK is selected by SAD1(pin35), SAD2(pin36) and SAD3(pin12).
33	VD	IC3	⎍	Ver. drive pulse	An input pin for the Vertical reference signal. To be connected to the DSP-IC.
34	HP	IC3	⎍	Hor. drive pulse	An input pin for the Horizontal reference signal. To be connected to the DSP-IC.
35	SAD1	ICU3	–	ADCK phase control input	Pins to control the phase of ADCK.
36	SAD2	ICU5	–		
37	PBLK	O5	⎍	Pre-blanking pulse output	A pulse that correspondes to the cease period of the horizontal transfer pulse.
38	FS	O6MA5	⎍	CDS pulse 2	A pulse to sample-hold the signal from CCD. Generated by SFS1(pin 5) and SFS2(pin 6).
39	FCDS	O6MA5	⎍	CDS pulse 1	A pulse to clamp the feed-through level from CCD. Generated by SFC1(pin 1) and SFC2(pin 2).
40	TVMD	ICU5	–	TV mode select	An input pin to select TV standards. L level ; NTSC mode H level or open : PAL mode
41	FH1B	O6MA 52	⎍⎍	Hor. transfer pulse 1B	A horizontal transfer pulse for CCD. To be connected to ϕH1B of CCD.
42	VDD5	–	–	Power supply	Supply +5 V power.
43	GND	–	–	Ground	A grounding pin.
44	FH1	O6MA 52	⎍⎍	Hor. transfer pulse 1	A horizontal transfer pulse for CCD. To be connected to ϕH1 of CCD.
45	VDD5	–	–	Power supply	Supply +5 V power.
46	FH2	O6MA 52	⎍⎍	Hor. transfer pulse 2	A horizontal transfer pulse for CCD. To be connected to ϕH2 of CCD.
46	FH2B	O6MA 52	⎍⎍	Hor. transfer pulse 2B	A horizontal transfer pulse for CCD. To be connected to ϕH2B of CCD.
48	TST3	ICD3	–	Test terminal 3	A test pin. Set open or to L level in the normal mode.

SAD1	SAD2	SAD3	ADCK
L	L	L	0°
H	L	L	delayed 60°
L	H	L	delayed 120°
H	H	L	delayed 180°
L	L	H	delayed 240°
H	L	H	delayed 300°

4-2. Shutter Speed Contorol.

(1) Timing of Serial Data input



The data of shutter speed is latched by the rising edge of HP, wich horizontal line number is in VTGX output.

(2) Table of the serial shutter data

Serial Data													Exposure Period(H)	
D0	D1	D2	D3	D4	D5	D6	D7	D8	SMD1	SMD2	dummy	n	NTSC	PAL
×	×	×	×	×	×	×	×	×	H	H	×	–	262H, 263H	312H, 312H
×	×	×	×	×	×	×	×	×	L	L	×	–	157H+A	260H+B
×	×	×	×	×	×	×	×	×	H	L	×	–	INHIBIT	INHIBIT
L	L	L	L	L	L	L	L	L	L	H	×	–	INHIBIT	INHIBIT
H	L	L	L	L	L	L	L	L	L	H	×	1	261H+A	311H+B
L	H	L	L	L	L	L	L	L	L	H	×	2	260H+A	310H+B
H	H	L	L	L	L	L	L	L	L	H	×	3	259H+A	309H+B
L	L	H	L	L	L	L	L	L	L	H	×	4	258H+A	308H+B
H	L	H	L	L	L	L	L	L	L	H	×	5	257H+A	307H+B
L	H	H	L	L	L	L	L	L	L	H	×	6	256H+A	306H+B
H	H	H	L	L	L	L	L	L	L	H	×	7	255H+A	305H+B
L	L	L	H	L	L	L	L	L	L	H	×	8	254H+A	304H+B
H	L	L	H	L	L	L	L	L	L	H	×	9	253H+A	303H+B
L	H	L	H	L	L	L	L	L	L	H	×	10	252H+A	302H+B
H	H	L	H	L	L	L	L	L	L	H	×	11	251H+A	301H+B
L	L	H	H	L	L	L	L	L	L	H	×	12	250H+A	300H+B
H	L	H	H	L	L	L	L	L	L	H	×	13	249H+A	299H+B
L	H	H	H	L	L	L	L	L	L	H	×	14	248H+A	298H+B
H	H	H	H	L	L	L	L	L	L	H	×	15	247H+A	297H+B
L	L	L	L	H	L	L	L	L	L	H	×	16	246H+A	296H+B
H	L	L	L	H	L	L	L	L	L	H	×	17	245H+A	295H+B
⟆	⟆	⟆	⟆	⟆	⟆	⟆	⟆	⟆	⟆	H	×	⟆	⟆	⟆
L	L	H	L	H	H	H	H	L	L	H	×	244	18H+A	68H+B
H	L	H	L	H	H	H	H	L	L	H	×	245	17H+A	67H+B
L	H	H	L	H	H	H	H	L	L	H	×	246	16H+A	66H+B
H	H	H	L	H	H	H	H	L	L	H	×	247	15H+A	65H+B
L	L	L	H	H	H	H	H	L	L	H	×	248	14H+A	64H+B
H	L	L	H	H	H	H	H	L	L	H	×	249	13H+A	63H+B
L	H	L	H	H	H	H	H	L	L	H	×	250	12H+A	62H+B
H	H	L	H	H	H	H	H	L	L	H	×	251	11H+A	61H+B
L	L	H	H	H	H	H	H	L	L	H	×	252	10H+A	60H+B
H	L	H	H	H	H	H	H	L	L	H	×	253	9H+A	59H+B

Serial Data												n	Exposure Period(H)	
D0	D1	D2	D3	D4	D5	D6	D7	D8	SMD1	SMD2	dummy		NTSC	PAL
L	H	H	H	H	H	H	H	L	L	H	×	254	8H+A	58H+B
H	H	H	H	H	H	H	H	L	L	H	×	255	7H+A	57H+B
L	L	L	L	L	L	L	L	H	L	H	×	256	6.85H	56H+B
H	L	L	L	L	L	L	L	H	L	H	×	257	6H+A	55H+B
L	H	L	L	L	L	L	L	H	L	H	×	258	5.85H	54H+B
H	H	L	L	L	L	L	L	H	L	H	×	259	5H+A	53H+B
L	L	H	L	L	L	L	L	H	L	H	×	260	4.85H	52H+B
H	L	H	L	L	L	L	L	H	L	H	×	261	4H+A	51H+B
L	H	H	L	L	L	L	L	H	L	H	×	262	4.01H	50H+B
H	H	H	L	L	L	L	L	H	L	H	×	263	3.67H	49H+B
L	L	L	H	L	L	L	L	H	L	H	×	264	3H+A	48H+B
H	L	L	H	L	L	L	L	H	L	H	×	265	3.01H	47H+B
L	H	L	H	L	L	L	L	H	L	H	×	266	2.67H	46H+B
H	H	L	H	L	L	L	L	H	L	H	×	267	2H+A	45H+B
L	L	H	H	L	L	L	L	H	L	H	×	268	2.16H	44H+B
H	L	H	H	L	L	L	L	H	L	H	×	269	1.95H	43H+B
L	H	H	H	L	L	L	L	H	L	H	×	270	1.74H	42H+B
H	H	H	H	L	L	L	L	H	L	H	×	271	1.55H	41H+B
L	L	L	L	H	L	L	L	H	L	H	×	272	1H+A	40H+B
H	L	L	L	H	L	L	L	H	L	H	×	273	1,20H	39H+B
L	H	L	L	H	L	L	L	H	L	H	×	274	1.05H	38H+B
H	H	L	L	H	L	L	L	H	L	H	×	275	0.92H	37H+B
L	L	H	L	H	L	L	L	H	L	H	×	276	0.80H	36H+B
H	L	H	L	H	L	L	L	H	L	H	×	277	0.70H	35H+B
L	H	H	L	H	L	L	L	H	L	H	×	278	0.61H	34H+B
H	H	H	L	H	L	L	L	H	L	H	×	279	0.54H	33H+B
L	L	L	H	H	L	L	L	H	L	H	×	280	0.47H	32H+B
H	L	L	H	H	L	L	L	H	L	H	×	281	0.41H	31H+B
L	H	L	H	H	L	L	L	H	L	H	×	282	0.36H	30H+B
H	H	L	H	H	L	L	L	H	L	H	×	283	0.32H	29H+B
L	L	H	H	H	L	L	L	H	L	H	×	284	0.28H	28H+B
H	L	H	H	H	L	L	L	H	L	H	×	285	0.24H	27H+B
L	H	H	H	H	L	L	L	H	L	H	×	286	0.22H	26H+B
H	H	H	H	H	L	L	L	H	L	H	×	287	0.20H	25H+B
L	L	L	L	L	H	L	L	H	L	H	×	288	0.17H	24H+B
H	L	L	L	L	H	L	L	H	L	H	×	289	INHIBIT	23H+B
L	H	L	L	L	H	L	L	H	L	H	×	290	INHIBIT	22H+B
H	H	L	L	L	H	L	L	H	L	H	×	291	INHIBIT	21H+B
L	L	H	L	L	H	L	L	H	L	H	×	292	INHIBIT	20H+B
H	L	H	L	L	H	L	L	H	L	H	×	293	INHIBIT	19H+B
L	H	H	L	L	H	L	L	H	L	H	×	294	INHIBIT	18H+B
H	H	H	L	L	H	L	L	H	L	H	×	295	INHIBIT	17H+B
L	L	L	H	L	H	L	L	H	L	H	×	296	INHIBIT	16H+B
H	L	L	H	L	H	L	L	H	L	H	×	297	INHIBIT	15H+B
L	H	L	H	L	H	L	L	H	L	H	×	298	INHIBIT	14H+B

Serial Data													Exposure Period(H)	
D0	D1	D2	D3	D4	D5	D6	D7	D8	SMD1	SMD2	dummy	n	NTSC	PAL
H	H	L	H	L	H	L	L	H	L	H	×	299	INHIBIT	13H+B
L	L	H	H	L	H	L	L	H	L	H	×	300	INHIBIT	12H+B
H	L	H	H	L	H	L	L	H	L	H	×	301	INHIBIT	11H+B
L	H	H	H	L	H	L	L	H	L	H	×	302	INHIBIT	10H+B
H	H	H	H	L	H	L	L	H	L	H	×	303	INHIBIT	9H+B
L	L	L	L	H	H	L	L	H	L	H	×	304	INHIBIT	8H+B
H	L	L	L	H	H	L	L	H	L	H	×	305	INHIBIT	7H+B
L	H	L	L	H	H	L	L	H	L	H	×	306	INHIBIT	6.85H
H	H	L	L	H	H	L	L	H	L	H	×	307	INHIBIT	6H+B
L	L	H	L	H	H	L	L	H	L	H	×	308	INHIBIT	5.85H
H	L	H	L	H	H	L	L	H	L	H	×	309	INHIBIT	5H+B
L	H	H	L	H	H	L	L	H	L	H	×	310	INHIBIT	4.85H
H	H	H	L	H	H	L	L	H	L	H	×	311	INHIBIT	4H+B
L	L	L	H	H	H	L	L	H	L	H	×	312	INHIBIT	4.06H
H	L	L	H	H	H	L	L	H	L	H	×	313	INHIBIT	3.67H
L	H	L	H	H	H	L	L	H	L	H	×	314	INHIBIT	3H+B
H	H	L	H	H	H	L	L	H	L	H	×	315	INHIBIT	3.06H
L	L	H	H	H	H	L	L	H	L	H	×	316	INHIBIT	2.67H
H	L	H	H	H	H	L	L	H	L	H	×	317	INHIBIT	2H+B
L	H	H	H	H	H	L	L	H	L	H	×	318	INHIBIT	2.16H
H	H	H	H	H	H	L	L	H	L	H	×	319	INHIBIT	1.95H
L	L	L	L	L	L	H	L	H	L	H	×	320	INHIBIT	1.74H
H	L	L	L	L	L	H	L	H	L	H	×	321	INHIBIT	1.55H
L	H	L	L	L	L	H	L	H	L	H	×	322	INHIBIT	1H+B
H	H	L	L	L	L	H	L	H	L	H	×	323	INHIBIT	1.20H
L	L	H	L	L	L	H	L	H	L	H	×	324	INHIBIT	1.05H
H	L	H	L	L	L	H	L	H	L	H	×	325	INHIBIT	0.92H
L	H	H	L	L	L	H	L	H	L	H	×	326	INHIBIT	0.80H
H	H	H	L	L	L	H	L	H	L	H	×	327	INHIBIT	0.70H
L	L	L	H	L	L	H	L	H	L	H	×	328	INHIBIT	0.61H
H	L	L	H	L	L	H	L	H	L	H	×	329	INHIBIT	0.53H
L	H	L	H	L	L	H	L	H	L	H	×	330	INHIBIT	0.47H
H	H	L	H	L	L	H	L	H	L	H	×	331	INHIBIT	0.41H
L	L	H	H	L	L	H	L	H	L	H	×	332	INHIBIT	0.36H
H	L	H	H	L	L	H	L	H	L	H	×	333	INHIBIT	0.32H
L	H	H	H	L	L	H	L	H	L	H	×	334	INHIBIT	0.28H
H	H	H	H	L	L	H	L	H	L	H	×	335	INHIBIT	0.25H
L	L	L	L	H	L	H	L	H	L	H	×	336	INHIBIT	0.22H
H	L	L	L	H	L	H	L	H	L	H	×	337	INHIBIT	0.10H
L	H	L	L	H	L	H	L	H	L	H	×	338	INHIBIT	0.17H
H	H	L	L	H	L	H	L	H	L	H	×	339	INHIBIT	INHIBIT
L	L	H	L	H	L	H	L	H	L	H	×	340	INHIBIT	INHIBIT
H	L	H	L	H	L	H	L	H	L	H	×	341	INHIBIT	INHIBIT
∫	∫	∫	∫	∫	∫	∫	∫	∫	L	H	×	∫	INHIBIT	INHIBIT
H	H	H	H	H	H	H	H	H	L	H	×	511	INHIBIT	INHIBIT

A = B ≒ 0.37H

5. Electrical Characteristics

5-1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD3}, V_{DD5}	−0.3 ~ 6.0	V
Input voltage	V_{I3}	−0.3 ~ V_{DD3}+0.3	V
Input voltage	V_{I5}	−0.3 ~ V_{DD5}+0.3	V
Output voltage	V_{O3}	−0.3 ~ V_{DD3}+0.3	V
Output voltage	V_{O5}	−0.3 ~ V_{DD5}+0.3	V
Operation temperature	Topr	−20 ~ +70	℃
Storage temperature	Tstg	−55 ~ +150	℃

5-2. DC Characteristics (V_{DD3}=+3.3V±10%, V_{DD5}=+5V±10%, Topr=-20~+70℃)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Note
Input "High" voltage	V_{IH3}		0.7×V_{DD5}			V	1, 2, 3
Input "Low" voltage	V_{IL3}				0.3×V_{DD5}	V	
Input "High" voltage	V_{IH5}		3.5			V	4, 5
Input "Low" voltage	V_{IL5}				1.5	V	
Input "High" current	$\|I_{IH3-1}\|$	V_I = V_{DD3}			1.0	μA	1
	$\|I_{IH3-2}\|$	V_I = V_{DD3}	3.0		30	μA	2
	$\|I_{IH3-3}\|$	V_I = V_{DD3}			2.0	μA	3
Input "Low" current	$\|I_{IL3-1}\|$	V_I = 0 V			1.0	μA	1
	$\|I_{IL3-2}\|$	V_I = 0 V			2.0	μA	2
	$\|I_{IL3-3}\|$	V_I = 0 V	3.0		30	μA	3
Input "High" current	$\|I_{IH5-1}\|$	V_I = V_{DD5}			2.0	μA	4
	$\|I_{IH5-2}\|$	V_I = V_{DD5}	8.0		60	μA	5
Input "Low" current	$\|I_{IL5-1}\|$	V_I = 0 V	8.0		60	μA	4
	$\|I_{IL5-2}\|$	V_I = 0 V			2.0	μA	5
Output "High" voltage	V_{OH3-1}	I_{OH}= 2 mA	V_{DD3}-0.5			V	6
Output "Low" voltage	V_{OL3-1}	I_{OL}= 2 mA			0.4	V	
Output "High" voltage	V_{OH3-2}	I_{OH}= −6 mA	V_{DD3}-0.5			V	7
Output "Low" voltage	V_{OL3-2}	I_{OL}= 6 mA			0.4	V	
Output "High" voltage	V_{OH5-1}	I_{OH}= −6 mA	V_{DD5}-0.5			V	8
Output "Low" voltage	V_{OL5-1}	I_{OL}= 6 mA			0.4	V	
Output "High" voltage	V_{OH5-2}	I_{OH}= −12 mA	V_{DD5}-0.5			V	9
Output "Low" voltage	V_{OL5-2}	I_{OL}= 12 mA			0.4	V	

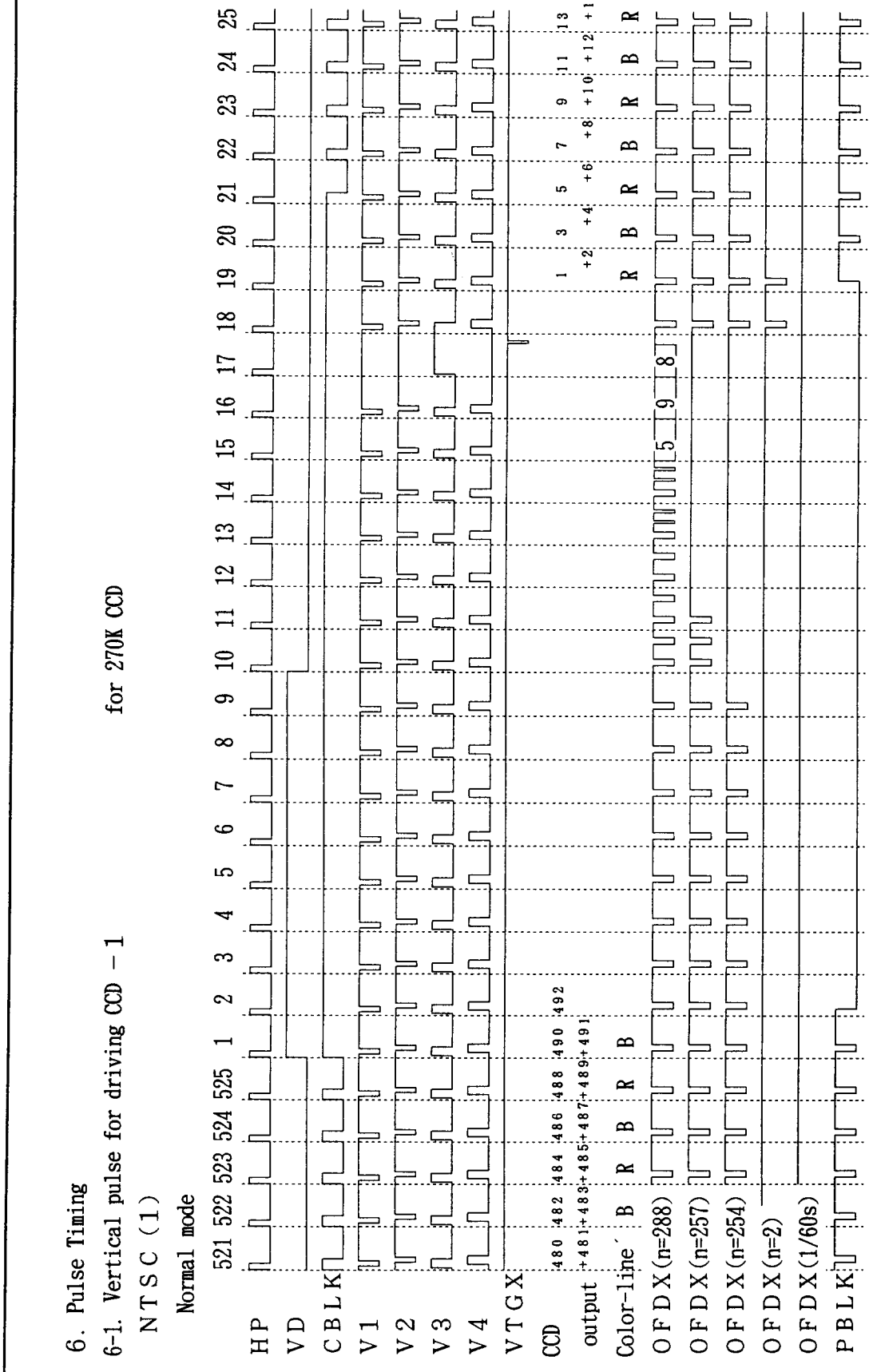
Note 1 : Applied to Inputs (IC3, OSCI3)
Note 2 : Applied to Input (ICD3).
Note 3 : Applied to Input (ICU3).
Note 4 : Applied to Input (ICU5).
Note 5 : Applied to Input (ICD5).
Note 6 : Applied to Output (OSCO3).
(Output(OSCO3) measures on conditions that input(OSCI3) level is 0V or V_{DD3}.)
Note 7 : Applied to Output(O6MA32).
Note 8 : Applied to Output(O6MA5).
Note 9 : Applied to Output(O6MA52).

6. Pulse Timing

6-1. Vertical pulse for driving CCD – 1 for 270K CCD

NTSC (1)

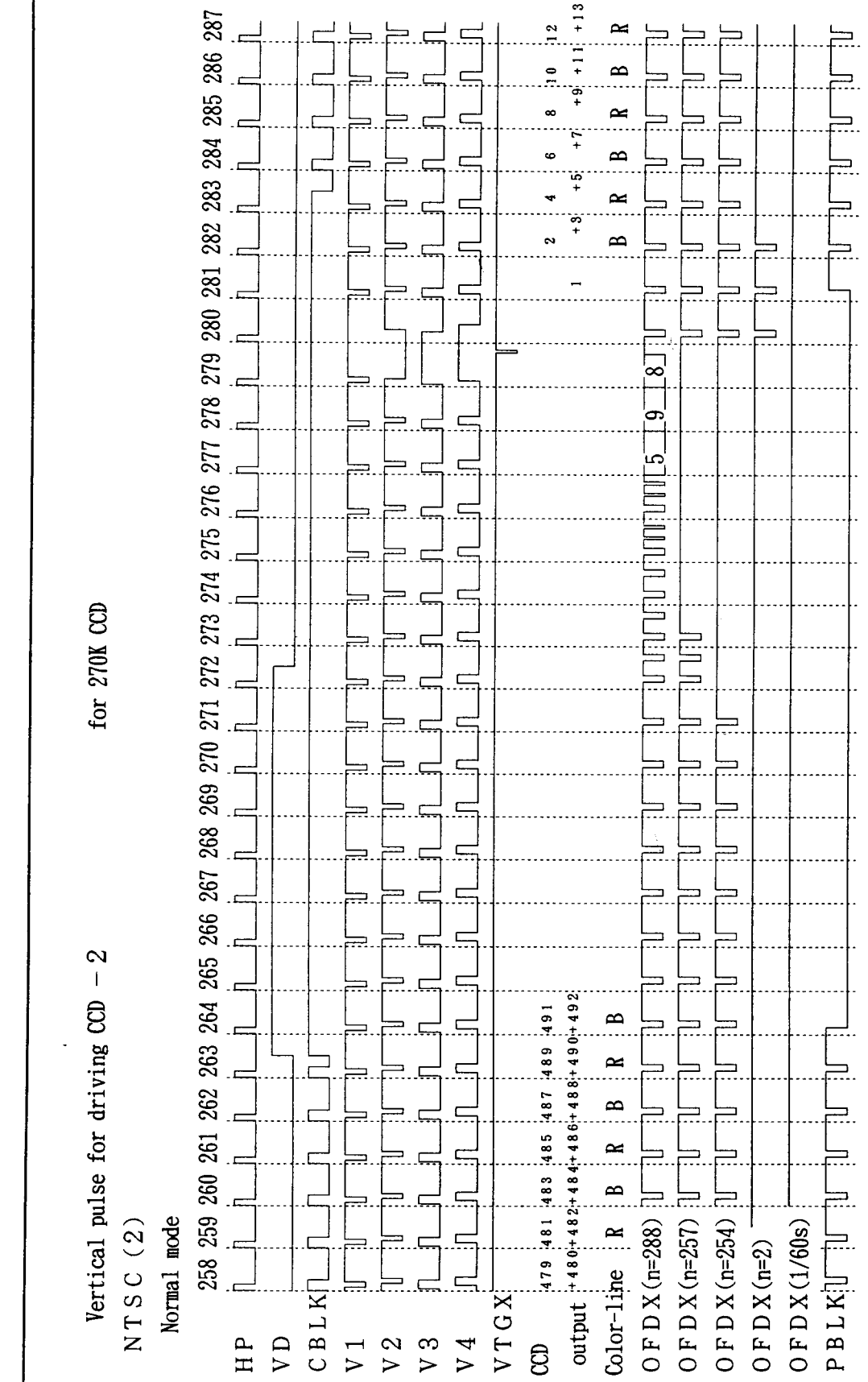
Normal mode



Vertical pulse for driving CCD – 2 for 270K CCD

NTSC (2)

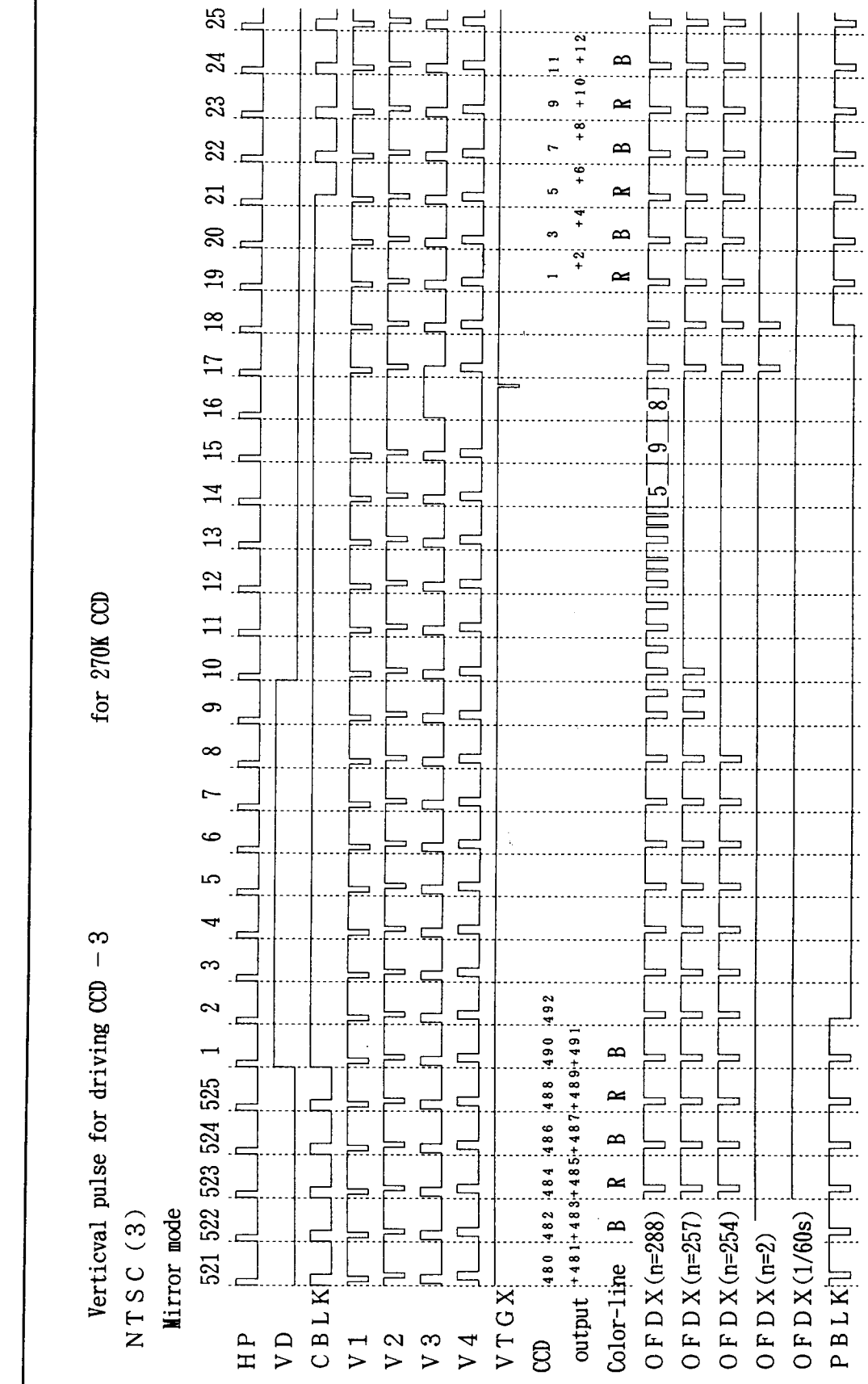
Normal mode



Verticval pulse for driving CCD – 3 for 270K CCD

NTSC (3)

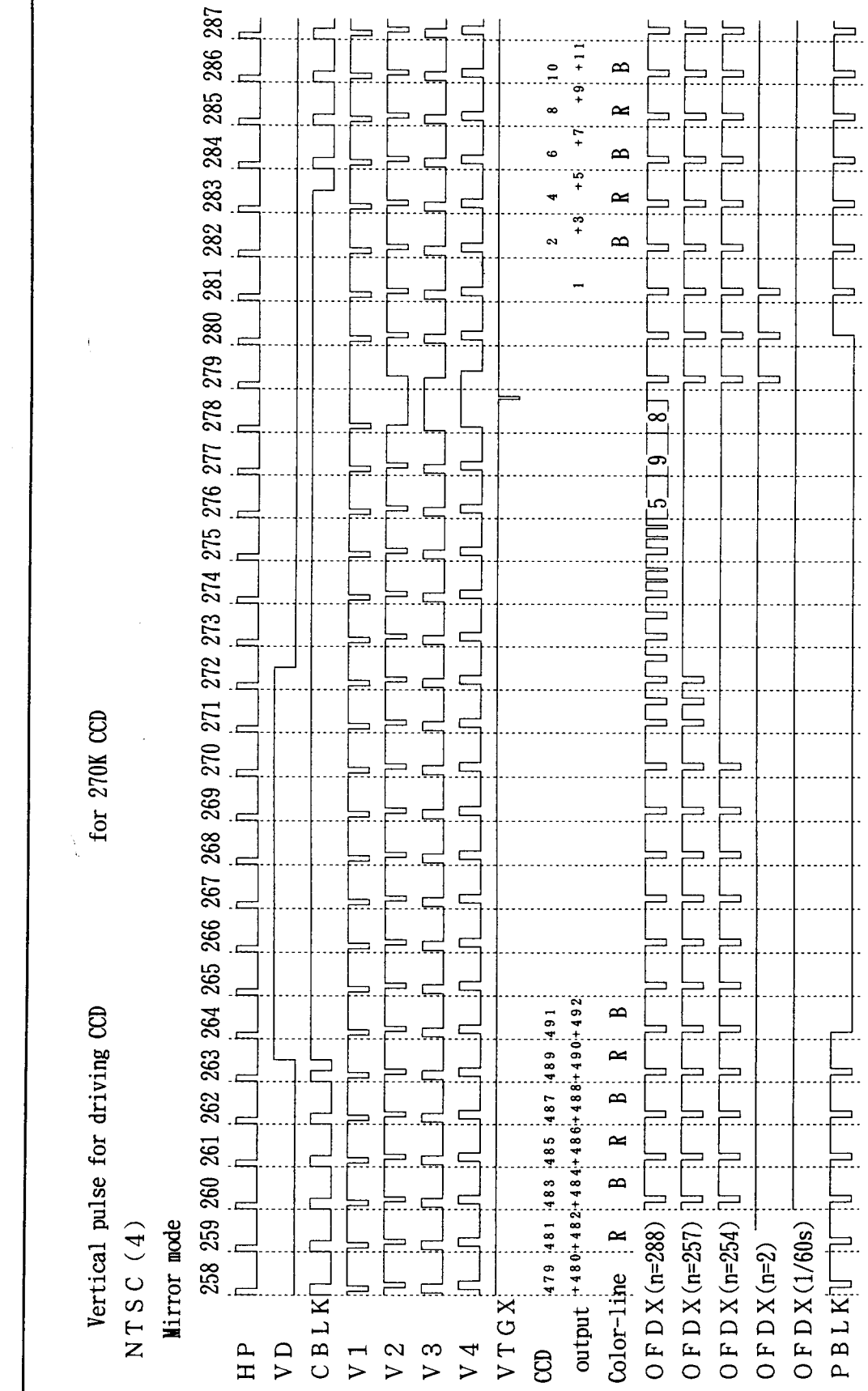
Mirror mode



Vertical pulse for driving CCD for 270K CCD

NTSC (4)

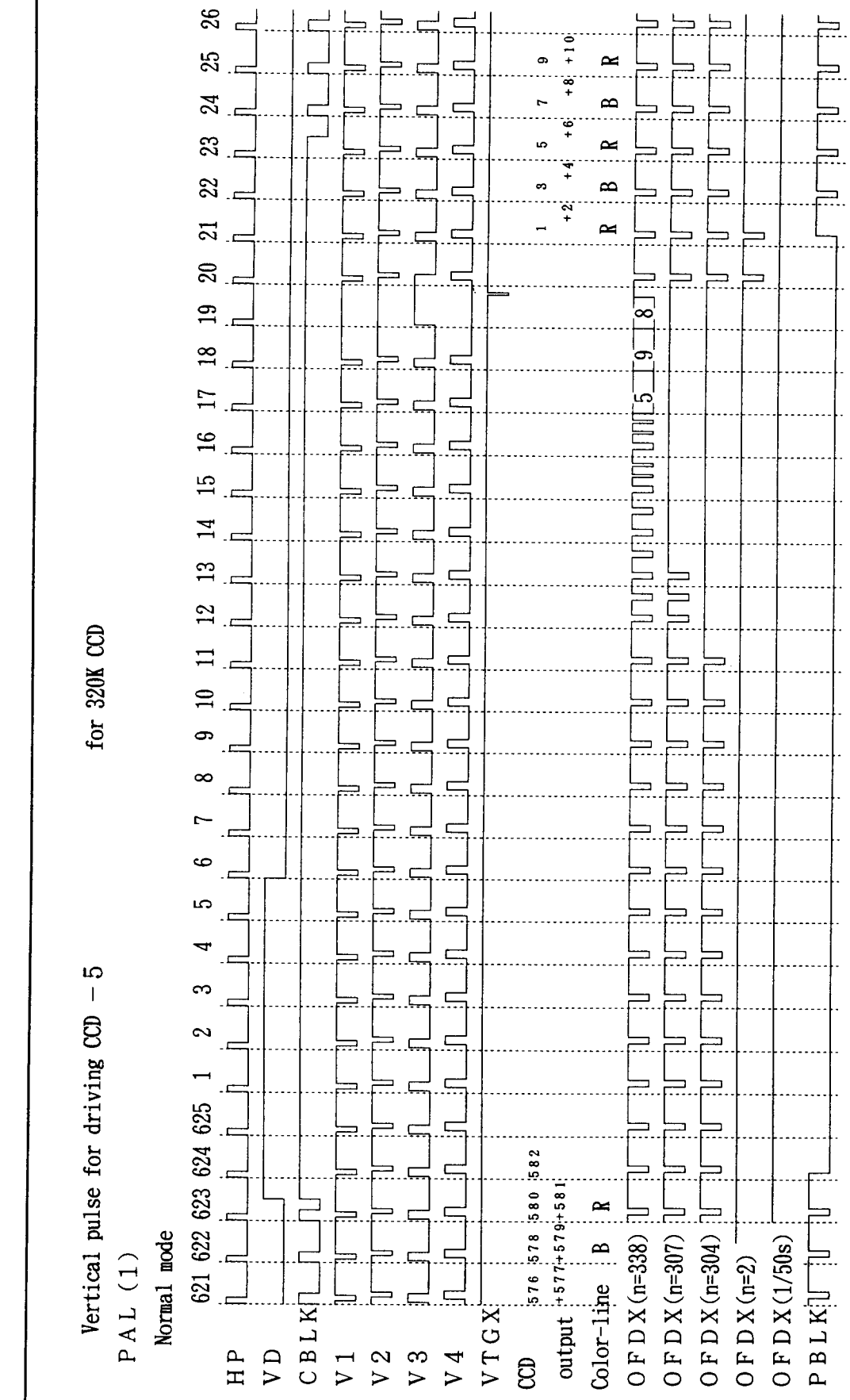
Mirror mode



Vertical pulse for driving CCD – 5 for 320K CCD

PAL (1)

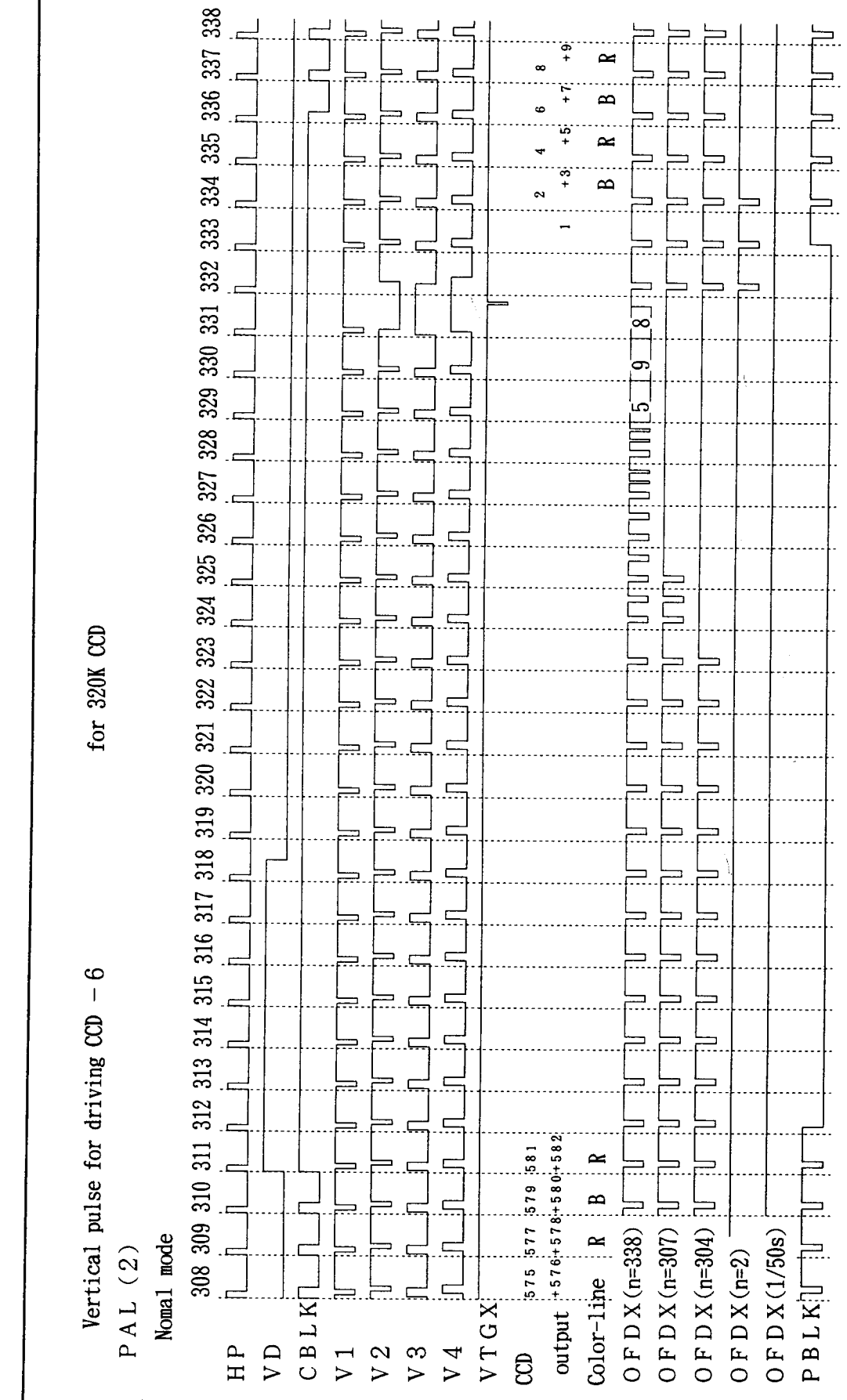
Normal mode



Vertical pulse for driving CCD – 6 for 320K CCD

PAL (2)

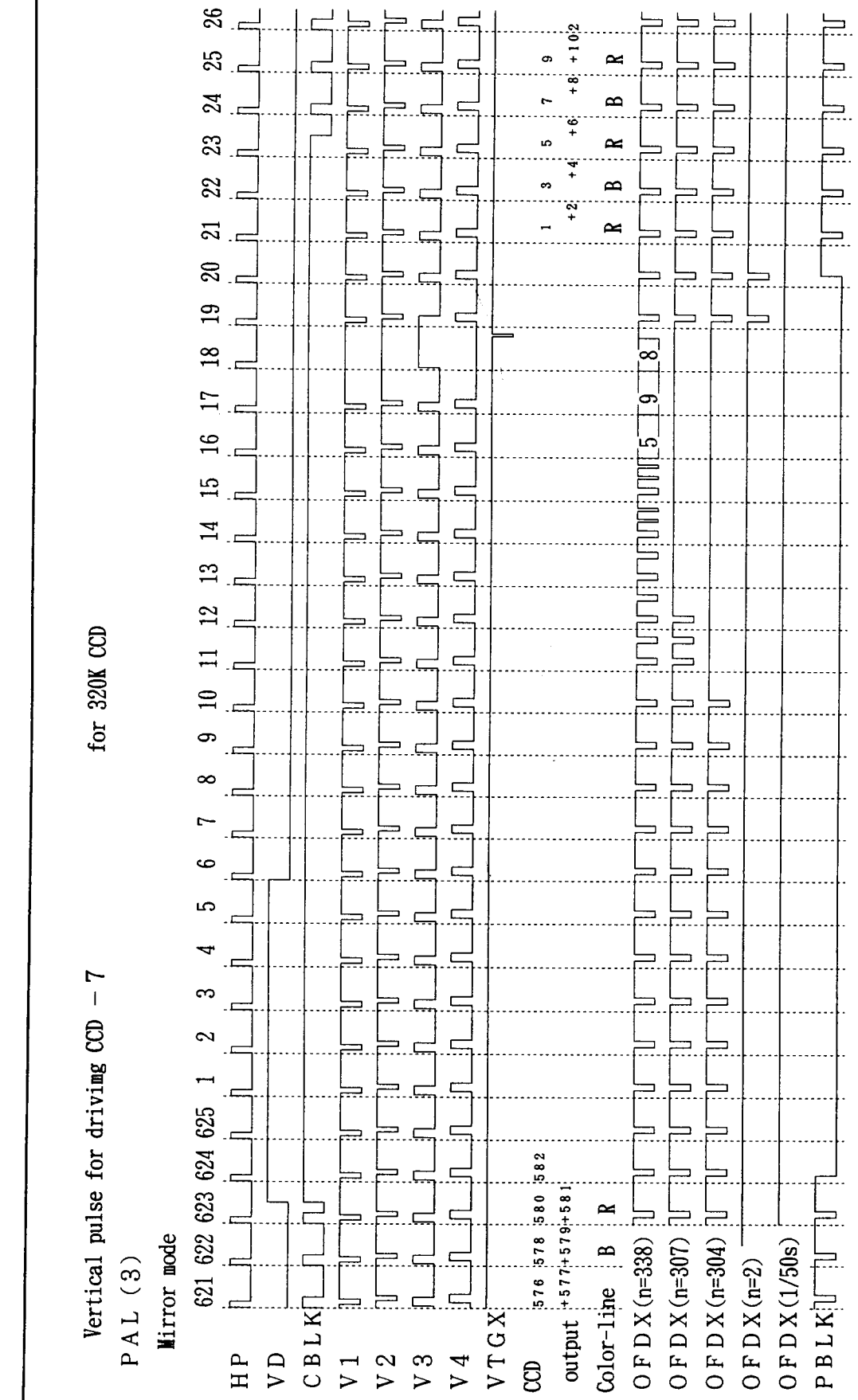
Nomal mode



Vertical pulse for driving CCD – 7 for 320K CCD

PAL (3)

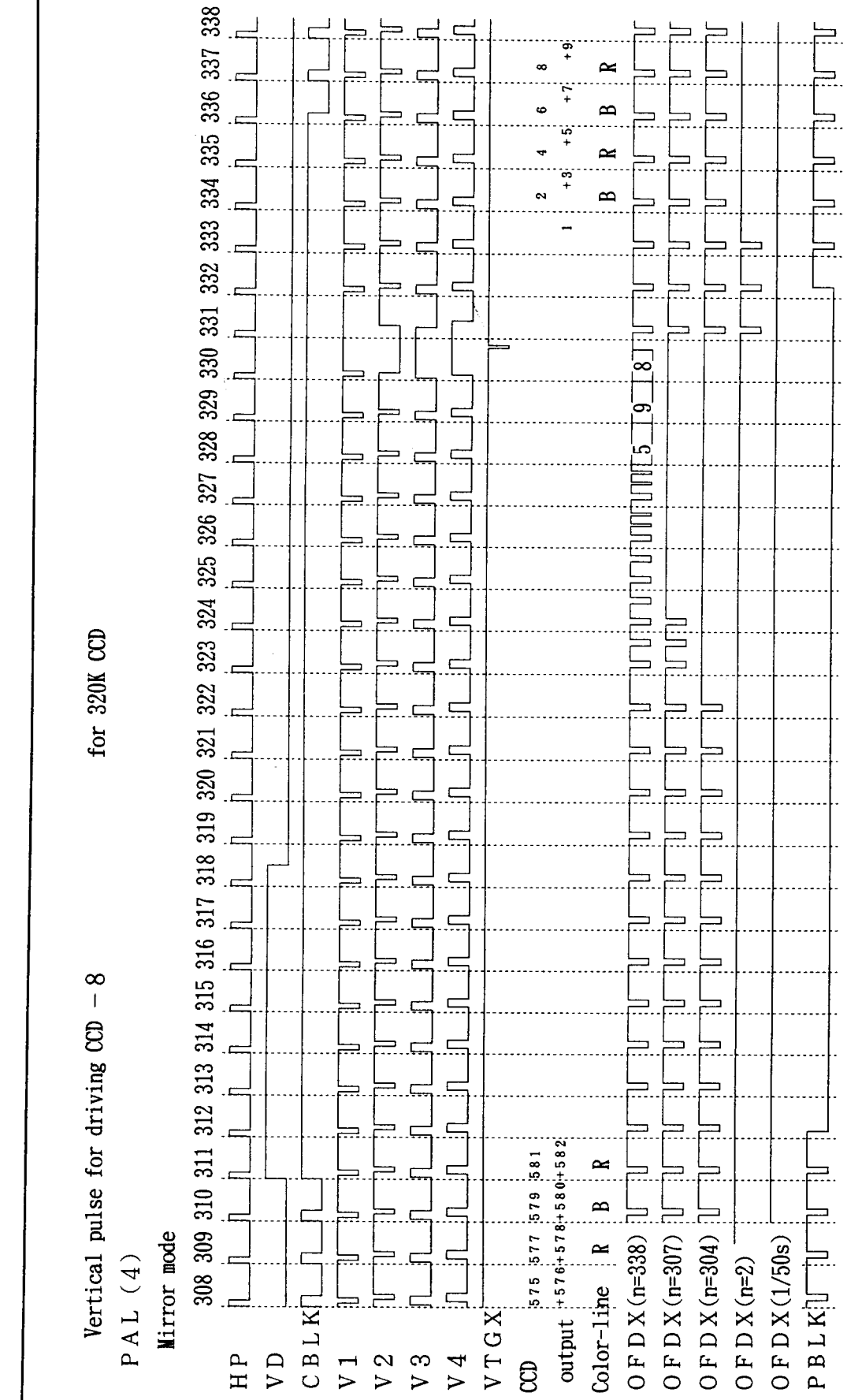
Mirror mode



Vertical pulse for driving CCD – 8 for 320K CCD

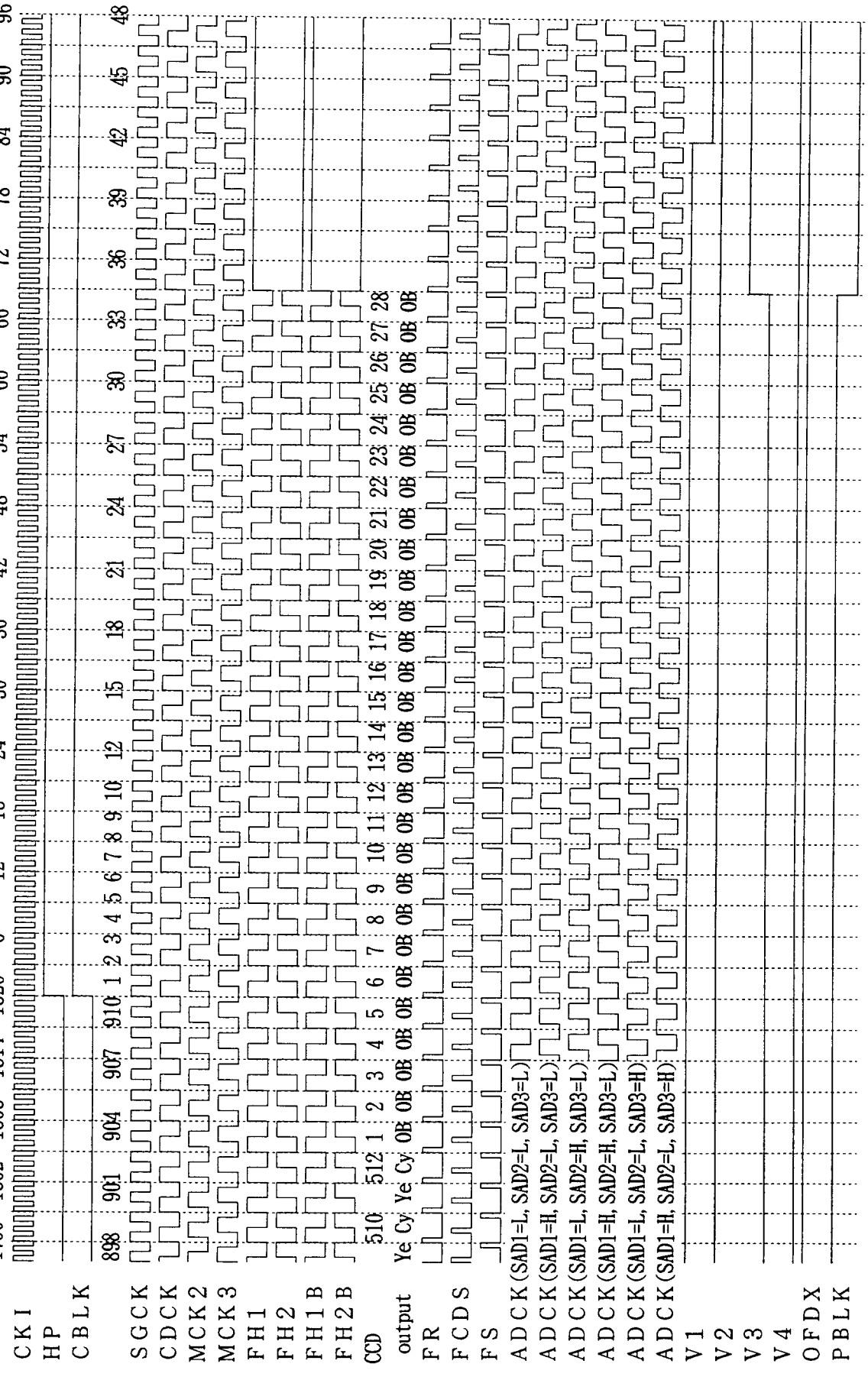
PAL (4)

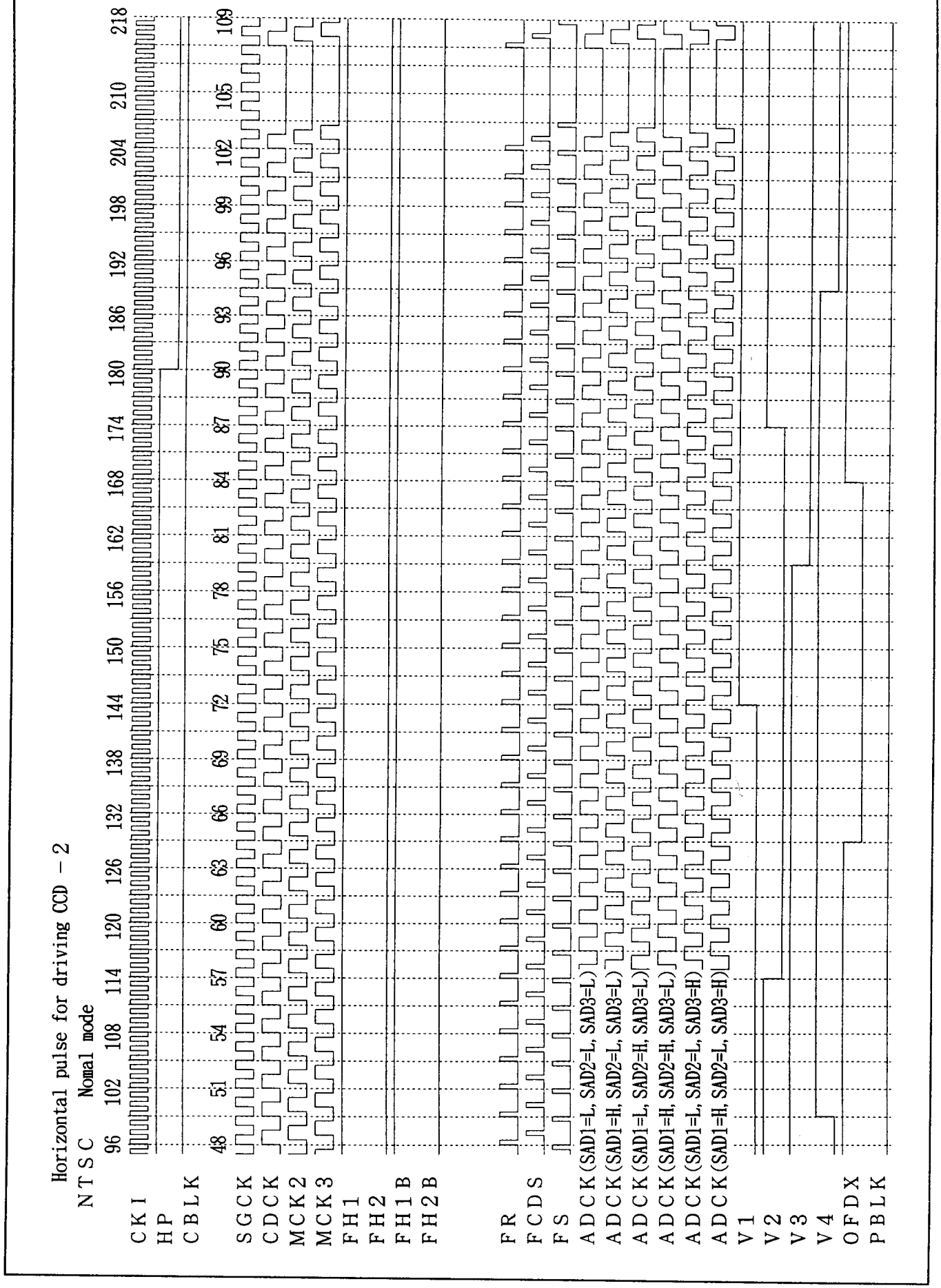
Mirror mode



6-2. Horizontal pulse for driving CCD – 1

NTSC Nomal mode

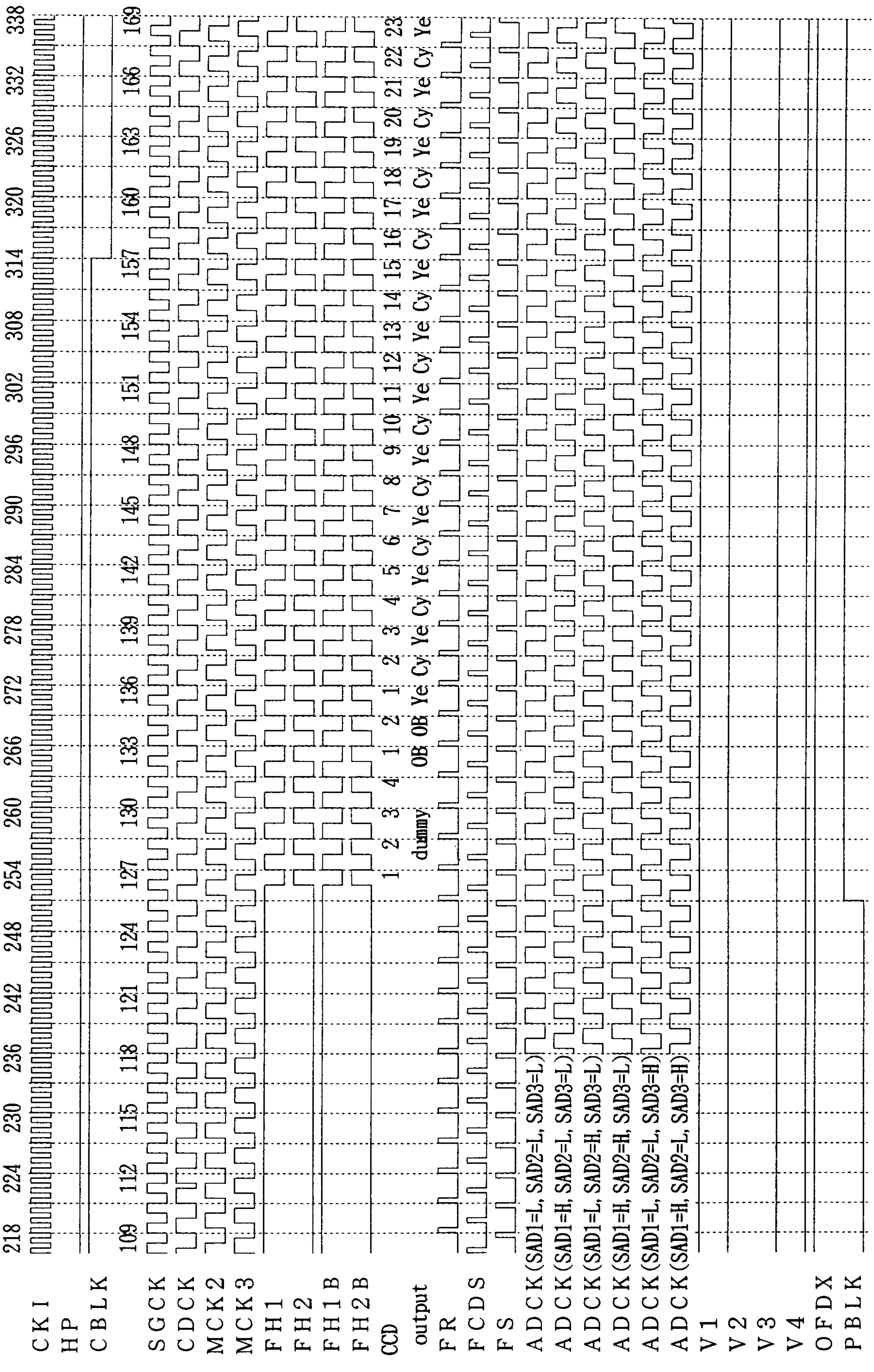



Horizontal pulse for driving CCD – 2
NTSC Nomal mode
96 102 108 114 120 126 132 138 144 150 156 162 168 174 180 186 192 198 204 210 218
48 51 54 57 60 63 66 69 72 75 78 81 84 87 90 93 96 99 102 105 109
CKI
HP
CBLK
SGCK
CDCK
MCK2
MCK3
FH1
FH2
FH1B
FH2B
FR
FCDS
FS
ADCK(SAD1=L, SAD2=L, SAD3=L)
ADCK(SAD1=H, SAD2=L, SAD3=L)
ADCK(SAD1=L, SAD2=H, SAD3=L)
ADCK(SAD1=H, SAD2=H, SAD3=L)
ADCK(SAD1=L, SAD2=L, SAD3=H)
ADCK(SAD1=H, SAD2=L, SAD3=H)
V1
V2
V3
V4
OFDX
PBLK

LR38277

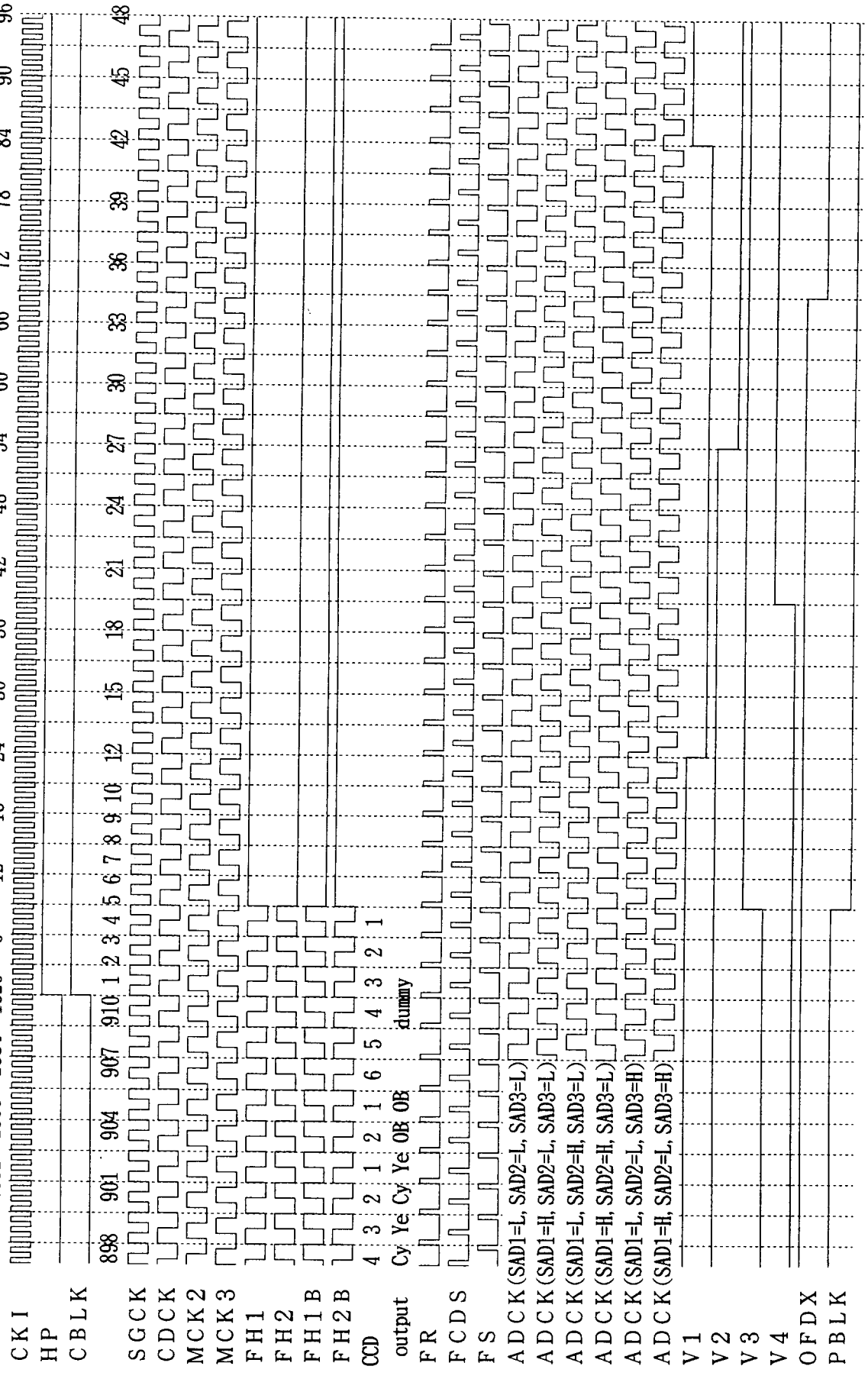
Horizontal pulse for driving CCD − 3

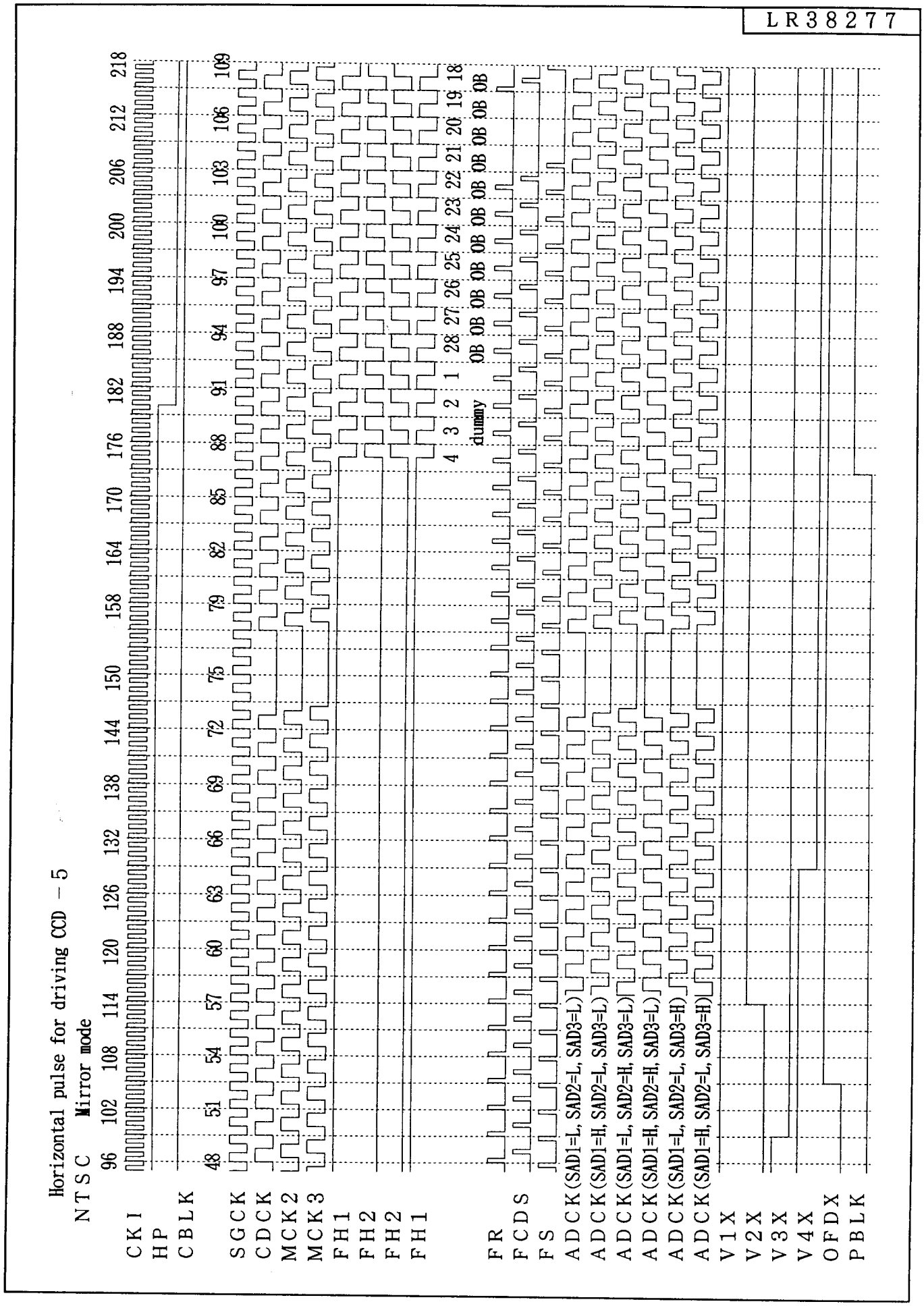
NTSC Nomal mode



Horizontal pulse for driving CCD – 4

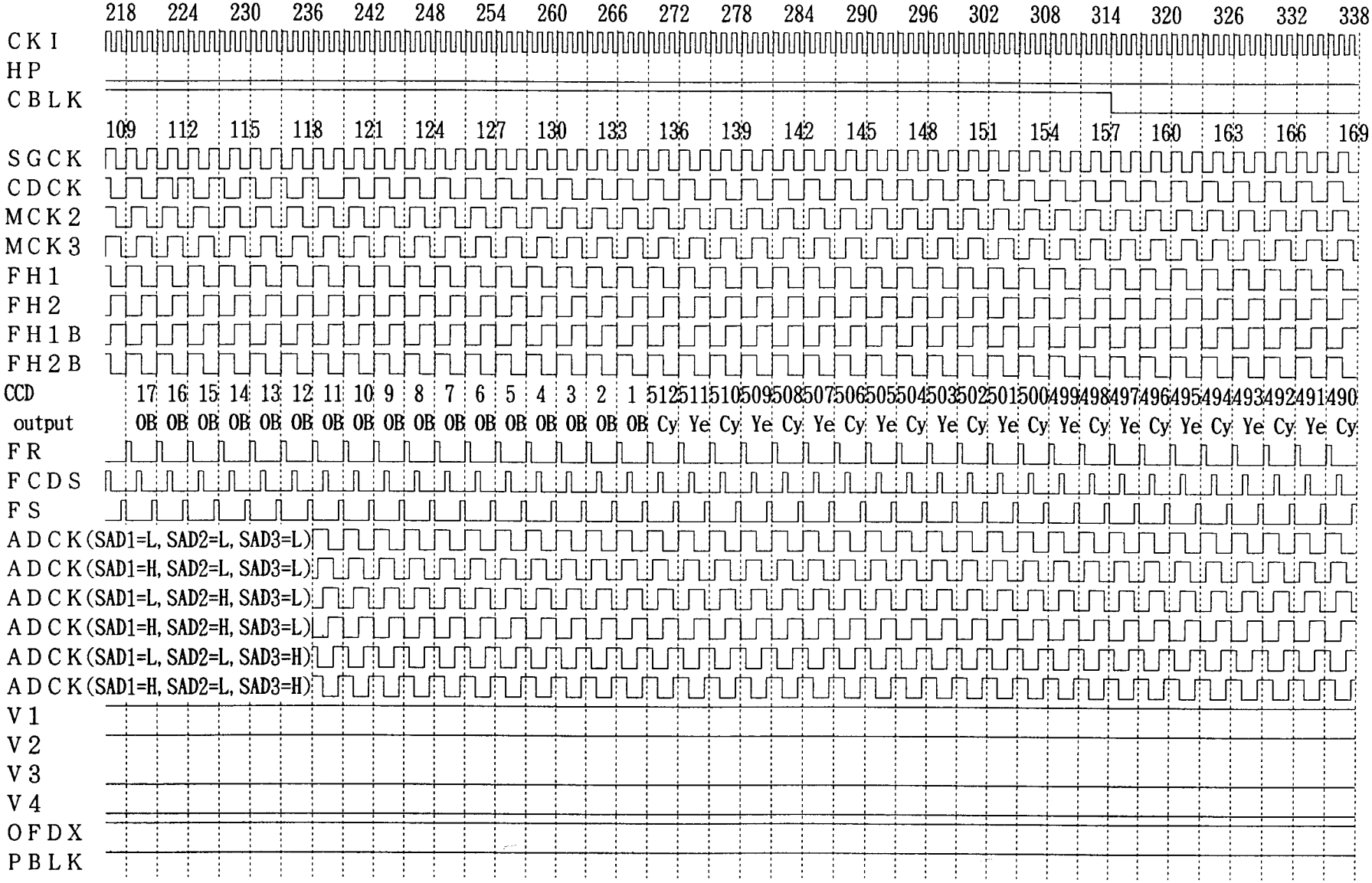
NTSC Mirror mode

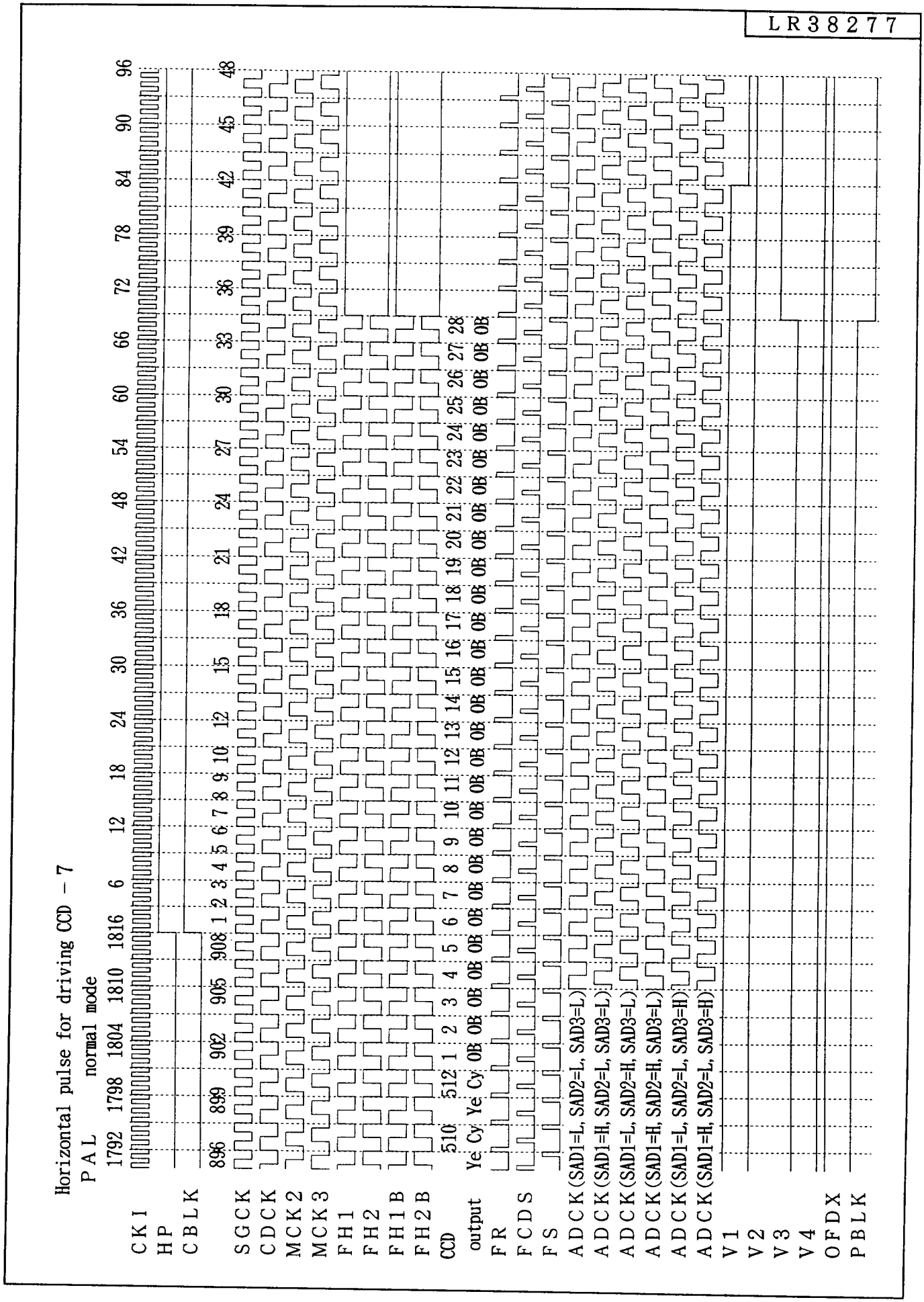



Horizontal pulse for driving CCD – 5
NTSC Mirror mode
96 102 108 114 120 126 132 138 144 150 158 164 170 176 182 188 194 200 206 212 218
48 51 54 57 60 63 66 69 72 75 79 82 85 88 91 94 97 100 103 106 109
4 3 2 1 28 27 26 25 24 23 22 21 20 19 18
dummy OB OB OB OB OB OB OB OB OB OB OB OB OB
CKI
HP
CBLK
SGCK
CDCK
MCK2
MCK3
FH1
FH2
FH2
FH1
FR
FCDS
FS
ADCK(SAD1=L, SAD2=L, SAD3=L)
ADCK(SAD1=H, SAD2=L, SAD3=L)
ADCK(SAD1=L, SAD2=H, SAD3=L)
ADCK(SAD1=H, SAD2=H, SAD3=L)
ADCK(SAD1=L, SAD2=L, SAD3=H)
ADCK(SAD1=H, SAD2=L, SAD3=H)
V1X
V2X
V3X
V4X
OFDX
PBLK

Horizontal pulse for driving CCD − 6

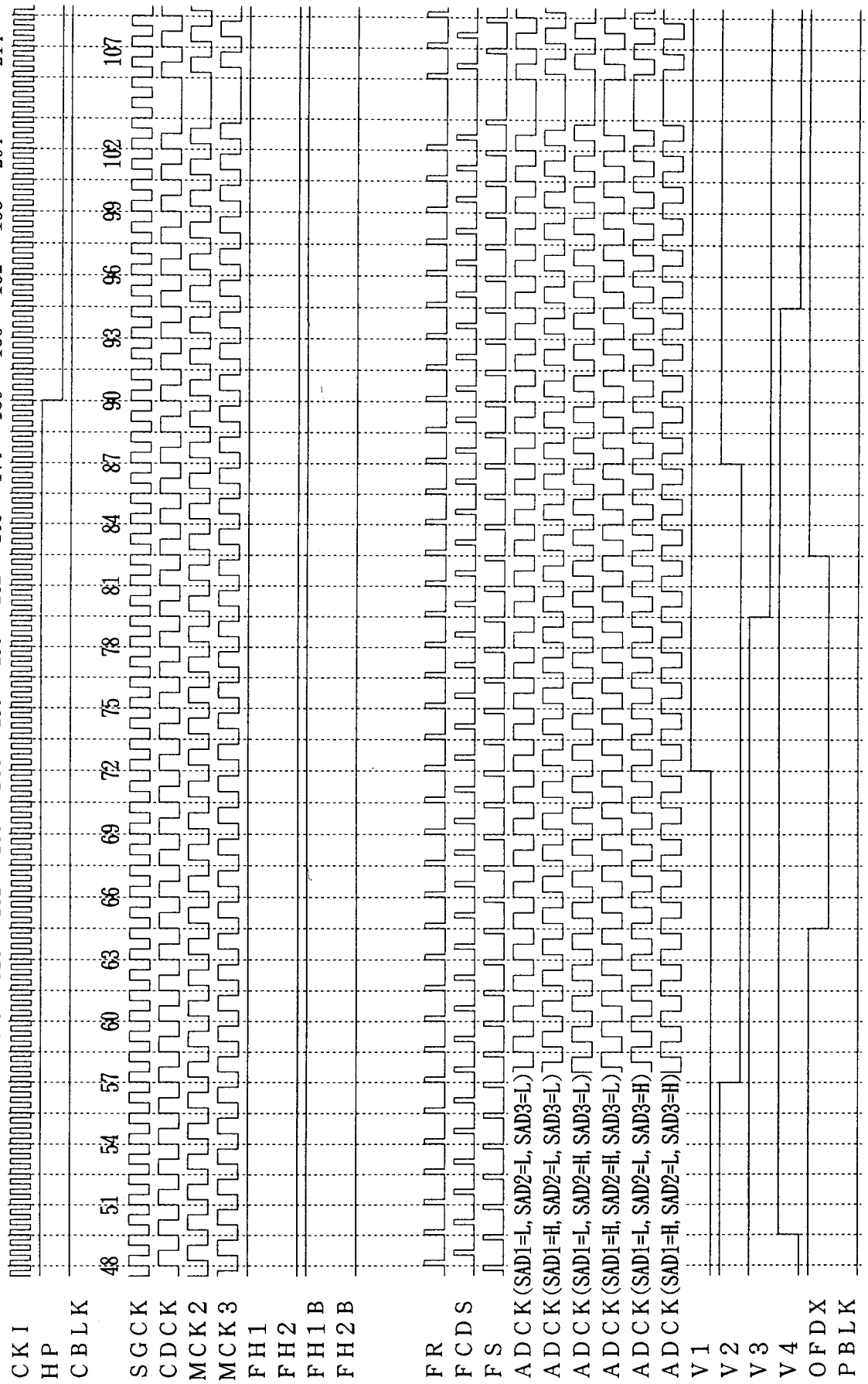
NTSC Mirror mode

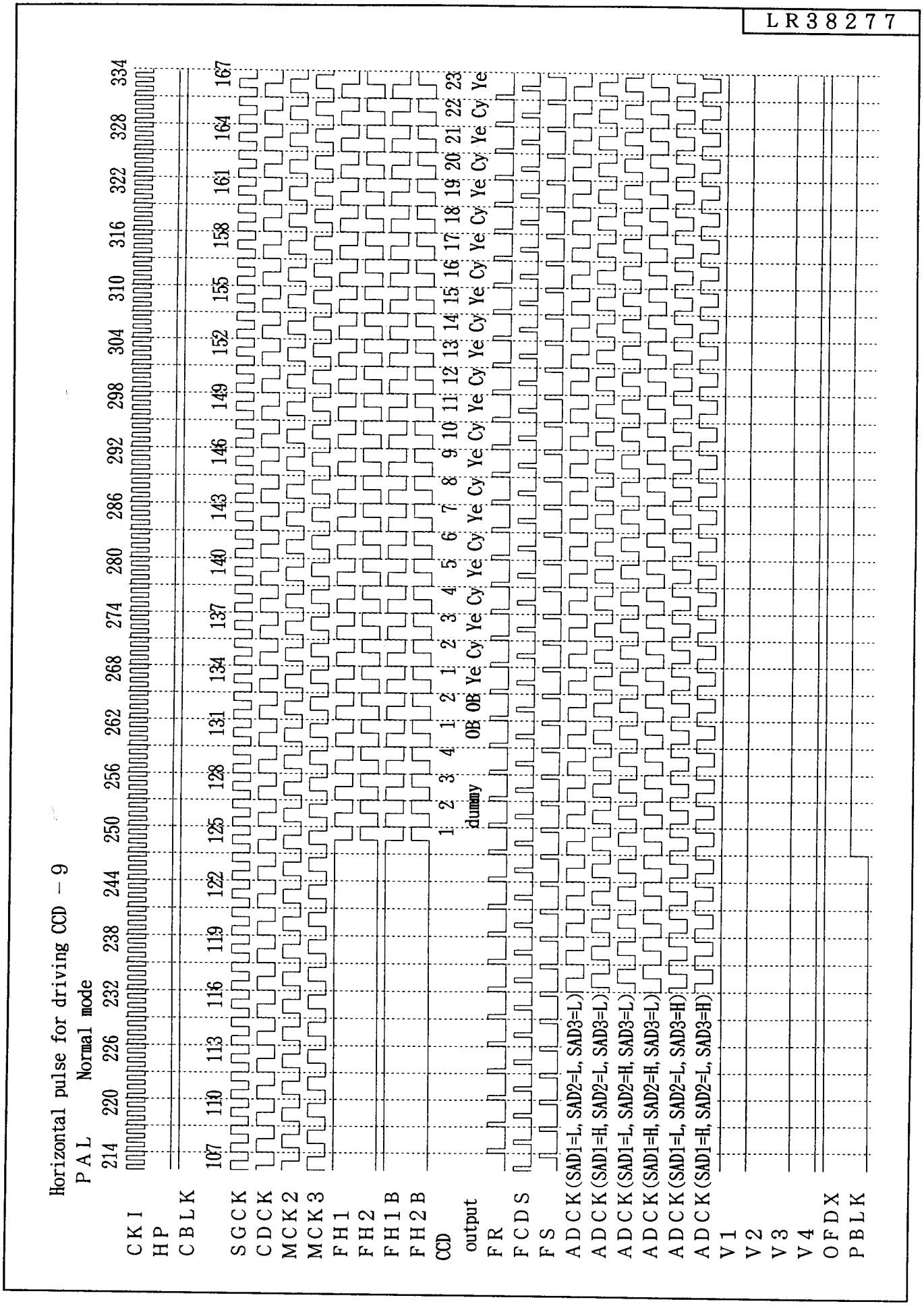


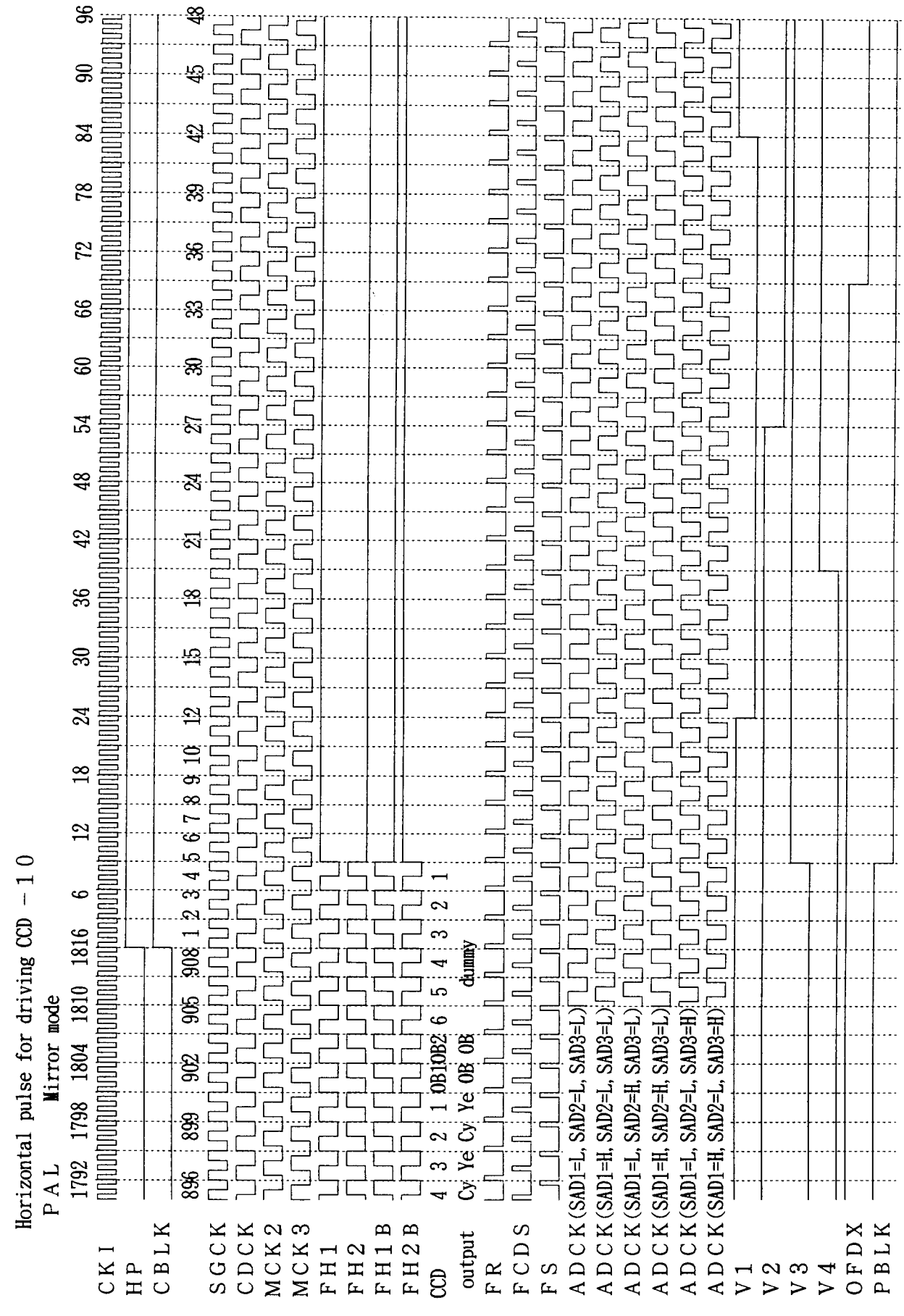

LR38277
Horizontal pulse for driving CCD – 7
PAL normal mode
CKI
HP
CBLK
SGCK
CDCK
MCK2
MCK3
FH1
FH2
FH1B
FH2B
CCD output
FR
FCDS
FS
ADCK (SAD1=L, SAD2=L, SAD3=L)
ADCK (SAD1=H, SAD2=L, SAD3=L)
ADCK (SAD1=L, SAD2=H, SAD3=L)
ADCK (SAD1=H, SAD2=H, SAD3=L)
ADCK (SAD1=L, SAD2=L, SAD3=H)
ADCK (SAD1=H, SAD2=L, SAD3=H)
V1
V2
V3
V4
OFDX
PBLK

Horizontal pulse for driving CCD – 8

PAL Normal mode

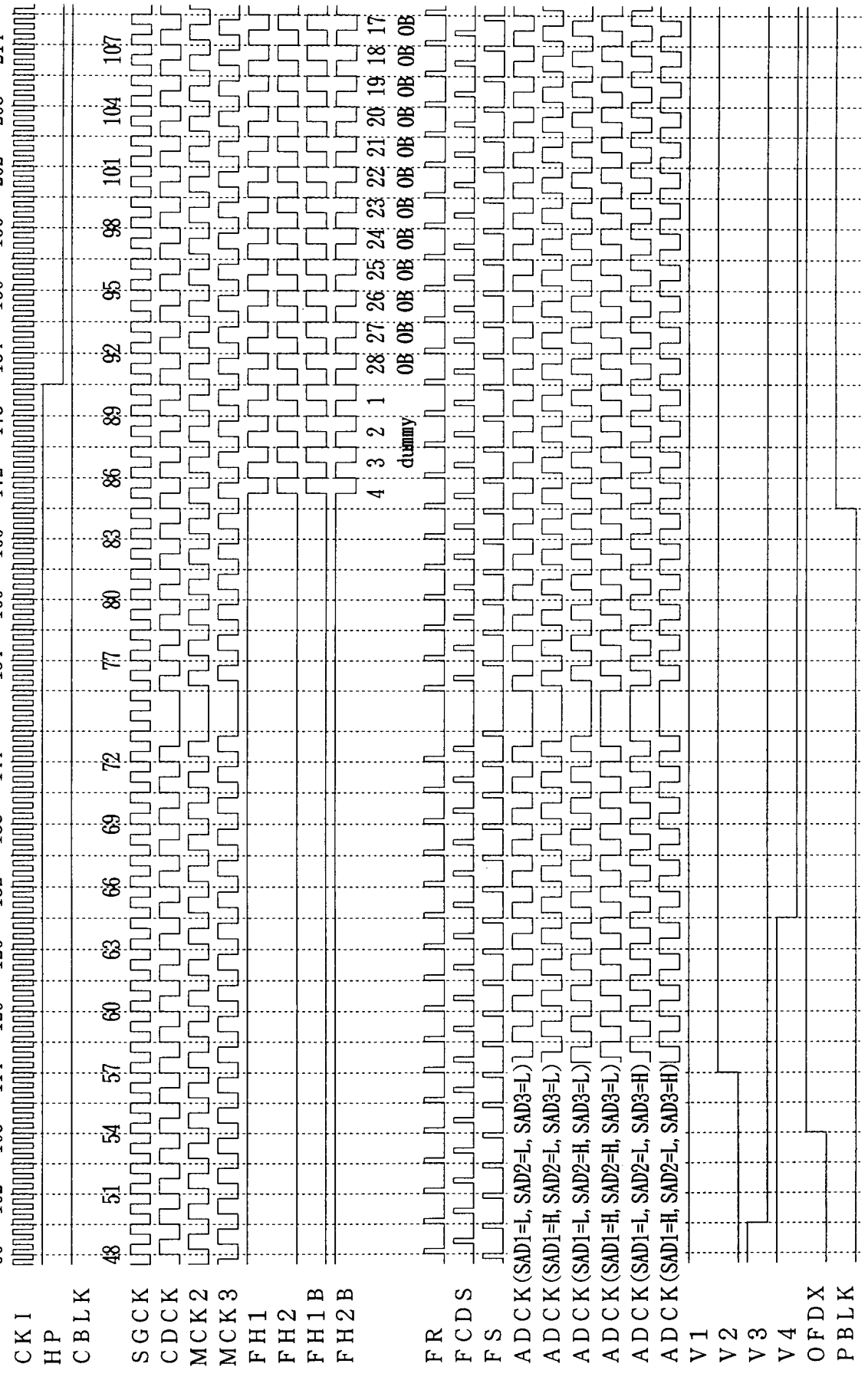



Horizontal pulse for driving CCD – 9
PAL Normal mode
214 220 226 232 238 244 250 256 262 268 274 280 286 292 298 304 310 316 322 328 334
107 110 113 116 119 122 125 128 131 134 137 140 143 146 149 152 155 158 161 164 167
CKI
HP
CBLK
SGCK
CDCK
MCK2
MCK3
FH1
FH2
FH1B
FH2B
CCD output
1 2 3 4 dummy OB 1 2 OB Ye Cy 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 Ye Cy Ye Cy Ye Cy Ye Cy Ye Cy Ye Cy Ye Cy Ye Cy Ye Cy Ye Cy Ye Cy Ye Cy Ye
FR
FCDS
FS
ADCK (SAD1=L, SAD2=L, SAD3=L)
ADCK (SAD1=H, SAD2=L, SAD3=L)
ADCK (SAD1=L, SAD2=H, SAD3=L)
ADCK (SAD1=H, SAD2=H, SAD3=L)
ADCK (SAD1=L, SAD2=L, SAD3=H)
ADCK (SAD1=H, SAD2=L, SAD3=H)
V1
V2
V3
V4
OFDX
PBLK


Horizontal pulse for driving CCD – 1 0
PAL Mirror mode
1792 1798 1804 1810 1816 6 12 18 24 30 36 42 48 54 60 66 72 78 84 90 96
896 899 902 905 908 1 2 3 4 5 6 7 8 9 10 15 18 21 24 27 30 33 36 39 42 45 48
CKI
HP
CBLK
SGCK
CDCK
MCK2
MCK3
FH1
FH2
FH1B
FH2B
CCD
4 3 2 1 OB10B2 6 5 4 3 2 1
output
Cy Ye Cy Ye OB OB dummy
FR
FCDS
FS
ADCK(SAD1=L, SAD2=L, SAD3=L)
ADCK(SAD1=H, SAD2=L, SAD3=L)
ADCK(SAD1=L, SAD2=H, SAD3=L)
ADCK(SAD1=H, SAD2=H, SAD3=L)
ADCK(SAD1=L, SAD2=L, SAD3=H)
ADCK(SAD1=H, SAD2=L, SAD3=H)
V1
V2
V3
V4
OFDX
PBLK

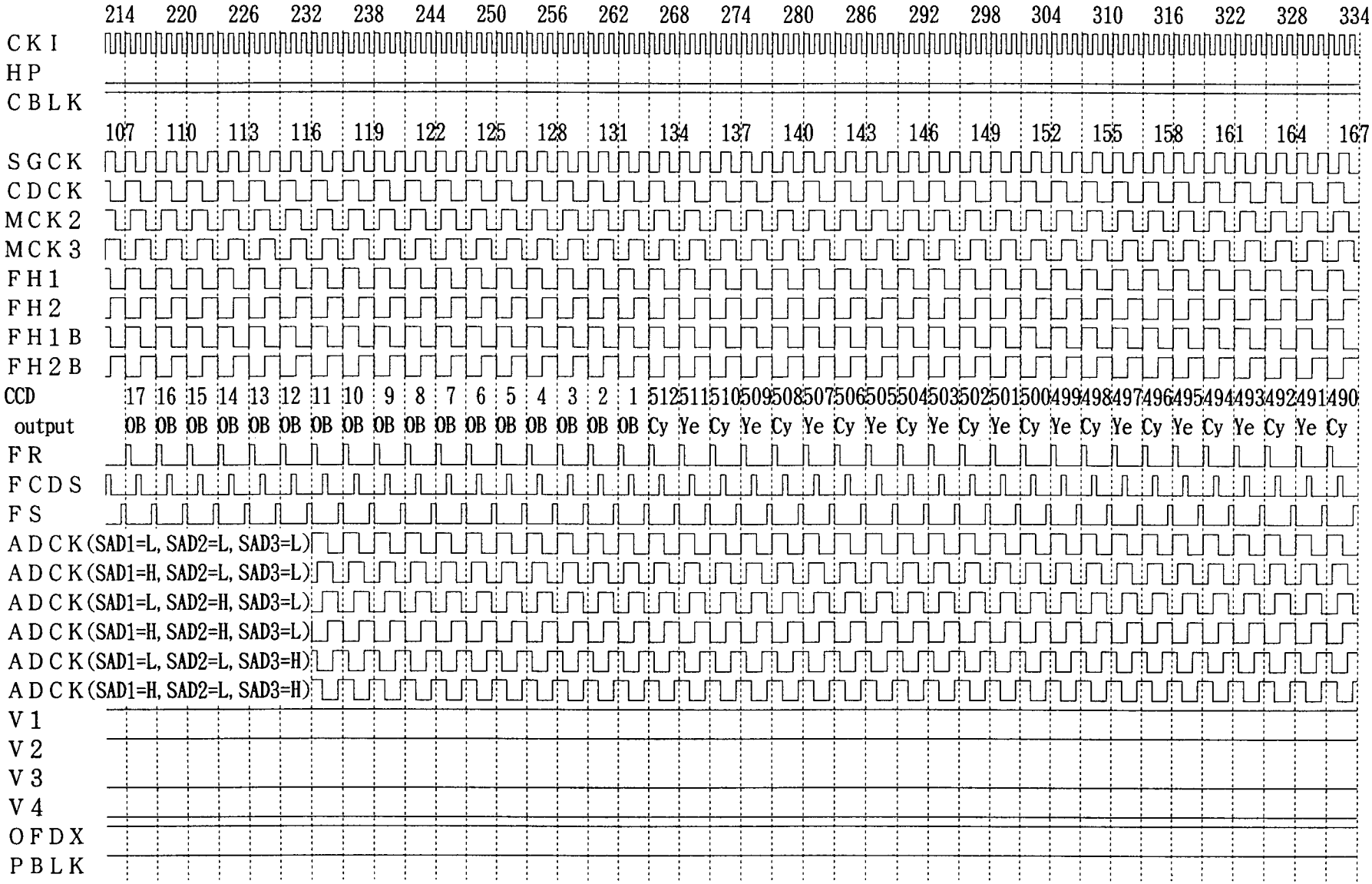
Horizontal pulse for driving CCD – 1 1

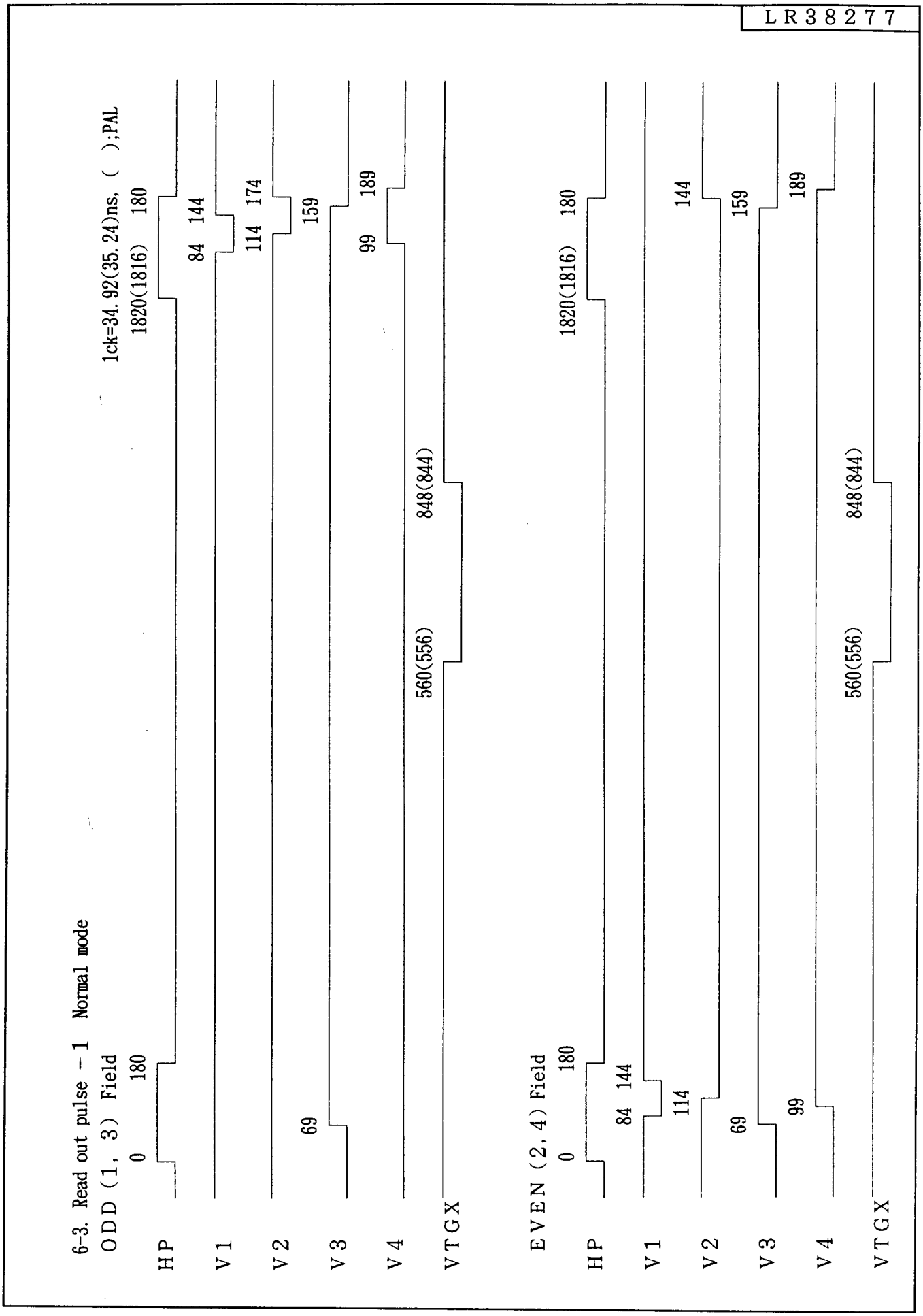
PAL Mirror mode

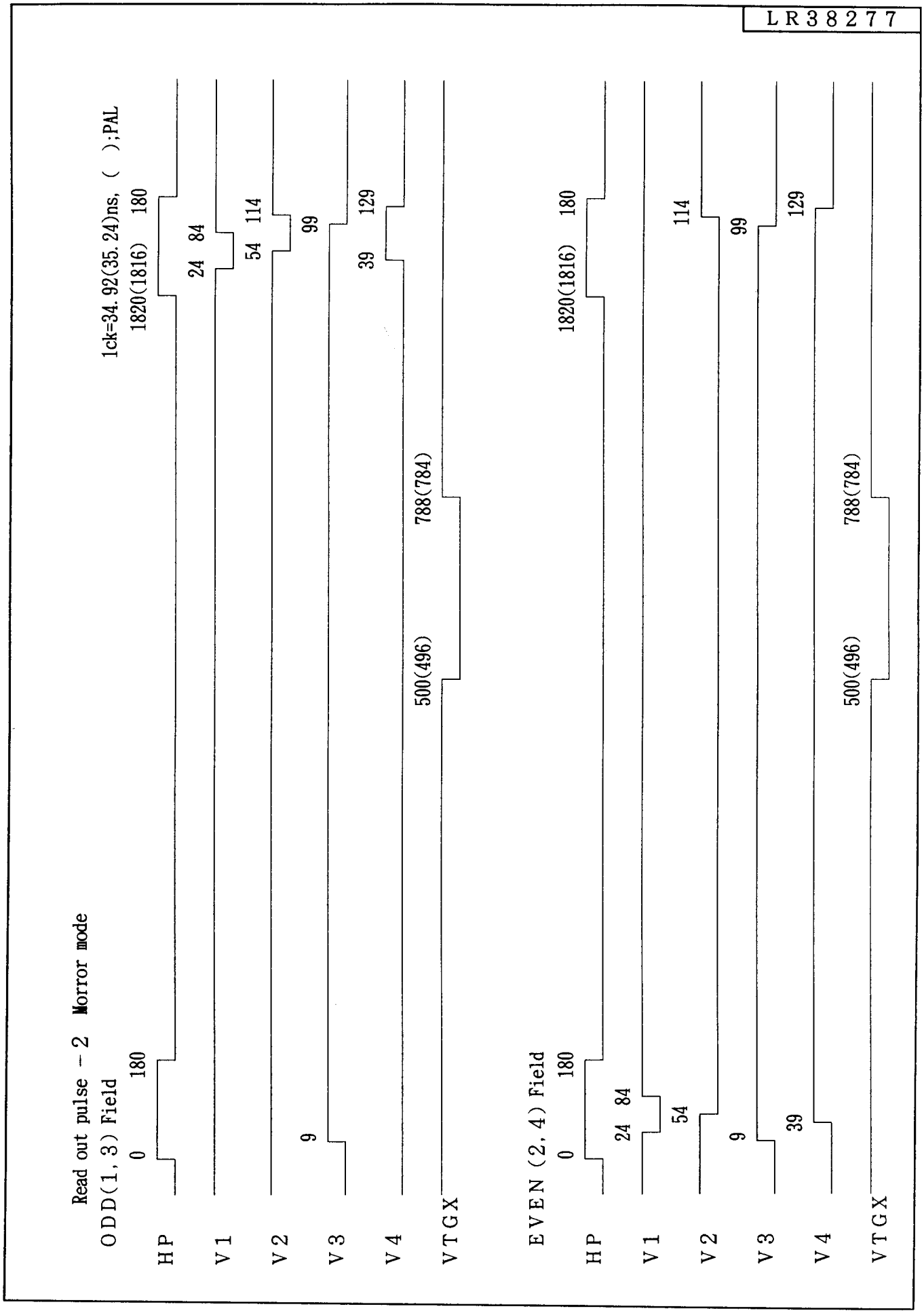


Horizontal pulse for driving CCD －12

PAL　　Mirror mode

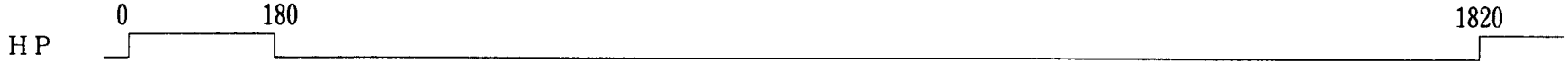



LR38277
6-3. Read out pulse - 1 Normal mode
1ck=34.92(35.24)ns, ( ):PAL
ODD (1, 3) Field
0
180
1820(1816)
180
84
144
114
174
69
159
99
189
560(556)
848(844)
HP
V1
V2
V3
V4
VTGX
EVEN (2, 4) Field
0
180
1820(1816)
180
84
144
114
144
69
159
99
189
560(556)
848(844)
HP
V1
V2
V3
V4
VTGX

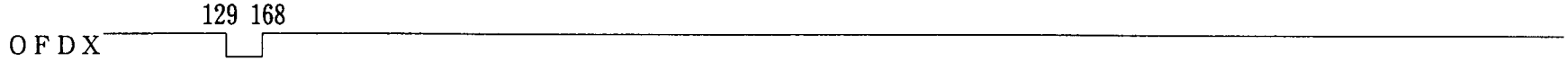

LR38277
Read out pulse - 2 Mirror mode
1ck=34.92(35.24)ns, ( ):PAL
ODD(1,3) Field
0
180
1820(1816)
180
24
84
54
114
9
99
39
129
500(496)
788(784)
HP
V1
V2
V3
V4
VTGX
EVEN(2,4) Field
0
180
1820(1816)
180
24
84
54
114
9
99
39
129
500(496)
788(784)
HP
V1
V2
V3
V4
VTGX

6-4. Shutter pulse －1

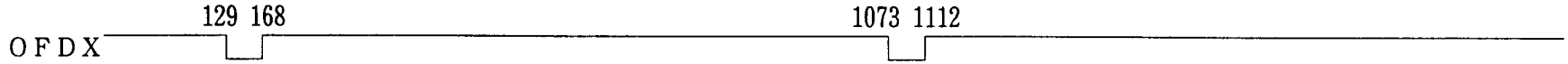
NTSC　　Nomal mode　　The number;clock pulse　　1ck=34.92ns



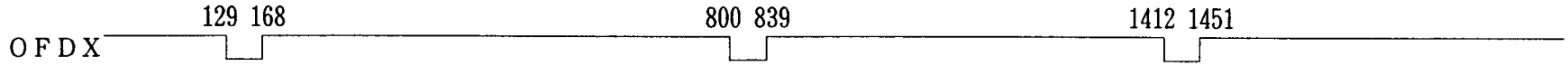
・Except 10(12)H～18(20)H, 272(324)H～280(332)H



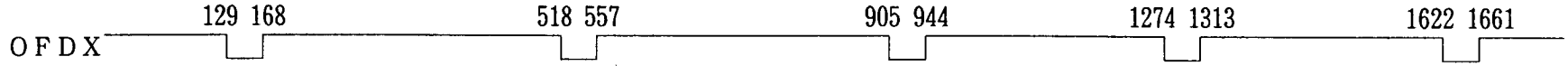
・10(12)H～12(14)H, 272(324)H～274(326)H



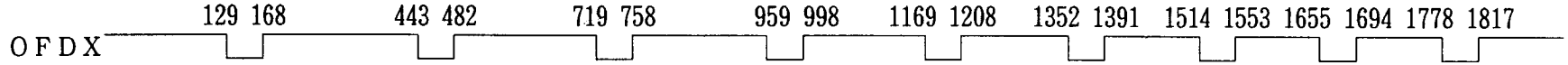
・13(15)H～14(16)H, 275(327)H～276(328)H



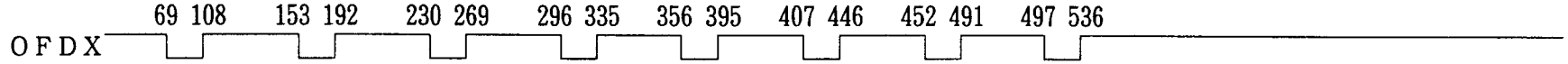
・15(17)H, 277(329)H



・16(18)H, 278(330)H



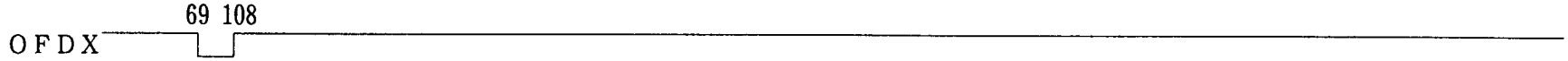
・17(19)H, 279(331)H



Shutter pulse －2

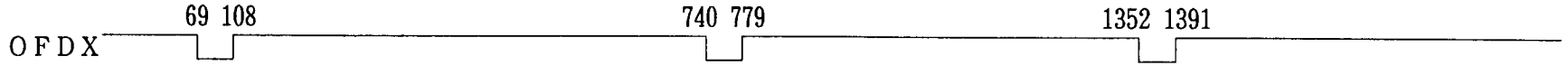
NTSC　　Mirror mode　　The number;clock pulse　　1ck=34.92ns

・Except 10(12)H～18(20)H, 272(324)H～280(332)H

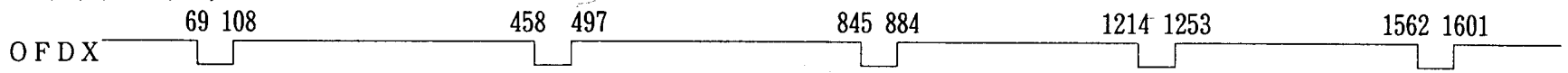


・10(12)H～12(14)H, 272(324)H～274(326)H

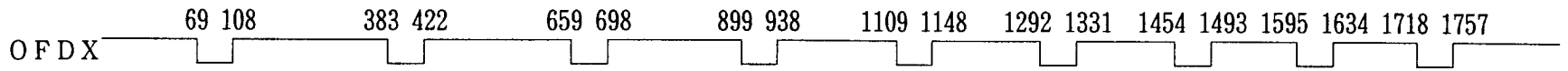
・13(15)H～14(16)H, 275(327)H～276(328)H



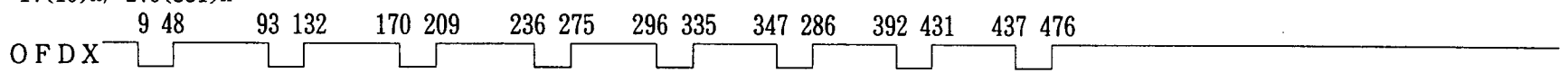
・15(17)H, 277(329)H



・16(18)H, 278(330)H

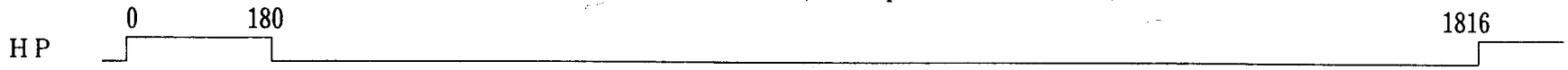


・17(19)H, 279(331)H

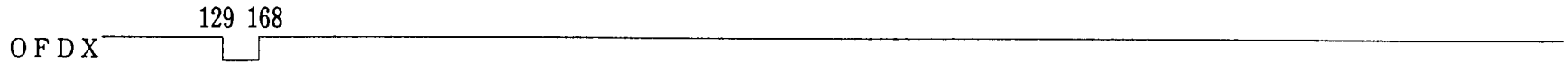


Shutter pulse − 3

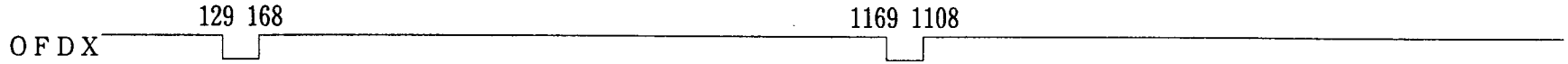
PAL　　Normal mode　　The number;clock pulse　　1ck=35.24ns



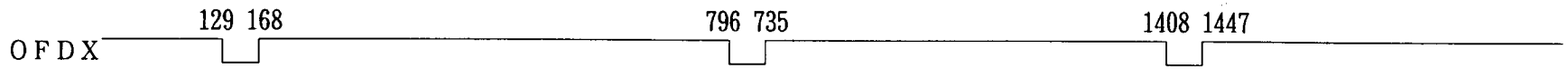
・Except 12H～20H, 324H～332H



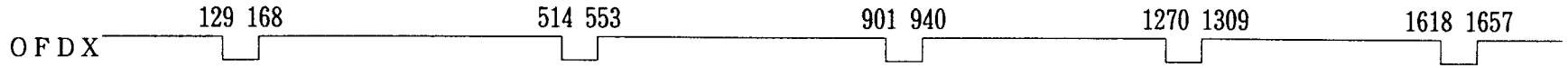
・12H～14H, 324H～326H



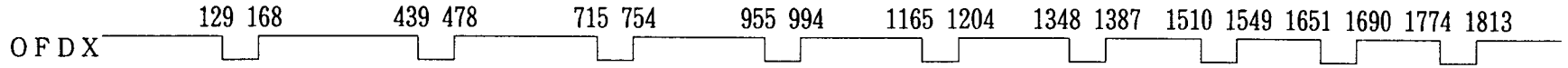
・15H～16H, 327H～328H



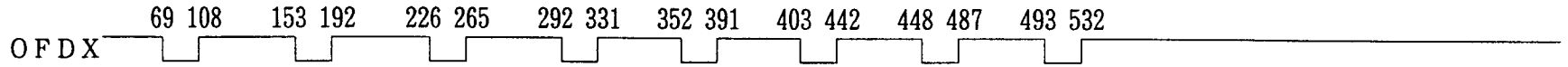
・17H, 329H

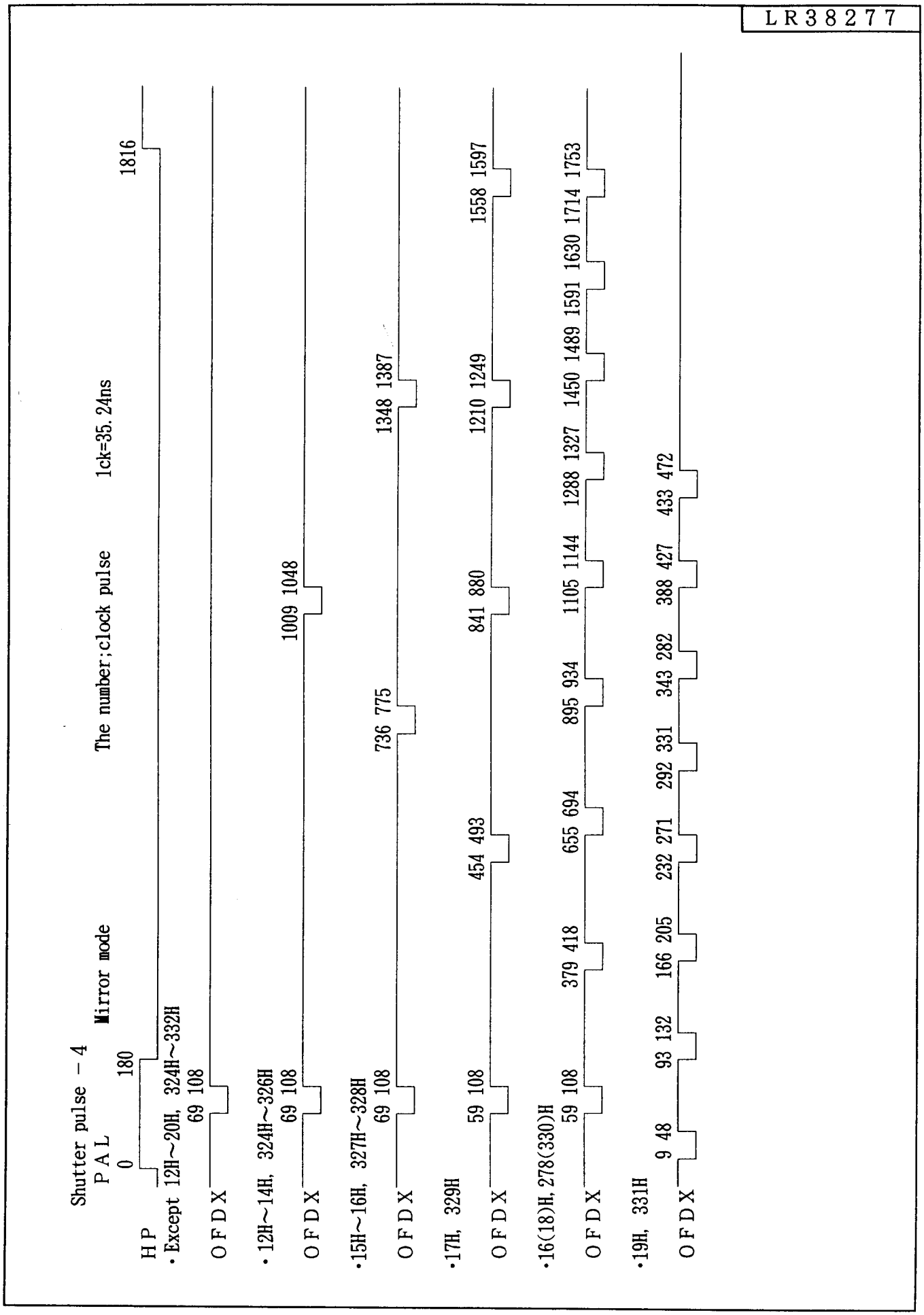


・18H, 330H



・19H, 331H




Shutter pulse – 4
Mirror mode
The number;clock pulse
1ck=35.24ns
PAL
0
180
1816
HP
・Except 12H~20H, 324H~332H
69 108
OFDX
・12H~14H, 324H~326H
69 108
1009 1048
OFDX
・15H~16H, 327H~328H
69 108
736 775
1348 1387
OFDX
・17H, 329H
59 108
454 493
841 880
1210 1249
1558 1597
OFDX
・16(18)H, 278(330)H
59 108
379 418
655 694
895 934
1105 1144
1288 1327
1450 1489
1591 1630
1714 1753
OFDX
・19H, 331H
9 48
93 132
166 205
232 271
292 331
343 282
388 427
433 472
OFDX

7 Package and packing specification

1. Package Outline Specification

Refer to drawing No.AA1035

2. Markings

2－1. Marking contents

(1) Product name : LR38277

(2) Company name : SHARP

(3) Date code

(Example) YY WW ×

- YY → Denotes the production year. (Lower two digits of the year.)
- WW → Denotes the production week. (01,02,03, ・・・・・52,53)
- × → Denotes the production ref.code.

Indicates the product was manufactured in the WWth week of 19YY.

(4) The marking of "JAPAN" indicates the country of origin.

2－2. Marking layout

Refer to drawing No.AA1035

(This layout do not define the dimensions of marking character and marking position.)

3. Packing Specification

3－1. Packing materials

Material Name	Material Specification	Purpose
Tray	Conductive plastic (80devices/tray)	Fixing of device
Upper cover tray	Conductive plastic (1tray/case)	Fixing of device
Laminated aluminum bag	Aluminum polyethylene (1bag/case)	Drying of device
Desiccant	Silica gel	Drying of device
P P band	Polypropylene (3 pcs/case)	Device tray fixing
Inner case	Card board (800devices/case)	Packaging of device
Label	Paper	Indicates part number, quantity and date of manufacture
Outer case	Cardboard	Outer packing of device case

(Devices shall be placed into a tray in the same direction.)

3－2. Outline dimension of tray

Refer to attached drawing

4. Precausion For Unpacking

(1) Unpacking should be done on the stand as well as human body treated with anti-ESD.

(2) Conductive treatment or anti-ESD treatment is given to a dray. Use the equivalent tray, if it is changed to another one.

5. Surface Mount Conditions

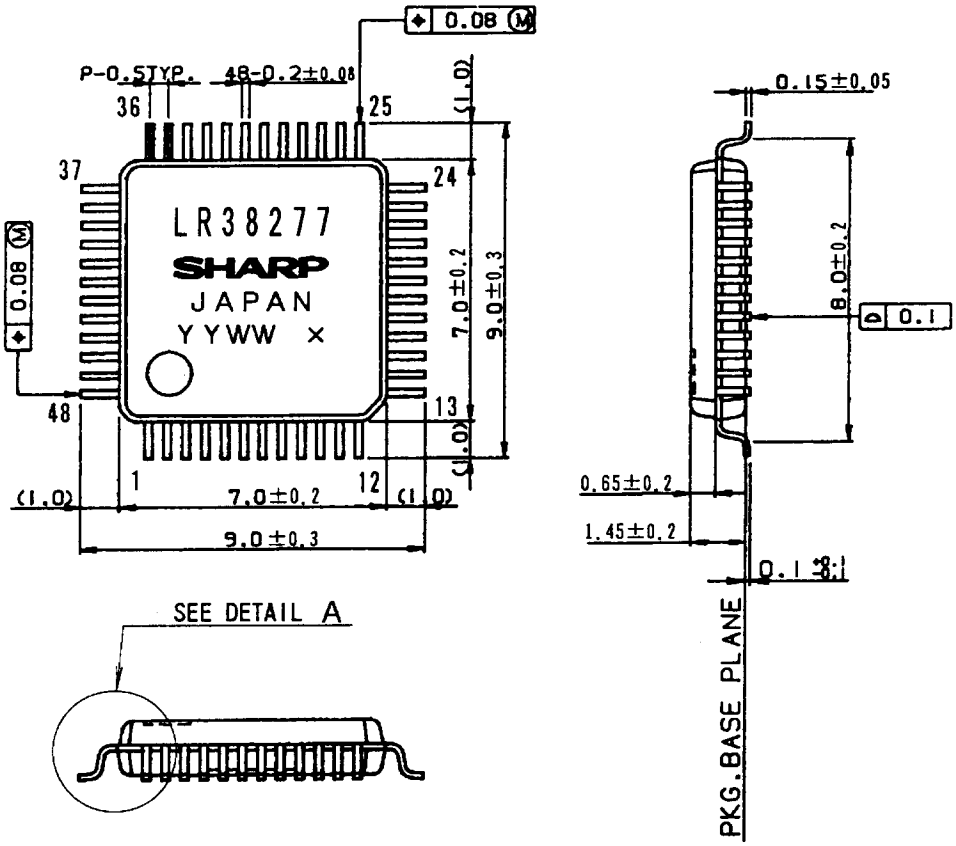
Please perform the following conditions when mounting ICs not to deteriorate IC quality.

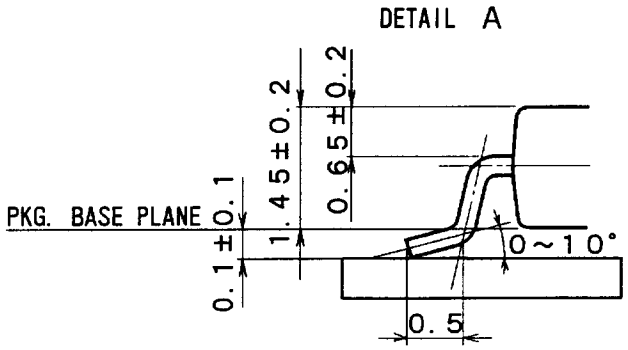
5－1.Soldering conditions(The following conditions are valid only for one time soldering.)

Mounting Method	Temperature and Duration	Measurement Point
Reflow soldering (air)	Peak temperature of 240℃, duration less than 15 seconds above 230℃, temperature increase rate of 1～4℃/second	IC surface
Vapor phase solderring	215℃ or less, duration less than 40 seconds above 200℃	Steam
Manual soldering (soldering iron)	260℃ or less, duration less than 10 seconds	IC outer lead surface

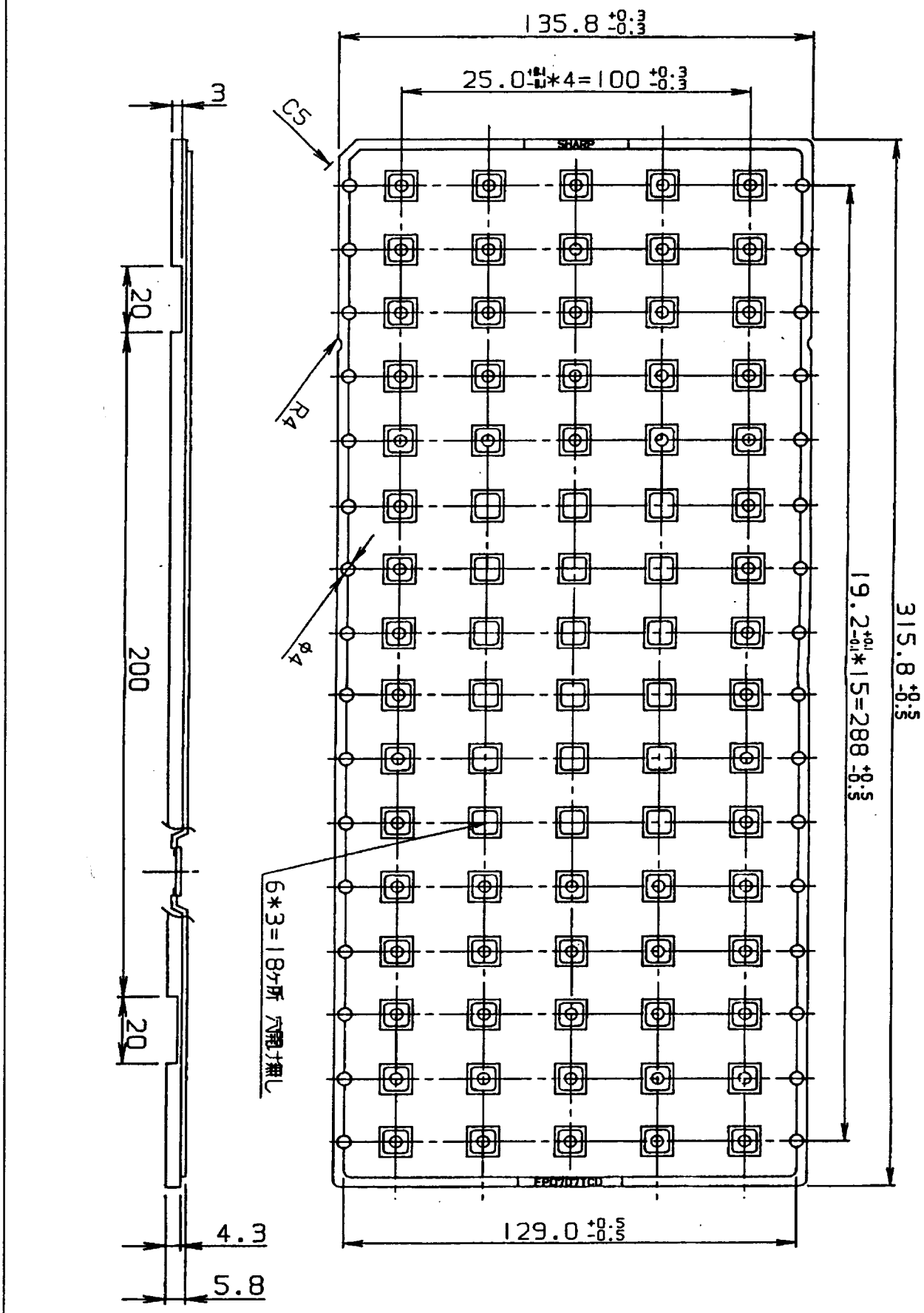
5－2. Conditions for removal of residual flux

(1) Ultrasonic washing power : 25 Watts/liter or less
(2) Washing time : Total 1 minute maximum
(3) Solvent temperature : 15～40℃





名称 NAME	QFP48-P-0707	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 NOTE プラスチックパッケージ外形寸法は、バリを含まないものとする。 Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1035	単位 UNIT	mm	



名称 NAME	FP0707TCD			備考 NOTE
DRAWING NO.	CV536	単位 UNIT	mm	