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SPECIFICATIONS

Product Type DIGITAL SIGNAL PROCESSOR FOR COLOR CCD CAMERA

Model No. LR38266

※This specification contains 31 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED

BY: K. Misawa

K. MISAWA
Dept. General Manager

REVIEWED BY: S. Yoshida

PREPARED BY: I. Yata

Engineering Dept. 3
Logic IC Engineering Center
Tenri Integrated Circuits Development Group
SHARP CORPORATION

●When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following applications areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

●Please direct all queries regarding the products covered herein to a sales representative of the company.

CONTENTS

1. GENERAL

This is the digital signal processor for color CCD camera system of 270K, 320K, 410K and 470K pixels CCD with the complementary color filter. The camera system consists of CDS·AGC·AD IC(IR3Y38M), DSP IC(LR38266), Timing IC (LR38277 / LR38278 / LR38578 / LR38581), and Microcomputer IC (LU850410 / LU850420).

1-1. FEATURES

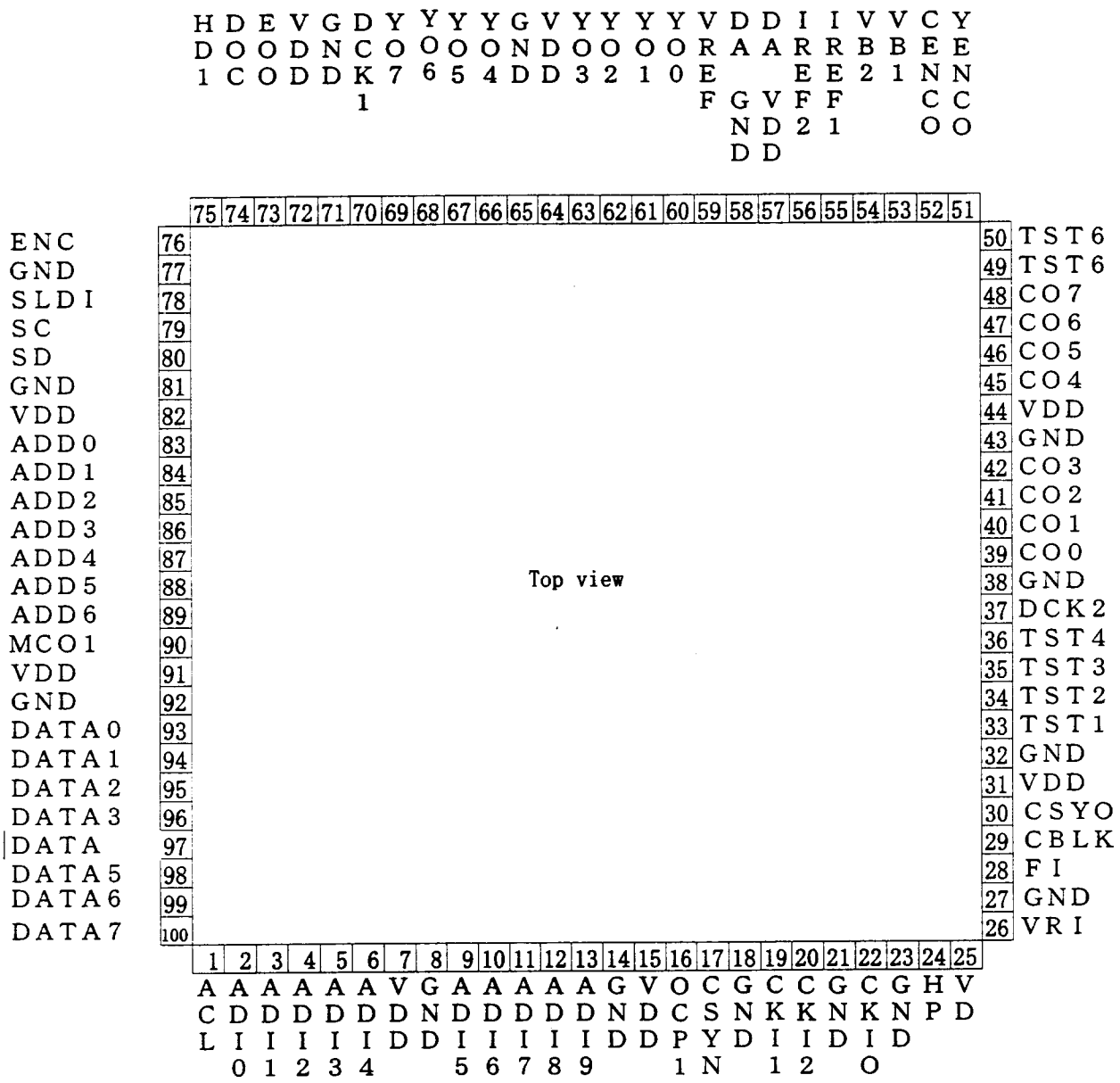
- The process (structure) is CMOS.
- A P-type silicon circuit board is used.
- The package type is 100-pin QFP.
- The package material is plastic.
- Not designed or rated as radiation hardened.

1-2. FUNCTIONS

- Single +3.3V power supply
- Available for 270K, 320K, 410K and 470K CCD with Mg, Cy, Ye and Gr color filter
- Available for NTSC and PAL
- External performance control
- Variable GAMMA and KNEE response
- 8 ~ 10 bits digital input
- Analog Y & C output by built-in 8 bits 2 ch DA converter
- Either Y & U / V (16 bits) or U / Y / V / Y (8 bits) output in digital
- Line-lock and External lock function
- CPU interface Input / Output
- Accumlater to control Auto Exposure and Auto White Balance.

2. PIN ASSIGNMENT

2-1. PIN ASSIGNMENT



2-2. PIN TABLE

Pin no.	Symbol	I/O
1	ACL	ICU
2	ADI0	IC
3	ADI1	IC
4	ADI2	IC
5	ADI3	IC
6	ADI4	IC
7	VDD	-
8	GND	-
9	ADI5	IC
10	ADI6	IC
11	ADI7	IC
12	ADI8	IC
13	ADI9	IC
14	GND	-
15	VDD	-
16	OCP1	O
17	CSYN	O
18	GND	-
19	CKI1	IC
20	CKI2	IC
21	GND	-
22	CKI0	IC
23	GND	-
24	HP	O
25	VD	O

Pin no.	Symbol	I/O
26	VRI	ICS
27	GND	-
28	FI	O
29	CBLK	O
30	CSYO	O
31	VDD	-
32	GND	-
33	TST1	ICD
34	TST2	ICD
35	TST3	ICD
36	TST4	ICD
37	DCK2	O
38	GND	-
39	CO0	TO
40	CO1	TO
41	CO2	TO
42	CO3	TO
43	GND	-
44	VDD	-
45	CO4	TO
46	CO5	TO
47	CO6	TO
48	CO7	TO
49	TST5	ICD
50	TST6	ICD

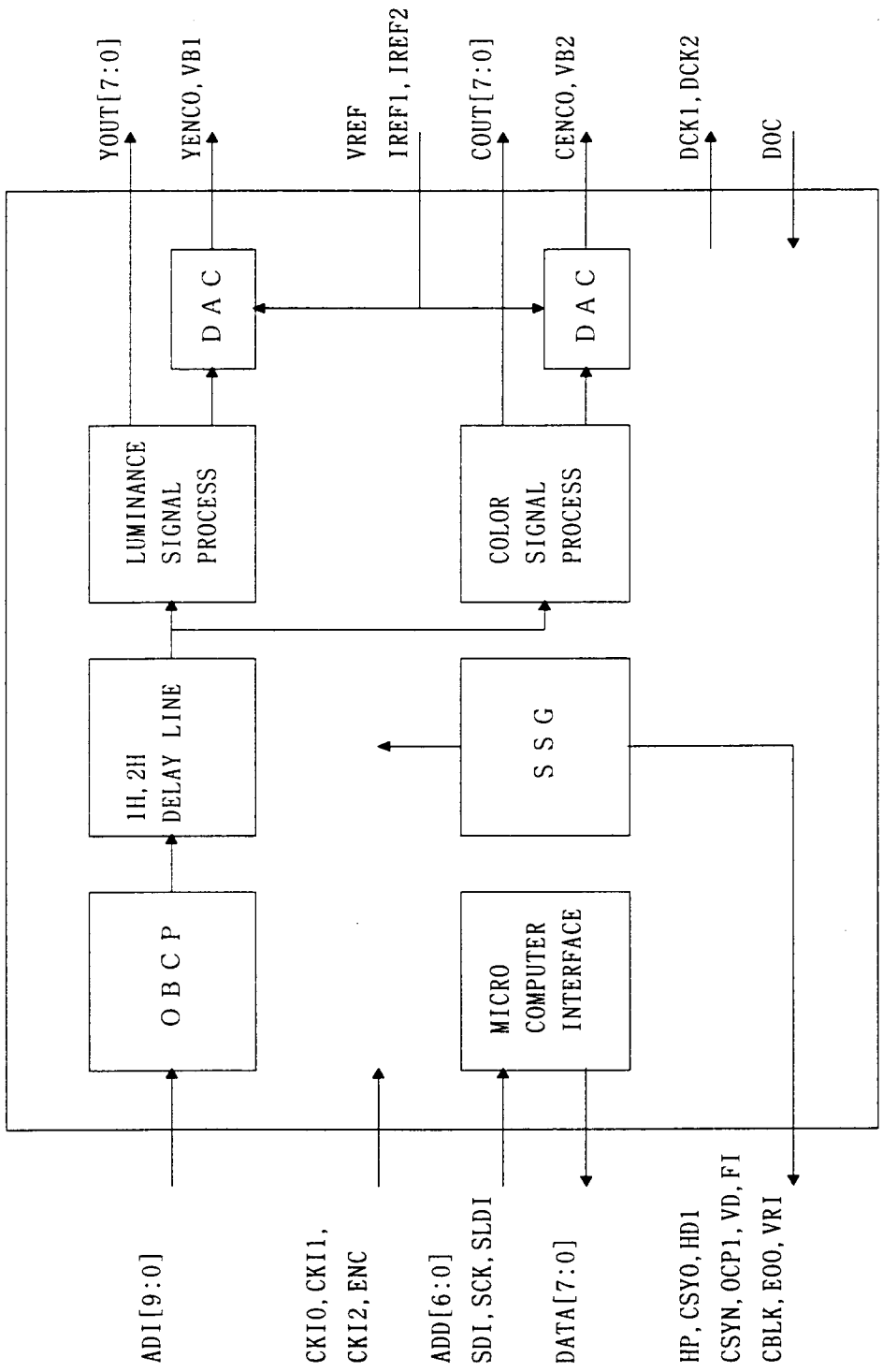
Pin no.	Symbol	I/O
51	YENCO	DAO
52	CENCO	DAO
53	VB1	DAO
54	VB2	DAO
55	IREF1	DAO
56	IREF2	DAO
57	DA VDD	-
58	DA GND	-
59	VREF	DAI
60	YO0	TO
61	YO1	TO
62	YO2	TO
63	YO3	TO
64	VDD	-
65	GND	-
66	YO4	TO
67	YO5	TO
68	YO6	TO
69	YO7	TO
70	DCK1	O
71	GND	-
72	VDD	-
73	EO0	XTO
74	DOC	ICD
75	HD1	O

Pin no.	Symbol	I/O
76	ENC	IC
77	GND	-
78	SLDI	IC
79	SCK	IC
80	SDI	IC
81	GND	-
82	VDD	-
83	ADD0	IC
84	ADD1	IC
85	ADD2	IC
86	ADD3	IC
87	ADD4	IC
88	ADD5	IC
89	ADD6	IC
90	MCO1	O
91	VDD	-
92	GND	-
93	DATA0	O
94	DATA1	O
95	DATA2	O
96	DATA3	O
97	DATA4	O
98	DATA5	O
99	DATA6	O
100	DATA7	O

IC : Input pin under the condition of CMOS 3.3 V
ICU : Input pin under the condition of CMOS 3.3 V with a pull-up register
ICD : Input pin under the condition of CMOS 3.3 V with a pull-down register
ICS : Input pin under the condition of Schmidt 3.3 V with a pull-down register
DAI : Input pin for DA converter

O : Output pin with 2 mA 3.3 V
TO : Tri-state output pin with 2 mA 3.3 V
XTO : Tri-state output pin with 2 mA 3.3 V
DAO : DA converter output pin

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

NO.	SYMBOL	POLARITY	I/O	FUNCTION
1	ACL	—	ICU	All reset input. The internal circuit is initialized at power-on with a capacitor of 0.01 μF.
2	ADI0	—	IC	ADI0 ~ ADI9 are Digital signal inputs.
3	ADI1	—	IC	ADI0 is LSB.
4	ADI2	—	IC	ADI9 is MSB.
5	ADI3	—	IC	
6	ADI4	—	IC	
7	VDD	—	-	+3.3 V input
8	GND	—	-	Ground
9	ADI5	—	IC	
10	ADI6	—	IC	
11	ADI7	—	IC	
12	ADI8	—	O	
13	ADI9	—	O	
14	VDD	—	-	+3.3 V input
15	GND	—	-	Ground
16	OCP	—	O	Opticalblack clamp pulse output
17	CSYNC	—	O	Composite sync. pulse output for analog video output.
18	GND	—	-	Ground
19	CKI1	—	IC	Clock input. The frequency is below for each CCD. 270K, 410K CCD : 14.31818 MHz 320K, 470K CCD : 14.1875 MHz
20	CKI2	—	IC	Clock input. The frequency is below for each CCD. 270K CCD : 9.5454 MHz 320K CCD : 9.4583 MHz 410K CCD : 14.3181 MHz 470K CCD : 14.1875 MHz
21	GND	—	-	Ground
22	CKI0	—	IC	Clock input. The frequency is below for each CCD. 270K, 410K CCD : 28.6363 MHz 320K, 470K CCD : 28.3750 MHz
23	GND	—	IC	Ground
24	HP	—	O	Horizontal drive pulse output.
25	VD	—	O	Vertical drive pulse output.
26	VRI	—	O	Vertical reset input. Built-in vertical counter is reset by a Low-input more than one horizontal period.
27	GND	—	O	Ground
28	FI	—	O	Field index pulse output.
26	VRI	—	O	Vertical reset input. Built-in vertical counter is reset by a Low-input more than one horizontal period.
27	GND	—	O	Ground

NO.	SYMBOL	POLARITY	I/O	FUNCTION
28	FI	—	O	Field index pulse output.
29	CBLK	—	O	Composite blanking pulse output.
30	CSYO	—	O	Composite sync. pulse output. Output timing is vaiable by output mode.
31	VDD	—	-	+3.3 V input.
32	GND	—	-	Ground.
33	TST1	—	ICD	Test input. Connected to Low or Open.
34	TST2	—	ICD	Test input. Connected to Low or Open.
35	TST3	—	ICD	Test input. Connected to Low or Open.
36	TST4	—	ICD	Test input. Connected to Low or Open.
37	DCK2	—	O	Clock output for digital Cout.
38	GND	—	—	Ground.
39	CO0	—	O	8 bits digital color signal output. CO0 is LSB. CO7 is MSB.
40	CO1	—	O	
41	CO2	—	O	
42	CO3	—	O	
43	GND	—	O	Ground
44	VDD	—	O	+3.3 V input.
45	CO4	—	O	
46	CO5	—	O	
47	CO6	—	O	
48	CO7	—	O	
49	TST5	—	ICD	Test input. Connected to Low or Open.
50	TST6	—	ICD	Test input. Connected to Low or Open.
51	YENCO	—	OA	Analog Y signal output.
52	CENCO	—	OA	Analog C signal output.
53	VB1	—	DAO	Bias voltage input for built-in DA.
54	VB2	—	DAO	Bias voltage input for built-in DA.
55	IREF1	—	DAO	YENCO output voltage amplitude adjustment.
56	IREF2	—	DAO	CENCO output voltage amplitude adjustment.
57	VDD	—	-	+3.3 V input for built-in DA converter.
58	GND	—	-	Ground for built-in DA converter.
59	VREF	—	DAI	Reference voltage input for built-in DA converter.
60	YO0	—	TO	Y digital outputs. YO0 is LSB. YO7 is MSB.
61	YO1	—	TO	
62	YO2	—	TO	
63	YO3	—	TO	
64	VDD	—	-	+3.3 V input.
65	GND	—	-	Ground.
66	YO4	—	TO	
67	YO5	—	TO	

NO.	SYMBOL	POLARITY	I/O	FUNCTION
68	YO6	—	TO	
69	YO7	—	TO	
70	DCK1	—	O	Clock output for YO output.
71	GND	—	-	Ground.
72	VDD	—	-	+3.3 V input.
73	EOO	—	TO	Phase detector output comparing internal HD and HD1.
74	DOC	—	ICD	Control input of YO and CO. H level sets both YO and CO High-impeadance.
75	HD1	—	O	Horizontal drive pulse generated from ENC of pin 76.
76	ENC	—	IC	Clock input to encorde color signal. Internal sync. mode : CKI2 Line lock mode same as CCD CLOCK from outside or 4fsc
77	GND	—	-	Ground.
78	SLDI	—	IC	Data input to set each coefficient of DSP.
79	SCK	—	IC	Clock pulse input to set SLDI data to DSP.
80	SDI	—	IC	Timing pulse input to set SLDI data to DSP.
81	GND	—	-	Ground.
82	VDD	—	-	+3.3 V input.
83	ADDO	—	IC	Address input to choose a output data of DATA pins used in Auto white balance and Auto iris. The detail is shown at other page.
84	ADD1	—	IC	
85	ADD2	—	I	
86	ADD3	—	O	
87	ADD4	—	I	
88	ADD5	—	—	
89	ADD6	—	I	
90	MCO1	—	—	Control input to update an internal data stored in DSP register. Data is updated at the rising edge of MCO1.
91	VDD	—	-	+3.3 V input.
92	GND	—	-	Ground.
93	DATAO	—	IC	Data output to control Auto white balance and Auto iris. Data of address set by ADD inputs is output.
94	DATA1	—	IC	
95	DATA2	—	IC	
96	DATA3	—	IC	
97	DATA4	—	IC	
98	DATA5	—	IC	
99	DATA6	—	IC	
100	DATA7	—	IC	

5. Electric characteristics

5-1. Absolute Maximum Ratings

ITEM	SYMBOL	RATING	UNIT
Power supply voltage	VDD	−0.3 ～ 4.6	V
Input voltage	VI	−0.3 ～ VDD+0.3	V
Output voltage	VO	−0.3 ～ VDD+0.3	V
Storage temperature	Tstg	−55 ～ 150	℃

5-2. Operating Conditions

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Power supply voltage	VDD	3.0	3.3	3.6	V
Operating temperature	Topr	−10	25	70	℃
Clock input	Fck		28.6		MHz

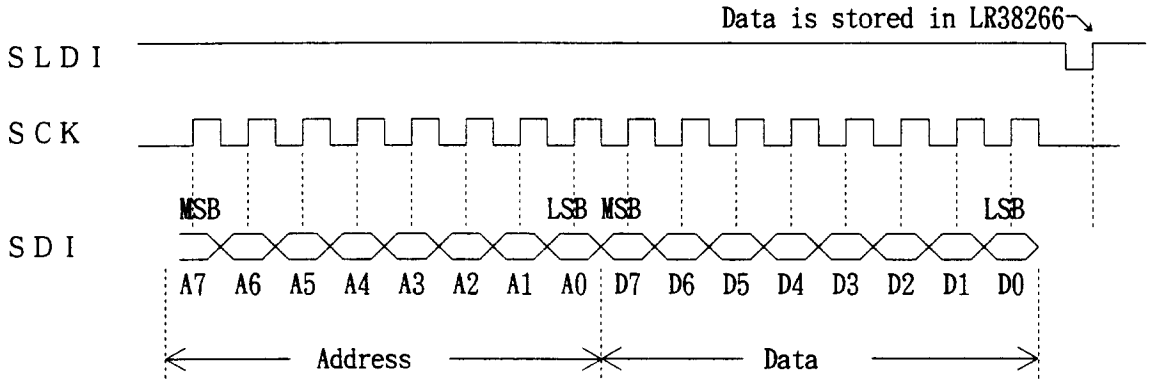
5-3. Electric operating characteristics (VDD = +3.3 V±10 %, Ta = -20～70℃)

ITEM	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
L level input voltage	VIL				0.2VDD	V	1
H level input voltage	VIH		0.8VDD			V	
L level input voltage	VT-				0.2VDD	μA	2
H level input voltage	VT+		0.8VDD				
Hysterisis voltage			0.2				
L level output voltage	VOL1	IOL = -1.6 mA			0.1VDD	V	3
H level output voltage	VOH2	IOH = 0.8 mA	0.9VDD			V	
Output leak current	IOZ	High-impeadance	-1.0		1.0	μA	
L level output voltage	VOL1	IOL = -1.6 mA			0.1VDD	V	4
H level output voltage	VOH2	IOH = 0.8 mA	0.9VDD			V	
Output leak current	IOZ	High-impeadance	-1.0		1.0	μA	
Input current	IOL1	VIN = 0 V		10		μA	5
Input current	IOH2	VIN = VDD		10		μA	6
L level output voltage	VOL1	IOL = -1.6 mA			0.1VDD	V	7
H level output voltage	VOH2	IOH = 0.8 mA	0.9VDD			V	
Resolution	RES			8		Bit	8
Linearity Error	EL	Vref = 1.0 V			±3.0	LSB	
Differential error	ED	Rref = 4.8 KΩ			±1.0	LSB	
Full scale current	IFS	Rout = 75 Ω		13		mA	
Reference voltage	V ref			1.0		V	9
Reference register	R ref			4.8		KΩ	10
Output load register	R out			75		Ω	11

1 : Input pins (IC, ICD, ICU)
2 : Input pins (ICS)
3 : Output pins (TO)
4 : Output pins (XTO)
5 : Input pins (ICU)
6 : Input pins (ICD)
7 : Output pins (O)
8 : Output pins (YENCO, CENCO)
9 : Input pins (REF)
10 : Input pins (IREF1, IREF2)
11 : Output pins (YENCO, CENCO)

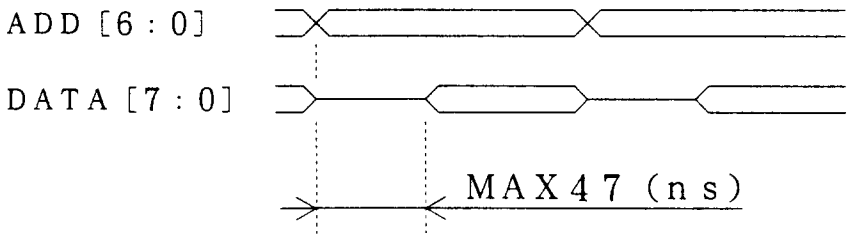
5-4. DATA INTERFACE TIMING.

5-4-1 DATA INPUT



SCK should be slower than 20MHz

5-4-2 DATA OUTPUT



Data output in 47ns or more after Address input is valid.

6. Detail explanation

6-1. CCD

CCD type out of 270K, 320K, 410K and 470K pixels is selected by ADR 01H.

6-2. Output signal format

(1) Analog video signal output

Built-in DA converters outputs Luminance (Y) signal without CSYNC. and modulated color signal of NTSC or PAL.

Stand-by mode of DA converter makes DA output pins High impeadance.

(2) Digital video signal output (ADR 01H)

One out of below three format is selectable by ADR 01H. High level of pin 74 as DOC makes all digital output pins High impeadance.

1. 8 bits Y and 8 bits C
2. 8 bits Y and 8 bits U / V
3. 8 bits U / Y / V / Y

6-3. Camera control data output

(1) Iris control data output (64 data with 8 bits and 2 data with 8 bits)

An Averaged Luminance level of each block, which are 64 blocks gotten by the 8 X 8 spread in user-defined image area by ADR., are at DATA output pins.

In the defined area, there are the maximum Luminance level and the minimum Luminance level at DATA output pins.

(2) White balance control data output (two kinds of 16 data with 8 bits)

Averaged color signal levels of either both I and Q or both R-Y and B-Y, which are 16 blocks gotten by the 4 X 4 spread of user-defined image area by ADR., are at DATA output pins.

(3) Black balance control data output (3 data with 8 bits)

Below three kinds of outputs are at DATA output pins.

* An average signal of CCD optical-black portion consisting of 4 pixels per Horizontal line for 128 Horizontal lines located in the image center.
* An average signal of CCD optical-black portion consisting of 2 pixels per Horizontal line for 128 Horizontal lines located in the image center. which is available to tune the base level of Mg + Ye color signal component.
* An average signal of CCD optical-black portion consisting of 2 pixels per Horizontal line for 128 Horizontal lines located in the image center. which is available to tune the base level of Mg + Cy color signal component.

6-4. Camera signal processing

(1) Optical-black signal clamping

The optical -black signal portion is clamped so as to be 64H by using the average level of the input digital signal. The averaging is done every field.

(2) Horizontal period delay line

There are two Horizontal delay lines in this IC for camera signal processing.

(3) Digital filter for Luminance signal

There are Low pass filter to make Y signal from colr CCD signal.

(4) Gamma correction for Luminance signal

10 bits input signal is converted to 8 bits signal with a gamma curve defined by 10 straight lines. A slope and position of every straight line is settable by ADR.

(5) Edge enhancement of Luminance signal

After Gamma correction, the edge of Luminance signal is enhanced in both Horizontal and Vertical. How to enhance is tunable by ADR..

(6) Set-up level of Luminance signal

The set-up level is tunable by ADR..

(7) Polarity option and level tuning of Luminance signal

The polarity of input signal from AD converter can be inverted before filtering.
The DC offset level and the amplitude is tunnable by ADR..

(8) Masking Luminance signal

The restricted area in whole image is settable by ADR..
The iris function and the auto white balance function can be done only in the restricted area.

(9) Extract of Color signal component

Color signal components are extracted by below processing.

Red = (Mg + Ye) - K1 (G + Cy)

Blue = (Mg + Cy) - K2 (G + Ye)

YL = ((Mg + Ye) + (G + Cy) + (Mg + Cy) + (G + Ye)) / 4

K1 and K2 are variable by ADR..

(10) Digital filter of Color signal component

Red, Blue and YL are passed to limit each bandwidth so as to be half of extracted signals by low pass filters.

(11) Black level clamping of Color signal component

The black level of Red and Blue signal can be tuned by ADR 15, 16, 17, and 18.

(12) White balance

The amplitude of Red and Blue sugnal can be tuned by ADR. 19, 1A, 1B, and 1C so as to White balance situation.

(13) Color Gamma correction

10 bits input signal of Red, Blue and YL signal is converted to 8 bits signal with Gamma curve defined by 10 straight lines.
A slope and position of every straight line is settable by ADR..

(14) Color matrix correction

Color rendition can be tuned by ADR. 1D and 1E under below equation.

R - Y = (R - Y) + K1 (B - Y)

B - Y = (B - Y) + K2 (R - Y)

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(15) Color level adjustment

The amplitude of R - Y and B - Y can be tuned by ADR. 1F and 20.

(16) Color level suppression

The faluse color signal at both the transient portion of Luminance signal and the high-light portion of Luminance signal can be suppressed by ADR. 2B, 2C, 2D, 2E, 30, 31, 32, 33, 34 and 35.

(17) Polarity option and level tuning of Color signal

The polarity of color component signal can be inverted before Gamma correction. The DC offset level and the amplitude is tunnable by ADR. 36, 37, 38 and 39.

(18) NTSC/PAL Color signal encoder

R - Y and B - Y color signal are modulated under NTSC or PAL format.
Modulated clock frequency and TV format are chosen by ADR. 03, 21, 22 and 23.
Line-lock system requires the clock generater outside LR38266.

(19) Accumlater to control the exposure

Below three kinds of output data become available by ADR. A0, 00 - 3F, 60 and 61.

Average signal in either whole image or restricted area
Maximum signal in either whole image or restricted area
Minimum signal in either whole image or restricted area

(20) Accumlater to control White balance

Below output data become available by ADR. 24, 25, 26, 27, 28, 29, 2A, A0 and 4F - 5F.

Average signal of I (R - Y) and Q (B - Y) in 16 area of whole image
These data can be weighted by both the color zone of I - axis and/or Q - axis and the range of Luminance range.

(21) Accumlater to control color black balance

Average signal of the optical black portion to clamp the black level of color signal is available by ADR. 62, 63 and 64.

(22) Others

* The output timing of Synchronus Sync. signal is available by ADR. 06, 07 and 08.
* Functions like Stand-by, Muting etc. are available by ADR. 01, 03, 04 and 21.

6-5. Internal coefficient table

6-5-1. System setting

ADDRESS	LABEL	Data range	CONTENTS
01 H	OMOD	7 bits	CCD option, output format option
02 H	MODE1	7 bits	Mode setting
03 H	MODE2	5 bits	Mode setting
04 H	MODE3	6 bits	Mode setting
06 H	CSYNCVARI	8 bits	Position tuning of Csync with the range from + 8 clock to - 7 clock of CKI1 Upper 4 bits:CSYNC, Lower 4 bits:CSYO
07 H	CBLKBALI	8 bits	Position tuning of CBLK with the ditto range
08 H	CB_BFVARI	8 bits	Position tuning of internal BLK with the range from + 1 clock to - 1 clock of CKI2.

ADR. 01 : OMOD (Default data : *0010110)

Bit	LABEL	CONTENTS		
7	*	Not used		
6	STB DA	Stand-by of DA converter 1: Stand-by		
5	OUTPUT2	Output format option	bit4=0 Y/C (bit5=0)	U/Y/V/Y (bit5=1)
4	OUTPUT1	Output format option	bit4=1 Y, U/V (bit5=0)	Prohibited (bit5=1)
3	TVMD	TV format option 0 : NTSC, 1 : PAL		
2	TYPE2	CCD option	bit2=0	bit2=1
1	TYPE1	CCD option	bit1=0 270K/320K with Mirror	Prohibited
			bit1=1 270K/320K	410K/470K
0	MIR	Image type option 0 : Normal, 1 : Mirror		

ADR. 02 : MODE1 (Default data : *0000000)

Bit	LABEL	CONTENTS
7	*	Not used
6	ADTI1	Input data is delayed by 1 clock 0 : Not delayed 1 : delayed
5	ADTI2	The clock type to input the data 0 : Non-inverted 1 : inverted
4	APTVC	Vertical edge enhancement 0 : ON, 1 : OFF
3	APTHC	Horizontal edge enhancement 0 : ON, 1 : OFF
2	CKIL	Color killer function 0 : ON, 1 : OFF
1	MUTE D	Muting Digital signal outputs 0 : OFF, 1 : ON
0	MUTE A	Muting Analogue signal outputs 0 : OFF, 1 : ON

ADR. 03 : MODE2 (Default data : ***00000)

Bit	LABEL	CONTENTS	
7	*	Not used	
6	*	Not used	
5	*	Not used	
4	EOOCTRL	The polarity of EOO output	0 : Normal
3	INVSP	The polarity of SP1, SP2	0 : Normal
2	HGCO	The polarity of HG	0 : Normal
1	INTL	Interlace / Non-Interlace	0 : Interlace
0	EX_SXB	Stand-by of EOO function	0 : Stand-by

ADR. 04 : MODE3 (Default data : **00*000)

Bit	LABEL	CONTENTS	
7	*	Not used	
6	*	Not used	
5	TESYL	Set YL zero in color processing	0 : OFF, 1 : ON
4	K1	Prohibited to change	0 : Should be kept
3	*	Not used	
2	RAM_ST	Stand-by of Delay lines	0 : OFF, 1 : ON
1	SEL_UV	The option of U/V sequence	0 : Normal
0	SEL_RB	The option of R/B sequence	0 : Normal

ADR. 08 : CB_BFVARI (Default data : 00000000)

Bit	LABEL	CONTENTS			
7	CBK_Y	The position tuning of Y-CBLK		bit7=0	bit7=1
6	CBK_Y	by CKI2 clock	bit6=0	No tune	-1 clock
			bit6=1	1 clock	-1 clock
5	CBLK_C	The position tuning of modulated		bit5=0	bit5=1
4	CBLK_C	C-CBLK by CKI2 clock	bit4=0	No tune	-1 clock
			bit4=1	1 clock	-1 clock
3	CBLK_UV	The position tuning of baseband		bit3=0	bit3=1
2	CBLK_UV	C-CBLK by CKI2 clock	bit2=0	No tune	-1 clock
			bit2=1	1 clock	-1 clock
1	BFVARI	The position tuning of color		bit1=0	bit1=1
0	BFVARI	burst signal by CKI2 clock	bit0=0	No tune	-1 clock
			bit0=1	1 clock	-1 clock

ADR. 21 : ENC MO (Default data : ****0000)

Bit	LABEL	CONTENTS
7	*	Not used
6	*	Not used
5	*	Not used
4	*	Not used
3	ENC TI	The clock type of Encoder input 0 : Non-Inverte 1 : Inverted
2	L fsc	Latched by fsc clock before Encode 0 : Latched 1 : Non-Latched
1	MO ENC	Encoding phase of PAL 0 : 4 phase 1 : 16/5 phase
0	MUTE E	Muting color signal at Encoder 0 : Normal 1 : Muting

ADR. 2E : CKI HLTI (Default data : *000*000)

Bit	LABEL	CONTENTS		
7	*	Not used	bit6, bit5, bit4	000 : No tuning
6	HT SIG	Color killer timing	001	1 clock delay
5	HT 1	at Higher Luminance	010, 011	2 clocks delay
4	HT 0		100, 101, 110	2 clocks advance
3	*	Not used	111	1 clock advance
2	LT SIG	Color killer timing	bit2, bit1, bit0	000 : No tuning
1	LT 1	at Lower Luminance	001	1 clock delay
0	LT_0		010, 011	2 clocks delay
			100, 101, 110	2 clocks advance
			111	1 clock advance

ADR. 32 : CKI ETI (Default data : 0000*000)

Bit	LABEL	CONTENTS		
7	SEL ESFT	Level of Edge signal	0 : 1/4 times	1 : 1 times
6	VET SIG	Color killer timing	bit6, bit5, bit4	000 : No tuning
5	VET 1	at Vertical transient	001	1 clock delay
4	VET 0	portion	010, 011	2 clocks delay
3	*	Not used	100, 101, 110	2 clocks advance
			111	1 clock advance
2	HET SIG	Color killer timing	bit2, bit1, bit0	000 : No tuning
1	HET 1	at Horizontal transient	001	1 clock delay
0	HET_1	portion	010, 011	2 clocks delay
			100, 101, 110	2 clocks advance
			111	1 clock advance

ADR. 35 : C_ETC (Default data : *****000)

Bit	LABEL	CONTENTS
7	*	Not used
6	*	Not used
5	*	Not used
4	*	Not used
3	*	Not used
2	C_NE1	The polarity of color signal 0 : Normal 1 :Inverted
1	C_NE2	The polarity of color signal at Gamma outp 0 : Normal 1 :Inverted
0	BLK_CTRL	CBLK availability at output 0 : ON 1 : OFF

ADR. 67 : VARI_Y (Default data : ***00000)

Bit	LABEL	CONTENTS
7	*	Not used
6	*	Not used
5	*	Not used
4	6ADV	1 : 6 clocks advance of Luminance signal 0 : No variation
3	8ADV	1 : 8 clocks advance of Luminance signal 0 : No variation
2	4DLY	1 : 4 clocks delay of Luminance signal 0 : No variation
1	2DLY	1 : 2 clocks delay of Luminance signal 0 : No variation
0	1DLY	1 : 1 clock delay of Luminance signal 0 : No variation

ADR. 69 : Y_NE (Default data : ****0000)

Bit	LABEL	CONTENTS
7	*	Not used
6	*	Not used
5	*	Not used
4	*	Not used
3	Y_MUTE	Muting analog Luminance signal output 0 : Normal 1 : Muting
2	CBLK_OFF	CBLK availability for Luminance signal 0 : ON 1 : OFF
1	SEL_BLK	Pedistal level of Luminance signal 0 : 16th step 1 : 0 step
0	Y_NEGA	The polarity of Luminance signal 0 : Normal 1 : Inverted

6-5-2. Mask function coefficient

ADDRESS	LABEL	Data range	CONTENTS
A0 H	MSK_M0	8 bits	Mask mode option
A1 H	HMSKF_U	2 bits	Upper 2 bits of starting point to mask in Horizontal
A2 H	HMSKF_L	8 bits	Lower 8 bits of starting point to mask in Horizontal
A3 H	HMSKR_U	2 bits	Upper 2 bits of ending point to mask in Horizontal
A4 H	HMSKR_L	8 bits	Lower 8 bits of ending point to mask in Horizontal
A5 H	VMSKF_U	1 bits	Upper 1 bit of starting point to mask in Vertical
A7 H	VMSKF_L	8 bits	Lower 8 bits of starting point to mask in Vertical
A8 H	VMSKR_U	1 bits	Upper 1 bit of ending point to mask in Vertical
A9 H	VMSKR_L	8 bits	Lower 8 bits of ending point to mask in Vertical

ADR. A0 : MSK_M0 (Default data : 00000000)

Bit	LABEL	CONTENTS
7	SEL_WBD	The option of White balance data equation 0 : Accumlated data / Image area 1 : Accumlated data / Number of data
6	PEAK4_8	The option to detect Peak level to control the exposure 0 : Accumlated data of 4 pixels 1 : Accumlated data of 8 pixels
5	PEAHA_H	The area in Horizontal to detect Peak level to control the exposure 0 : OFF 1 : ON
4	PEAKA_V	The area in Vertical to detect Peak level to control the exposure 0 : OFF 1 : ON
3	I_WBA_H	The area in Horizontal to detect Average level to control both the exposure and White balance 0 : OFF 1 : ON
2	I_WBA_V	The area in Vertical to detect Average level to control both the exposure and White balance 0 : OFF 1 : ON
1	MASK_H	Horizontal Mask signal availability 0 : OFF 1 : ON
0	MASK_V	Vertival Mask signal availability 0 : OFF 1 : ON

6-5-3. Internal coefficient for Color signal processing

ADDRESS	LABEL	Data range	CONTENTS
11 H	CSP_R1	8 bits	Coefficient to extract Red color component
12 H	CSP_B1	8 bits	Coefficient to extract Blue color component
13 H	CSP_R2	7 bits	Coefficient to tune the base level of Red signal
14 H	CSP_B2	7 bits	Coefficient to tune the base level of Blue signal
15 H 16 H	CB_R1 CB_R2	6 bits 8 bits	Coefficient of the black balance of Red signal (15H) MSB:sign, other 5bits:upper 5bits of coefficient (16H) lower 8bits of coefficient
17 H 18 H	CB_B1 CB_B2	6 bits 8 bits	Coefficient of the black balance of Blue signal (17H) MSB:sign, other 5bits:upper 5bits of coefficient (18H) lower 8bits of coefficient
19 H 1A H	WB_R1 WB_R2	1 bit 8 bits	Upper coefficient to make White balance of Red signal (19H) MSB of coefficient (1AH) lower 8bits
1B H 1C H	WB_B1 WB_B2	1 bit 8 bits	Upper coefficient to make White balance of Blue signal (1BH) MSB of coefficient (1CH) lower 8bits
1D H	MAT_R-Y	6 bits	Coefficient of R-Y matrix (MSB) sign bit
1E H	MAT_B-Y	6 bits	Coefficient of B-Y matrix (MSB) sign bit
1F H	GA_R-Y	6 bits	Coefficient of R-Y gain
20 H	GA_B-Y	6 bits	Coefficient of B-Y gain
21 H	ENC_M0	1 bit	Encorder mode select (See other page in detail)
22 H	BAS_R-Y	8 bits	Coefficient of color burst level at R-Y (MSB) sign bit
23 H	BAS_B-Y	8 bits	Coefficient of color burst level at B-Y (MSB) sign bit
24 H	WBA_IP	8 bits	Positive range of white color signal at I-axis
25 H	WBA_IM	8 bits	Negative range of white color signal at I-axis
26 H	WBA_QP	8 bits	Positive range of white color signal at Q-axis
27 H	WBA_QM	8 bits	Negative range of white color signal at Q-axis
28 H	WBA_SEL	2 bits	Option of color signal type I/Q or R-Y/B-Y
29 H	WB_HCL	8 bits	Limitter of AWB function at higher Luminance level
2A H	WB_LCL	8 bits	Limitter of AWB function at lower Luminance level
2B H	CKI_HCL	8 bits	Color suppression point at higher Luminance level
2C H	CKI_LCL	8 bits	Color suppression point at lower Luminance level
2D H	CKI_HLGA	8 bits	Luminance level to suppress color signal Upper 4 bits : higher Luminance level Lower 4 bits : lower Luminance level

ADDRESS	LABEL	Data range	CONTENTS
2E H	CKI_HLTI	6 bits	Luminance signal position to suppress color signal
2F H	CKI_HECL	8 bits	Horizontal aperture level to suppress color signal
30 H	CKI_VECL	8 bits	Vertical aperture level to suppress color signal
31 H	CKI_EGA	8 bits	Aperture level to suppress color signal Upper 4 bits : Vertical aperture level Lower 4 bits : Horizontal aperture level
32 H	CKI_ETI	8 bits	Color suppress mode (See other page in detail)
33 H	CKI_LEV	8 bits	Level to suppress color signal
34 H	NSUP_R-Y	8 bits	Coring level of R-Y signal
35 H	NSUP_B-Y	8 bits	Coring level of B-Y signal
36 H	C-ETC	2 bits	Color signal mode (See other page in detail)
37 H	YL_SFT1	2 bits	Base level of YL signal (37H) Upper 2bits of coefficient (38H) lower 8bits of coefficient
38 H	YL_SFT2	8 bits	
39 H	YL_AMP	8 bits	YL signal level to make R-Y and B-Y
40 H	CGAM-A1	8 bits	1st input range of Color Gamma correction
41 H	CGAM-A2	8 bits	2nd input range of Color Gamma correction
42 H	CGAM-A3	8 bits	3rd input range of Color Gamma correction
43 H	CGAM-A4	8 bits	4th input range of Color Gamma correction
44 H	CGAM-A5	8 bits	5th input range of Color Gamma correction
45 H	CGAM-A6	8 bits	6th input range of Color Gamma correction
46 H	CGAM-A7	8 bits	7th input range of Color Gamma correction
47 H	CGAM-A8	8 bits	8th input range of Color Gamma correction
48 H	CGAM-A9	8 bits	9th input range of Color Gamma correction
49 H	CGAM-P1	8 bits	Offset of 1st straight line at Color Gamma correction
4A H	CGAM-P2	8 bits	Offset of 2nd straight line at Color Gamma correction
4B H	CGAM-P3	8 bits	Offset of 3rd straight line at Color Gamma correction
4C H	CGAM-P4	8 bits	Offset of 4th straight line at Color Gamma correction
4D H	CGAM-P5	8 bits	Offset of 5th straight line at Color Gamma correction
4E H	CGAM-P6	8 bits	Offset of 6th straight line at Color Gamma correction
4F H	CGAM-P7	8 bits	Offset of 7th straight line at Color Gamma correction
50 H	CGAM-P8	8 bits	Offset of 8th straight line at Color Gamma correction
51 H	CGAM-P9	8 bits	Offset of 9th straight line at Color Gamma correction
52 H	CGAM-P10	8 bits	Offset of 10th straight line at Color Gamma correction
53 H	CGAM-F	1 bit	Polarity of Color Gamma correction 0:+, 1:-
54 H	CGAM-S1	8 bits	Slope of 1st straight line at Color Gamma correction

ADDRESS	LABEL	Data range	CONTENTS
55 H	CGAM-S2	8 bits	Slope of 2nd straight line at Color Gamma correction
56 H	CGAM-S3	8 bits	Slope of 3rd straight line at Color Gamma correction
57 H	CGAM-S4	8 bits	Slope of 4th straight line at Color Gamma correction
58 H	CGAM-S5	8 bits	Slope of 5th straight line at Color Gamma correction
59 H	CGAM-S6	8 bits	Slope of 6th straight line at Color Gamma correction
5A H	CGAM-S7	8 bits	Slope of 7th straight line at Color Gamma correction
5B H	CGAM-S8	8 bits	Slope of 8th straight line at Color Gamma correction
5C H	CGAM-S9	8 bits	Slope of 9th straight line at Color Gamma correction
5D H	CGAM-S10	8 bits	Slope of 10th straight line at Color Gamma correction

6-5-4. Internal coefficient for Luminance signal processing

ADDRESS	LABEL	Data range	CONTENTS
60 H	SETUP	6 bits	Set up level of Luminance signal
61 H	APT HGA	5 bits	Horizontal aperture gain
62 H	APT HCL	7 bits	Coring level of Horizontal aperture signal
63 H	APT VGA	5 bits	Vertical aperture gain
64 H	APT VCL	7 bits	Coring level of Vertical aperture signal
65 H			Not used
66 H	VARI MASK	4 bits	Position to erase color signal by Luminance mask signal
67 H	VARI Y	5 bits	Position of Luminance signal (See other in detail)
68 H	HVARI	2 bits	Position of Horizontal aperture signal
69 H	Y NE	4 bits	Luminance signal mode (See other page in detail)
6A H	Y NESFT	8 bits	Base level of Luminance signal
6B H	Y NEAMP	8 bits	Luminance signal level
6C H	MASK NE	8 bits	Masking level of Luminance signal
6D H			Not used
6E H			Not used
6F H			Not used
70 H	CGAM-A1	8 bits	1st input range of Color Gamma correction
71 H	CGAM-A2	8 bits	2nd input range of Color Gamma correction
72 H	CGAM-A3	8 bits	3rd input range of Color Gamma correction
73 H	CGAM-A4	8 bits	4th input range of Color Gamma correction
74 H	CGAM-A5	8 bits	5th input range of Color Gamma correction
75 H	CGAM-A6	8 bits	6th input range of Color Gamma correction
76 H	CGAM-A7	8 bits	7th input range of Color Gamma correction

ADDRESS	LABEL	Data range	CONTENTS
77 H	CGAM-A8	8 bits	8th input range of Color Gamma correction
78 H	CGAM-A9	8 bits	9th input range of Color Gamma correction
79 H	CGAM-P1	8 bits	Offset of 1st straight line at Color Gamma correction
7A H	CGAM-P2	8 bits	Offset of 2nd straight line at Color Gamma correction
7B H	CGAM-P3	8 bits	Offset of 3rd straight line at Color Gamma correction
7C H	CGAM-P4	8 bits	Offset of 4th straight line at Color Gamma correction
7D H	CGAM-P5	8 bits	Offset of 5th straight line at Color Gamma correction
7E H	CGAM-P6	8 bits	Offset of 6th straight line at Color Gamma correction
7F H	CGAM-P7	8 bits	Offset of 7th straight line at Color Gamma correction
80 H	CGAM-P8	8 bits	Offset of 8th straight line at Color Gamma correction
81 H	CGAM-P9	8 bits	Offset of 9th straight line at Color Gamma correction
82 H	CGAM-P10	8 bits	Offset of 10th straight line at Color Gamma correction
83 H	CGAM-F	1 bit	Polarity of Color Gamma correction 0:+, 1:-
84 H	CGAM-S1	8 bits	Slope of 1st straight line at Color Gamma correction
85 H	CGAM-S2	8 bits	Slope of 2nd straight line at Color Gamma correction
86 H	CGAM-S3	8 bits	Slope of 3rd straight line at Color Gamma correction
87 H	CGAM-S4	8 bits	Slope of 4th straight line at Color Gamma correction
88 H	CGAM-S5	8 bits	Slope of 5th straight line at Color Gamma correction
89 H	CGAM-S6	8 bits	Slope of 6th straight line at Color Gamma correction
8A H	CGAM-S7	8 bits	Slope of 7th straight line at Color Gamma correction
8B H	CGAM-S8	8 bits	Slope of 8th straight line at Color Gamma correction
8C H	CGAM-S9	8 bits	Slope of 9th straight line at Color Gamma correction
8D H	CGAM-S10	8 bits	Slope of 10th straight line at Color Gamma correction
8E H			Not used
8F H			Not used

6-6. Output data

6-6-1. Output data table

ADDRESS	LABEL	Data range	CONTENTS
00 ~ 07 H	IRIS-1-1~8	8 bits	Average data to control the exposure
08 ~ 0F H	IRIS-2-1~8	8 bits	Average data to control the exposure
10 ~ 17 H	IRIS-3-1~8	8 bits	Average data to control the exposure
18 ~ 1F H	IRIS-4-1~8	8 bits	Average data to control the exposure
20 ~ 27 H	IRIS-5-1~8	8 bits	Average data to control the exposure
28 ~ 2F H	IRIS-6-1~8	8 bits	Average data to control the exposure
30 ~ 37 H	IRIS-7-1~8	8 bits	Average data to control the exposure

ADDRESS	LABEL	Data range	CONTENTS
38 ～ 3F H	IRIS-8-1～8	8 bits	Average data to control the exposure
40 ～ 43 H	AWBI-1-1～4	8 bits	Average data of I/R-Y axis
44 ～ 47 H	AWBI-2-1～4	8 bits	to control Auto white balance
48 ～ 4B H	AWBI-3-1～4	8 bits	Average data of Q/B-Y axis
4C ～ 4F H	AWBI-4-1～4	8 bits	to control Auto white balance
50 ～ 53 H	AWBQ-1-1～4	8 bits	Average data of I/R-Y axis
54 ～ 57 H	AWBQ-2-1～4	8 bits	to control Auto white balance
58 ～ 5B H	AWBQ-3-1～4	8 bits	Average data of Q/B-Y axis
5C ～ 5F H	AWBQ-4-1～4	8 bits	to control Auto white balance
60 H	H PEAK	8 bits	Maximium of Luminance signal out of 64 blocks
61 H	L PEAK	8 bits	Minimum of Luminance signal out of 64 blocks
62 H	OB DATA	8 bits	Average data of Optical pixels
63 H	C1 OB R	8 bits	Average data of Optical pixels for Mg+Ye
64 H	C3 OB B	8 bits	Average data of Optical pixels for Mg+Cy

6-6-2. Position of each output on image screen

(1) Luminance signal data to control the exposure

Left-Top side of Image

IRIS-1-1	IRIS-1-2	IRIS-1-3	IRIS-1-4	IRIS-1-5	IRIS-1-6	IRIS-1-7	IRIS-1-8
IRIS-2-1	IRIS-2-2	IRIS-2-3	IRIS-2-4	IRIS-2-5	IRIS-2-6	IRIS-2-7	IRIS-2-8
IRIS-3-1	IRIS-3-2	IRIS-3-3	IRIS-3-4	IRIS-3-5	IRIS-3-6	IRIS-3-7	IRIS-3-8
IRIS-4-1	IRIS-4-2	IRIS-4-3	IRIS-4-4	IRIS-4-5	IRIS-4-6	IRIS-4-7	IRIS-4-8
IRIS-5-1	IRIS-5-2	IRIS-5-3	IRIS-5-4	IRIS-5-5	IRIS-5-6	IRIS-5-7	IRIS-5-8
IRIS-6-1	IRIS-6-2	IRIS-6-3	IRIS-6-4	IRIS-6-5	IRIS-6-6	IRIS-6-7	IRIS-6-8
IRIS-7-1	IRIS-7-2	IRIS-7-3	IRIS-7-4	IRIS-7-5	IRIS-7-6	IRIS-7-7	IRIS-7-8
IRIS-8-1	IRIS-8-2	IRIS-8-3	IRIS-8-4	IRIS-8-5	IRIS-8-6	IRIS-8-7	IRIS-8-8

(2) Color signal data to control Auto white balance

Left-Top side of Image

AWBI/AWBQ-1-1	AWBI/AWBQ-1-2	AWBI/AWBQ-1-2	AWBI/AWBQ-1-2
AWBI/AWBQ-2-1	AWBI/AWBQ-2-2	AWBI/AWBQ-2-2	AWBI/AWBQ-2-2
AWBI/AWBQ-3-1	AWBI/AWBQ-3-2	AWBI/AWBQ-3-2	AWBI/AWBQ-3-2
AWBI/AWBQ-4-1	AWBI/AWBQ-4-2	AWBI/AWBQ-4-2	AWBI/AWBQ-4-2

Either I or R-Y is selectable by ADR. 28 H.

Either Q or B-Y is selectable by ADR. 28 H.

7 Package and packing specification

1. Package Outline Specification

Refer to drawing No. AA1058

2. Markings

2－1. Marking contents

(1) Product name : LR38266

(2) Company name : SHARP

(3) Date code

(Example) YY WW ×××

- YY → Denotes the production year. (Lower two digits of the year.)
- WW → Denotes the production week. (01, 02, 03, ・・・・・52, 53)
- ××× → Denotes the production ref.code (1~3)

Indicates the product was manufactured in the WWth week of 19YY.

(4) The marking of "JAPAN" indicates the country of origin.

2－2. Marking layout

Refer to drawing No. AA1058

(This layout does not define the dimensions of marking character and marking position.)

3. Packing Specification (Dry packing for surface mount packages)

Dry packing is used for the purpose of maintaining IC quality after mounting packages on the PCB (Printed Circuit Board).

When the epoxy resin which is used for plastic packages is stored at high humidity, it may absorb 0.15% or more of its weight in moisture. If the surface mount type package for a relatively large chip absorbs a large amount of moisture between the epoxy resin and insert material (e.g. chip, lead frame) this moisture may suddenly vaporize into steam when the entire package is heated during the soldering process (e.g. VPS). This causes expansion and results in separation between the resin and insert material, and sometimes cracking of the package. This dry packing is designed to prevent the above problem from occurring in surface mount packages.

3－1. Packing Materials

Material Name	Material Specificaiton	Purpose
Tray	Conductive plastic (60devices/tray)	Fixing of device
Upper cover tray	Conductive plastic (1tray/case)	Fixing of device
Laminated aluminum bag	Aluminum polyethylene (1bag/case)	Drying of device
Desiccant	Silica gel	Drying of device
P P band	Polypropylene (3pcs/case)	Fixing of tray
Inner case	Card board (600devices/case)	Packaging of device
Label	Paper	Indicates part number, quantity and date of manufacture
Outer case	Card board	Outer packing of tray

(Devices shall be placed into a tray in the same direction.)

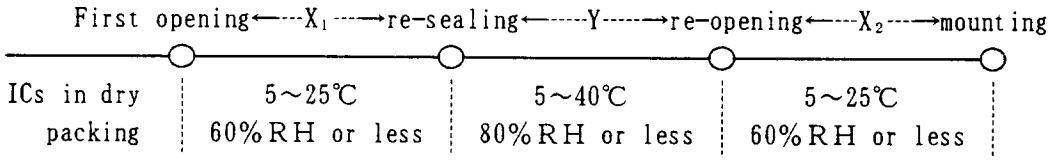
3－2. Outline dimension of tray
Refer to attached drawing.

4. Storage and Opening of Dry Packing

4－1. Store under conditions shown below before opening the dry packing
(1) Temperature range : 5～40℃
(2) Humidity : 80% RH or less

4－2. Notes on opening the dry packing
(1) Before opening the dry packing, prepare a working table which is grounded against ESD and use a grounding strap.
(2) The tray has been treated to be conductive or anti-static. If the device is transferred to another tray, use a equivalent tray.

4－3. Storage after opening the dry packing
Perform the following to prevent absorption of moisture after opening.
(1) After opening the dry packing, store the ICs in an environment with a temperature of 5～25℃ and a relative humidity of 60% or less and mount ICs within 4 days after opening dry packing.
(2) To re-store the ICs for an extended period of time within 4 days after opening the dry packing, use a dry box or re-seal the ICs in the dry packing with desiccant (whoes indicater is blue), and store in an environment with a temperature of 5～40℃ and a relative humidity of 80% or less, and mount ICs within 2 weeks.
(3) Total period of storage after first opening and re-opening is within 4 days, and store the ICs in the same environment as section 4-3.(1).



$X_1 + X_2$: within 4 days
Y : within 2 weeks

4－4. Baking (drying) before mounting
(1) Baking is necessary
(A) If the humidity indicator in the desiccant becomes pink
(B) If the procedure in section 4－3 could not be performed
(2) Recommended baking conditions
If the above conditions (A) and (B) are applicable, bake it before mounting. The recommended conditions are 16～24 hours at 120℃.
Heat resistance tray is used for shipping tray.
(3) Storage after baking
After baking ICs, store the ICs in the same environment as section 4-3.(1).

5. Surface Mount Conditions

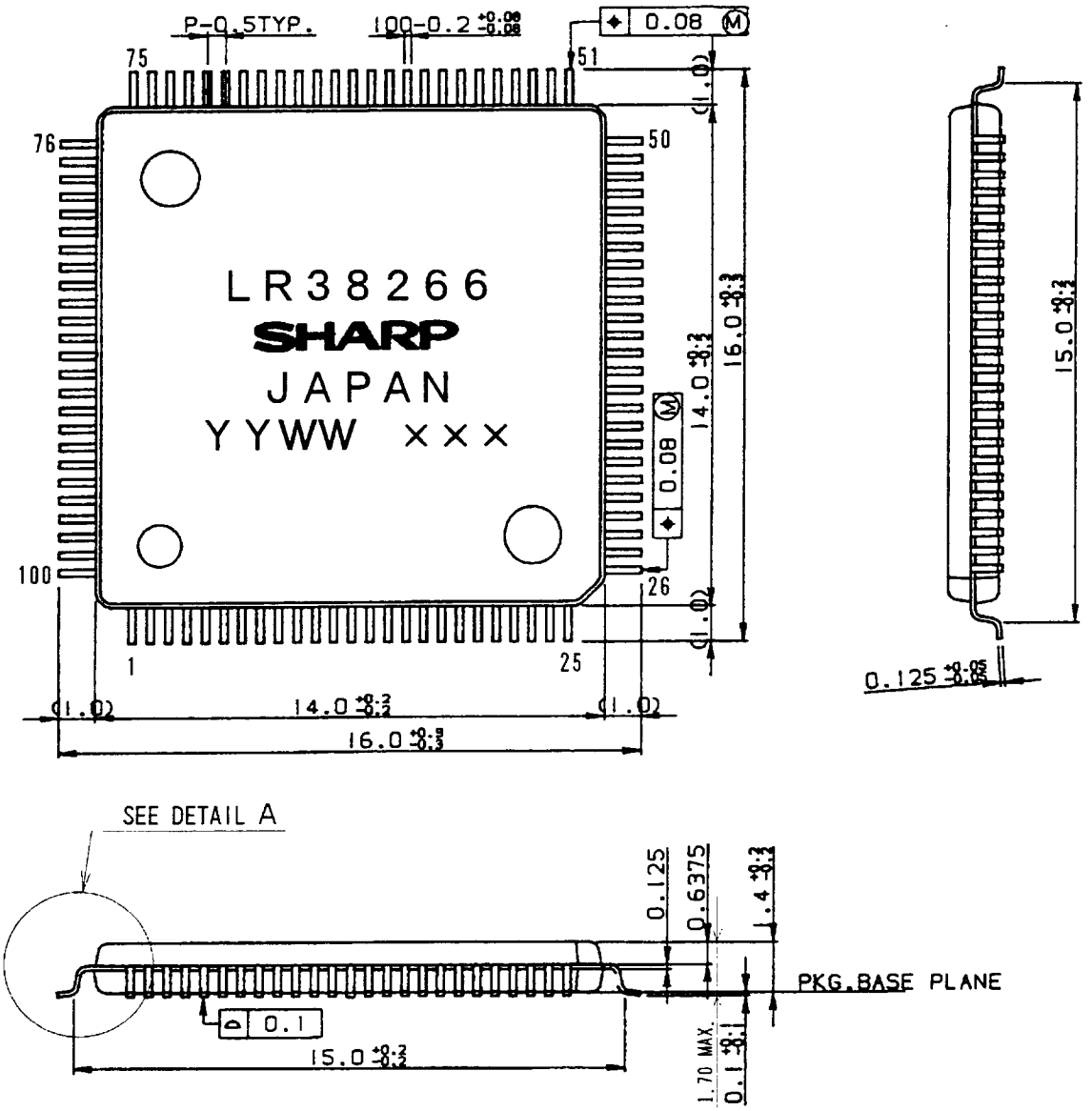
Please perform the following conditions when mounting ICs not to deteriorate IC quality.

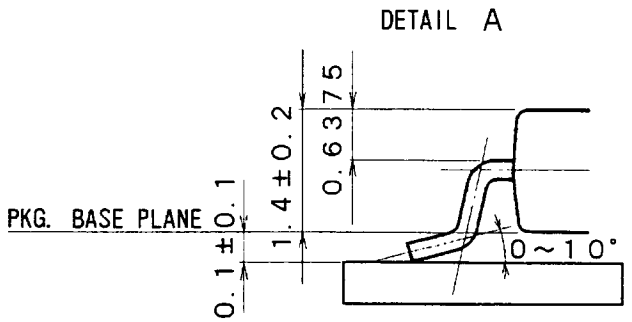
5－1.Soldering conditions(The following conditions are valid only for one time soldering.)

Mounting Method	Temperature and Duration	Measurement Point
Reflow soldering (air)	Peak temperature of 230℃ or less, duration of less than 15 seconds. 200℃ or over,duration of less than 40 seconds. Temperature increase rate of 1～4℃/second.	IC package surface
Vapor phase soldering	215℃ or less, duration of less than 40 seconds above 200℃	Steam
Manual soldering (soldering iron)	260℃ or less, duration of less than 10 seconds	IC outer lead surface

5－2. Conditions for removal of residual flux

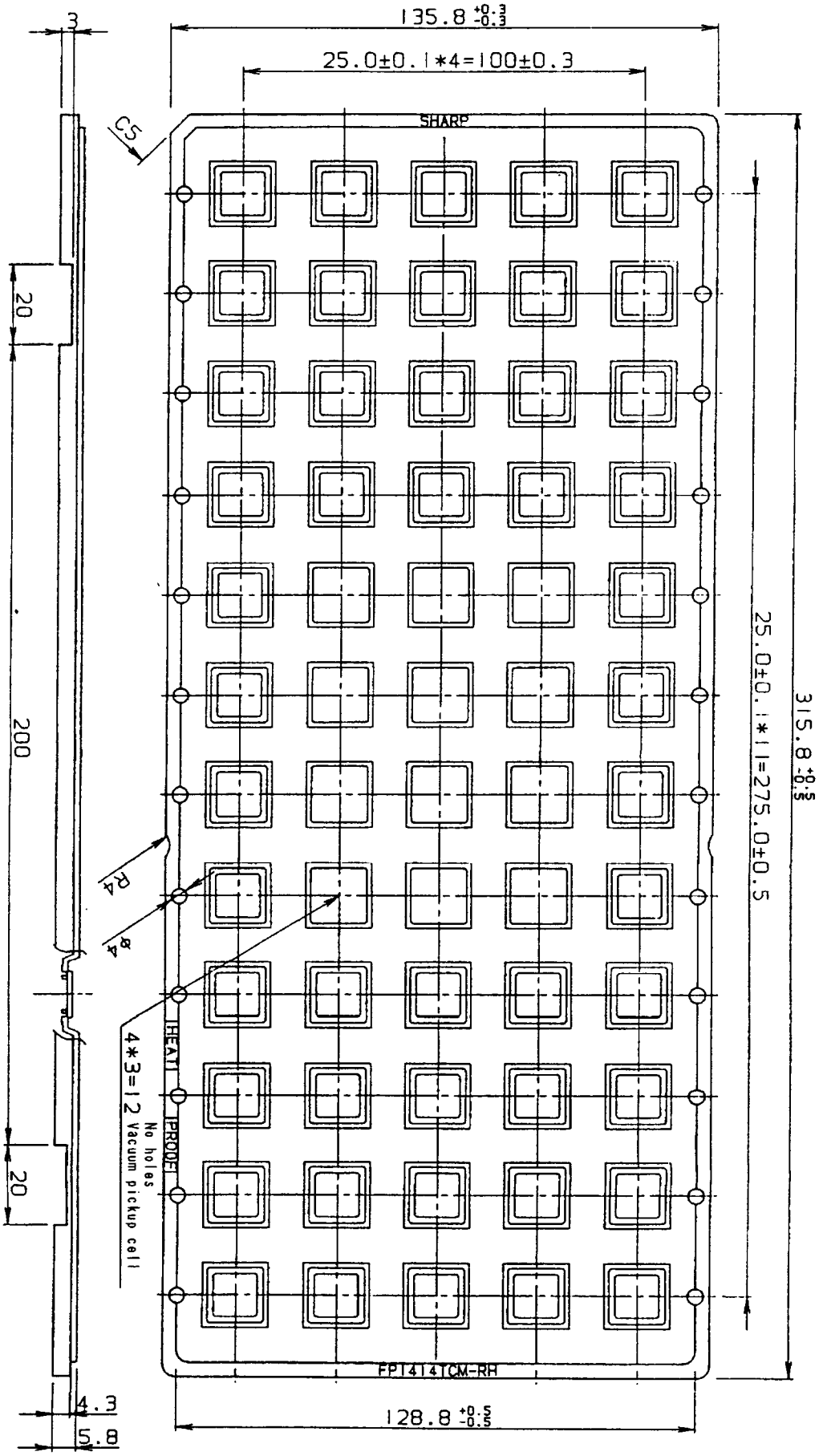
(1) Ultrasonic washing power : 25 Watts/liter or less
(2) Washing time : Total 1 minute maximum
(3) Solvent temperature : 15～40℃





名称 NAME	LQFP100-P-1414	リード仕上 LEAD FINISH	TIN-LEAD PLATING
DRAWING NO.	AA1058	単位 UNIT	mm

備考 NOTE プラスチックパッケージ外形寸法は、バリを含まないものとする。
Plastic body dimensions do not include burr of resin.



名称 NAME	FP1414TCM−RH	備考 NOTE
DRAWING NO.	CV557	
単位 UNIT	mm	