No. 2326

LM88PG99A

N Channel E/D MOS LSI EPROM-mountable 8-bit microcomputer for evaluating the LM8800 series microcomputers

1. Overview

The LM88PG99A is an EPROM-mountable single-chip 8-bit microcomputer, and can be used to develop and evaluate programs for the LM8800 series microcomputers.

Evaluation using an application program for a target microcomputer

The LM88PG99A will be able to have the same functions as those of the LM8800 series microcomputers by mounting EPROM 2732 or 2764, which enables the evaluation of a user application product before the user program is masked in the ROM by the mask options.

Program development

The LM88PG99A can be used to execute, stop and correct programs by combining it with the program debugging unit (EVA-410C) and the target board (TB88PG).

2. Characteristics

(1) Evaluation capabilities for input/output option functions
Input/output option functions can be selected by using data in the program ROM (On the LM8854, LM8804 and LM8802, input/output options can be selected by mask options).

(2) The mountable EPROMs are 2732, 2732A and 2764.

(3) Shrink type 64-pin configuration compatible with the LM8854 pin configuration.

(4) Memory capacity selectable
The memory capacity can be selected by setting external pins for evaluating the LM8854, LM8804 or LM8802 microcomputer. The program of 4K bytes or more can be evaluated.

(5) Program developing and evaluating functions
The LM88PG99A microcomputer allows programs to be executed and stopped if used together with the program debugging unit EVA-410C.
This microcomputer has the 28-pin socket on the package surface, which is used to mount the program EPROM. It also has the 14-pin socket used for controlling program execution. And the LM88PG99A microcomputer has the shrink type 64-pin configuration at the bottom, which is compatible with the LM8854 microcomputer. When evaluating the LM8804 and LM8802 microcomputers, use the pin conversion board (SK8804S) with the LM88PG99A microcomputer. With this board, the LM88PG99A microcomputer could have the shrink type 42-pin configuration which is compatible with the LM8804 and LM8802 microcomputers.

Notes on use

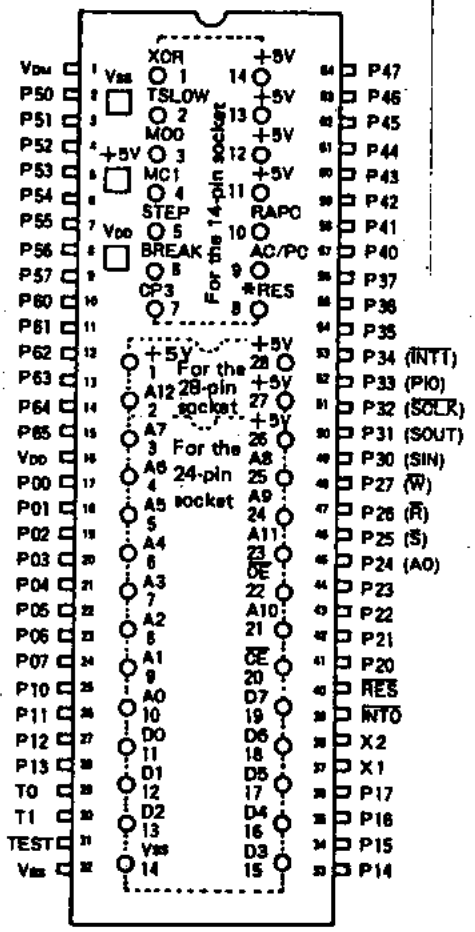
The following points should be taken into consideration when you use the LM88PG99A microcomputer. This microcomputer is designed for special use. In other words, the LM88PG99A is designed exclusively to develop and evaluate programs for the LM8800 series microcomputers.

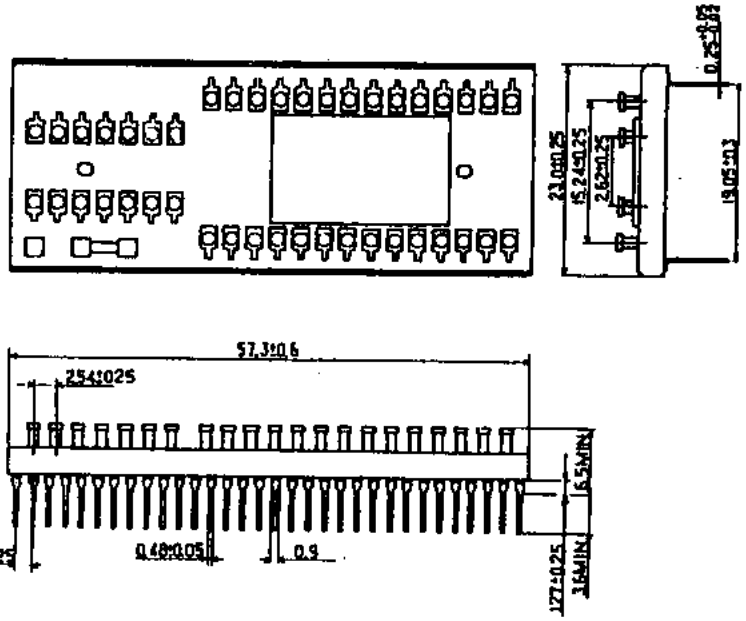
(1) The LM88PG99A microcomputer has different operating conditions from those of any production chip including a masked ROM. Especially, this microcomputer is adversely affected by high temperature and excessive humidity.

(2) The electric characteristics do not include the representative values and limit values of any production masked-ROM chip. For strict evaluation of an application where a production masked-ROM chip is used, use recommended constants for the electric characteristics of a production masked-ROM chip.

(3) Since the LM88PG99A microcomputer has different internal system configuration pattern from that of a production masked-ROM chip, keep the following in mind: (a) Initial values of RAM at the moment the power is first supplied (b) Static noise figures.

TOKYO SANYO ELECTRIC CO. LTD. SEMICONDUCTOR DIVISION


XOR
TSLOW
MOD
MC1
STEP
BREAK
CP3
RAPC
AC/PC
*RES
+5V
For the 14-pin socket
For the 28-pin socket
For the 24-pin socket
P47
P46
P45
P44
P43
P42
P41
P40
P37
P36
P35
P34 (INTT)
P33 (PIO)
P32 (SCLK)
P31 (SOUT)
P30 (SIN)
P27 (W)
P26 (R)
P25 (S)
P24 (A0)
P23
P22
P21
P20
RES
INTO
X2
X1
P17
P16
P15
P14
P50
P51
P52
P53
P54
P55
P56
P57
P60
P61
P62
P63
P64
P65
P00
P01
P02
P03
P04
P05
P06
P07
P10
P11
P12
P13
T0
T1
TEST


57.3±0.6
2.54±0.25
1.78±0.25
0.48±0.05
0.9
3.4MIN.
6.5MIN.

3. Pin description

Pin name	Number of pins	I/O	Functions	Remarks
V_{SS}	1	–		
V_{DD}	1	–	Power source for other than the RAM.	During the normal operation, the power must be supplied to the V_{DM} pin. And when the signal level at the $\overline{RES}$ terminal changes from "L" to "H", the V_{DD} voltage must be equal or greater than that of the V_{DM} terminal.
V_{DM}	1	–	Power source for RAM	
X_1	1	I, I/O	For external oscillation circuit or external clock circuit.	(Note 2) Option
X_2	1	O	For the ceramic resonator oscillation circuit. (Note 1)	
$\overline{RES}$	1	I	Reset input (with Pull-up Tr)	
TEST	1	I	For testing the LSI inside (connected to V_{SS} during the normal operation)	
T0	1	I	For the test 0 signal input or zero cross detection signal input. Also for the external interrupt 1 signal input.	Option
T1	1	I	For the test 1 signal input or counter signal input of timer 0	
$\overline{INT0}$	1	I	For the external interrupt 0 signal input or test faig input	
P00 to P07	8	I/O (N,PP)	Used as port 0 or as bi-directional data buses. Goes to high impedance at the reset.	
P10 to P17	8	I/O (H, ODA)	Used as port 1. Goes to high impedance at the reset. Large current port.	
P20 to P27	8	I/O (H, N, OD, PU)	Used as port 2. Or P24 used as A0, P25 as $\overline{S}$, P26 as $\overline{R}$ and P27 as $\overline{W}$. The output signal level at the reset can be selected as the "H" or "L" by using the mask options.	Option
P30 to P37	8	I/O (H, N, OD, PU)	Used as port 3. Or P30 used as SIN (1), P31 as SOUT (0), P32 as $\overline{SCLK}$ (I/O), P33 as PI0 (I/O) and P34 as $\overline{INT1}$. The output signal level at the reset can be selected as the "H" or "L" by using the mask options.	Option
P40 to P47	8	I(H)	Used as port 4	
P50 to P57	8	O (OD, PU)	Used as port 5 The output signal level at the reset can be selected as the "H" or "L" by using the mask options.	Option
P60 to P65	6 (Total 64)	O (OD)	Used as port 6. The output signal level at the reset can be selected as the "H" or "L" by using the mask options.	Option
XCR	1	I(N)	Used to select an oscillation circuit. (Note 2) The ceramic resonator oscillation circuit is selected when this input circuit is left open-circuited.	Pull-down
TSLOW	1	I(N)	Used to select a divider circuit for a selected oscillation circuit. When this circuit is left open-circuited, the 1/1 divider circuit is selected. When the "H" level signal is input to this circuit, the 1/2 divider circuit is selected.	Pull-down
MC0 to MC1	2	I(N)	Used to select the capacities of the RAM and ROM.	Pull-down
STEP BREAK	2	I(N)	Used to specify the step and break functions for the program currently being executed.	Pull-down
CP3	1	O(PU)	For the internal system clock pulse output.	Pull-up
AC/PC RAPC	2	I(N)	Used to select the A0 to A12 output data. Normally left open during program execution.	Pull-down
D0 to D7	8	I(N)	Used to input instructions.	
A0 to A12	13	O(PU)	For PC output, or ACC or RAM address output.	Pull-up

(Note 1) Contact our sales personnel for more information on the crystal oscillation.

(Note 2) At present time, only the ceramic resonator oscillation is available.

(Note 3) The above options can be selected by inputting the 2-byte data information to the area between the (last address minus 1) address and the last address in the ROM.

4. How to specify options

As explained below, the input/output circuit formats for the LM8800 series microcomputers can be selected by using the mask option.

When you evaluate programs for the LM8800 series microcomputers using the LM88PG99A, you can select the same input/output format and function as those of a production chip by mounting an EPROM whose option select area contains option codes and setting external switches, respectively. The use of the external switches enables the selections of the OSC, divider ratio and memory capacity.

ROM area	Bit	Input data and selectable input/output circuit formats
(Last address minus 1)	7	Used for specifying the output format for P54 through P57. 1 for selecting PU (Pull-up). 0 for OD (Open drain).
	6	Used for specifying the output format for P50 through P53. 1 for selecting PU (Pull-up). 0 for OD (Open drain).
	5	Used for sepcifying the output format for P34 through P37. 1 for selecting PU (Pull-up). 0 for OD (Open drain).
	4	Used for specifying the output format for P30 through P33. 1 for selecting PU (Pull-up). 0 for OD (Open drain).
	3	Used for specifying the output format for P24 through P27. 1 for selecting PU (Pull-up). 0 for OD (Open drain).
	2	Used for specifying the output format for P20 through P23. 1 for selecting PU (Pull-up). 0 for OD (Open drain).
	1	Used for specifying the output signal level of P30 through P37 and P60 through P65 at the reset. 1 for selecting the H level signal. 0 for the L level signal.
	0	Used for specifying the output signal level of P20 through P27 and P50 through P57 at the reset. 1 for selecting the H level signal. 0 for the L level signal.
(Last address)	7	Not available yet. *Note 1
	6	Used for specifying a divider ratio (TSLOW) of the OSC. *Note 2. 1 for specifying the 1/2 SLOW. 0 for the 1/1 FAST.
	5	Used for specifying an OSC type. *Note 2. 1=*Reserved. 0 for specifying the CF oscillation.
	4	Used for specifying the zero cross detection circuit for the T0 input. 1 for specifying the internal circuit. 0 for nonuse of the internal circuit.
	3	Used for specifying the input format of P34 through P37. 1=H (High threshold input). 0=N (Normal input).
	2	Used for specifying the input format of P30 through P33. 1=H. 0=N.
	1	Used for specifying the input format of P24 through P27. 1=H. 0=N.
	0	Used for specifying the input format of P20 through P23. 1=H. 0=N.

The option specification area varies depending on each ROM size. For the LM8854, it is between address 0FFEH and 0FFFH.

When evaluating programs for the LM8800 series microcomputers using either the LM8899A or LM88PG99A, you can select the following option specification areas by setting the external switches for selecting the memory capacities: (1FFEH, 1FFFH) for the 8K-byte ROM. (0FFEH, 0FFFH) for the 4K-byte ROM. (7FEH, 7FFH) for the 2K-byte ROM.

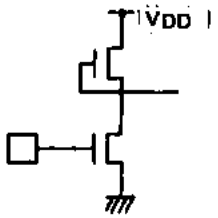
*Reserved: For Type Nos. under development or future Type Nos.

*Note 1: Specify 0. The data of 0 is automatically set when the Sanyo assembler is used.

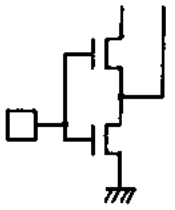
*Note 2: Use external switches when evaluating programs using the LM8899A or LM88PG99A. CF oscillation means the ceramic resonator oscillation.

[Input/output circuit format]

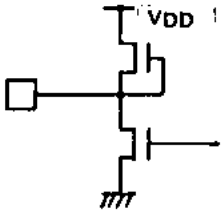
- Normal Input (N)



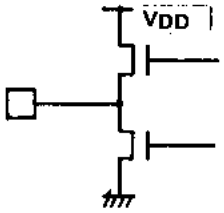
- High threshold (H)



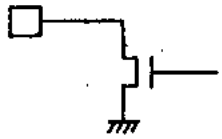
- Pull-up output (PU)



- Push-pull output (PP)



- Open drain output (OD, ODA)



5. Notes on use

(1) The LM88PG99A has the 28-pin socket for mounting either the 2732, 2732A or 2764 EPROM. Pins 1, 2, 27 and 28 should be open when the 2732 or 2732A EPROM is mounted on.

(2) How to select the OSC, divider ratio and memory capacities.
The OSC, divider ratio and memory capacity can be selected by setting pins 1 through 4 on the 14-pin socket on the package surface as follows.
To select other options, input option data to the option specification area.

Function type	Pin no.	Pin name	Pin setting		Function mode		Option data		
OSC	1	XCR	OFF		CF oscillation		Bit 5 of the last address	0	
			ON		RESERVED			–	
Clock prescaler divider ratio	2	TSLOW	OFF		1/1		Bit 6 of the last address	0	
			ON		1/2			1	
Memory capacity selection	3 4	MC0 MC1	Pin setting		Memory capacity		Option data area		
			MC0	MC1	ROM	RAM			
			OFF	OFF	4KB	256B	FFE, FFF_H		(LM8864/04)
			ON	OFF	8KB	256B	1FFE, $1FFF_H$		
			OFF	ON	2KB	128B	7FE, $7FF_H$		(LM8802)
			ON	ON	Reserved				

ON: +5V voltage supply. OFF: Open-circuited. Reserved: For the Type Nos. under development or future Type Nos.

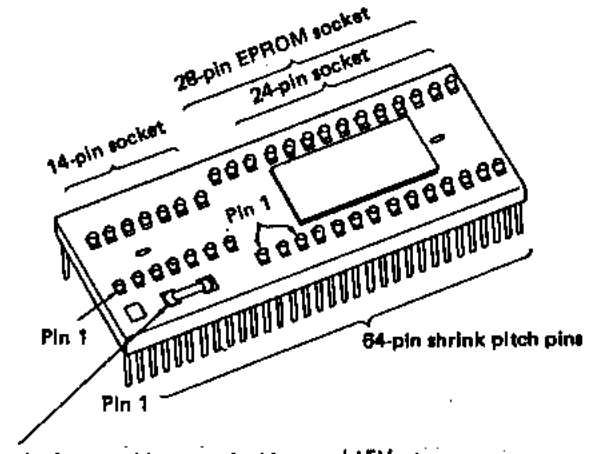
*The 8K-byte ROM is selected only to debug programs (Use assembler LM8899 COM. In this case, the option specification area is between address 1FFEH and address 1FFFH).

Pins 14, 13, 12 and 11 of the 14-pin socket are connected with +5V pin. These pins can be used only to supply +5V voltage to pins 1, 2, 3 and 5 respectively. Note that these pins cannot be used for any other purpose.

Pins 5, 6, 7, 8, 9 and 10 of the 14-pin socket are used for program debugging when the TB88PG of the program debugging unit (EVA-410C) is used together with the LM88PG99A microcomputer. Otherwise, all these pins should be left open.

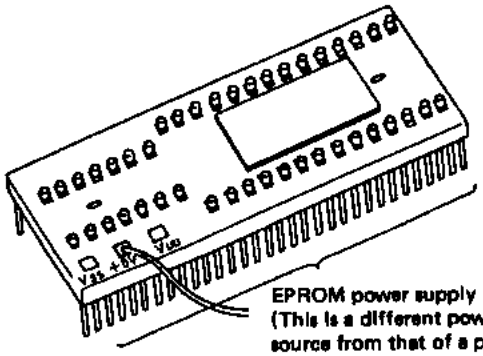
(3) EPROM power supply source

- Each EPROM normally consumes current of 50 to 100mA. When sufficient power cannot be supplied to an EPROM from an application product, an independent external power supply source can be used to operate the EPROM.
- At the shipment of the LM88PG99A, the +5V pin and the V_{DD} pin are connected. This means, the power is supplied to an EPROM from the pin 16 (V_{DD}) which is used for supplying the power to the LM8899.



At the factory shipment, the V_{DD} and +5V power supply pads are connected.

- Of the power supply pads on the package surface, the +5V pad is used to supply power to an EPROM.



EPROM power supply pad
(This is a different power supply source from that of a production chip.)

(4) Evaluation of programs for the LM8804/02 microcomputer

The LM8804/02 microcomputer has 42 pins. Therefore, the pin conversion board (SK8804S) needs to be used when the programs for the LM8804/02 microcomputer are evaluated by the LM88PG99A microcomputer.

6. Specifications

(1) Absolute maximum ratings (V_{SS}=0V, T_a=25°C)

Item	Symbol	Conditions		Unit
Maximum supply voltage	V_{DD} V_{DM}		−0.3 to +8	V
Input/output voltage Note 1	V_{IO1}	$\overline{INTO}$, T1, P4, P1 and input/output ports with open drain format	−0.3 to +15	V
	V_{IO2}	Input/output pins other than the above	−0.3 to V_{DD}+0.3	V
Average output current Note 2	I_{OHA}	Per pull-up or push-pull pin	−2.0	mA
	I_{OLA1}	Per output pin other than P1	18	mA
	I_{OLA2}	Per output pin of P1	30	mA
	I_{OLA3}	Total output of P0, P5 and P6	120	mA
	I_{OLA4}	Total output of P2 and P3	80	mA
	I_{OLA5}	Total output of upper four pins or lower four pins of P1	75	mA
Peak output current Note 3	I_{OHP}	Per pull-up or push-pull pin	−2.0	mA
	I_{OLP1}	Per output pin other than P1	18	mA
	I_{OLP2}	Per output pin of P1	30	mA
	I_{OLP3}	Total output of P0, P5 and P6	120	mA
	I_{OLP4}	Total output of P2 and P3	80	mA
	I_{OLP5}	Total output of upper four pins or lower four pins of P1	75	mA
Recommended power dissipation	P_{dmax}	Ta=10 to 40°C, DIC-64S	1000	mW
Operating temperature range	Topg		+10 to +40	°C
Storage temperature range	T_{stg}		−55 to +150	°C

Note 1: Output=OFF or "H". The output signal level width can be allowed at the X1 pin.
Note 2: Limit values: Average output current measured at any interval of 100ms should be less than those values.
Note 3: Ceiling limit values should not be exceeded at any moment.

(2) Recommended operating conditions (V_{DD}=V_{DM}=4.5 to 5.5V, V_{SS}=0V, T_a=10 to 40°C)

Item		Symbol	Conditions	min	typ	max	unit
Supply voltage		V_{DD}		4.5		5.5	V
RAM power supply voltage		V_{DM}	At the normal operation. See figure 6 for the interrelations of power supply waveforms and $\overline{RES}$.	4.5		5.5	V
		(V_{DM})	$\overline{RES}$="L" at the standby mode	3.5		5.5	V
Normal input ports	"H" level input voltage	V_{IH1}	P0, and normal input options for P2 and P3	2.2		5.5	V
	"L" level input voltage	V_{IL1}		V_{SS}		0.6	V
High threshold input ports	"H" level input voltage	V_{IH2}	P1 and P4, and high-threshold input options for P2 and P3. Note that only the normal input option can be selected for A_0, $\overline{S}$, $\overline{R}$, and $\overline{W}$.	0.6V_{DD}			V
	"L" level input voltage	V_{IL2}		V_{SS}		0.3V_{DD}	V
$\overline{INT0}$, T1	"H" level input voltage	V_{IH3}		0.6V_{DD}			V
	"L" level input voltage	V_{IL3}		V_{SS}		0.3V_{DD}	V
$\overline{RES}$	"H" level input voltage	V_{IH4}		0.6V_{DD}		V_{DD}	V
	"L" level input voltage	V_{IL4}		V_{SS}		0.9	V
	"L" level input voltage	V_{IL5}	V_{DM}=3.5V	V_{SS}		0.9	V
X1	"H" level input voltage	V_{IH6}	External drive option (Ceramic resonator oscillation)	0.4V_{DD} +1.0		V_{DD}	V
	"L" level input voltage	V_{IL6}		V_{SS}		0.9	V
	Clock pulse width	$t_{C\Phi}$	See Figure 1	0.14		0.5	µs
	Instruction cycle time	t_{CI}	$t_{C\Phi}$ x 8 x divider ratio (1 or 2)	1.12		4	µs
	"H" level clock pulse width	$t_{W\Phi H}$	External drive option (Ceramic resonator oscillation)	0.06			µs
	"L" level clock pulse width	$t_{W\Phi L}$	External drive option (Ceramic resonator oscillation)	0.06			µs
TEST	"L" level input voltage	V_{IL7}		V_{SS}		0.6	V
X1	Ceramic resonator oscillation External capacity	C1	Ceramic resonator oscillation options (4MHz, 6MHz and 7MHz) See figure 2. Note 4.	30	33	36	pF
X2		C2		42	47	52	pF
T0	"H" level input voltage	V_{IH8}	Normal input option	2.2		V_{DD}	V
	"L" level input voltage	V_{IL8}	Normal input option	V_{SS}		0.6	V
	Zero-cross input level	V_{ZIN}	Capacitor-coupled, peak to peak	1.0		2.2	V
	Zero-cross input frequency	f_{ZIN}	Zero-cross option	50		1000	Hz
$\overline{SCLK}$ (P32)	Input pulse cycle time	t_{SC}	See figure 3. External clock	1.0			µs
	Pulse width of "H" level input	t_{WSCH}		0.4			µs
	Pulse width of "L" level input	t_{WSCL}		0.4			µs
	Rise or fall time of input	t_{rf}	See figure 4. External clock			1.0	µs
$\overline{SCLK}$ (P32)	Data input set-up time	t_{ST}	See figure 3	0.3			µs
SIN (P30)	Data input hold time	t_{HD}	See figure 3	0.03			µs
A0 (P24)	Pre-$\overline{R/W}$ input set-up time	t_{SUP}	See figure 5. 8-bit bus interface	0.26			µs
$\overline{S}$ (P25)	Post-$\overline{R/W}$ input hold time	t_{HLD}	"	0			µs
$\overline{R}$ (P26)	Data input set-up time	t_{DSUP}	"	0.15			µs
$\overline{W}$ (P27)	Data input hold time	t_{DHLD}	"	0.03			µs
P00 to P07	$\overline{R/W}$ pulse width	t_{WRW}	"	0.225			µs

Note 4: Includes the stray capacitance of Board, Wiring, etc.

(3) Electric characteristics (V_{DD}=V_{DM}=4.5 to 5.5V, T_a=10 to 40°C)

Item		Symbol	Conditions	min	typ	max	unit
P4, T0, T1	"H" level input current	I_{IH1}	V_{IN}=13.5V (In this case, the normal input option must be selected for T0.)			5	μA
$\overline{INT0}$	"L" level input current	I_{IL1}	V_{IN}=V_{SS}. (In this case, the normal input option must be selected for T0.)	−5			μA
P0 port	"H" level input current	I_{IH2}	V_{IN}=V_{DD}, (with output OFF)			5	μA
	"L" level input current	I_{IL2}	V_{IN}=V_{SS}, (with output OFF)	−5			μA
Pull-up Input/output ports	"L" level input current	I_{IL3}	V_{DD}=5V±10% and V_{IN}=0.4V when the pull-up option is selected for P2 and P3, and the output level is "H".	−1.6			mA
Open drain Input/output ports	"H" level input current	I_{IH4}	V_{IN}=13.5V when the open drain option is selected for P1, and P2 and P3, and with output OFF.			5	μA
	"L" level input current	I_{IL4}	V_{IN}=V_{SS}, when the open drain option is selected for P1, and P2 and P3, and with output OFF.	−5			μA
X1	"H" level input current	I_{IH5}	V_{IN}=V_{DD}, when the ceramic resonator oscillation option is selected.	2		13	μA
	"L" level input current	I_{IL5}	V_{IN}=V_{SS}, when the ceramic resonator oscillation option is selected.	−13		−2	μA
$\overline{RES}$	"H" level input current	I_{IH6}	V_{IN}=V_{DD}			5	μA
	"L" level input current	I_{IL6}	V_{IN}=V_{SS}	−35		−6	μA
T0	"H" level input current	I_{IH7}	V_{IN}=V_{DD}, when the zero-cross detection option is selected.			195	μA
	"L" level input current	I_{IL7}	V_{IN}=V_{SS} when the zero-cross detection option is selected.	−70			μA
	Zero-cross detection Accuracy	V_{ZA}	60Hz sine wave input when the zero-cross detection option is selected.			±100	mV
P0 port	"H" level output voltage	V_{OH1}	V_{DD}=5V±10%, I_{OH}=−0.4mA	2.4			V
	"L" level output voltage	V_{OL1}	I_{OL}=14mA			1.5	V
Pull-up output ports	"H" level output voltage	V_{OH2}	I_{OH}=−50uA when the pull-up option is selected for P2, P3 and P5.	0.8V_{DD}			V
		V_{OH3}	I_{OH}=−100uA when the pull-up option is selected for P2, P3 and P5.	0.48V_{DD}			V
	"L" level output voltage	V_{OL2}	I_{OL}=14mA when the pull-up option is selected for P2, P3 and P5.			1.5	V
Open drain output ports	Leakage current with output OFF	I_{OFF1}	V_{OH}=13.5V when the open drain option is selected for P6, and P2, P3 and P5.			5	μA
		I_{OFF2}	V_{OH}=V_{DD} when the open drain option is selected for P6, and P2, P3 and P5.			1	μA
	"L" level output voltage	V_{OL3}	I_{OL}=15mA when the open drain option is selected for P6, and P2, P3 and P5.			1.5	V
P1 port	Leakage current with output OFF	I_{OFF3}	V_{OH}=13.5V			5	μA
		I_{OFF4}	V_{OH}=V_{DD}			1	μA
	"L" level output voltage	V_{OL4}	I_{OL}=25mA			2	V

Continued on next page.

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Item		Symbol	Conditions	min	typ	max	unit
TEST	"L" level input current	I_{IL8}	$V_{IN}=V_{SS}$	−10		—	μA
Serial output	Output delay time	t_{dSD}	See Figure 3. CL=50pF; pull-up resistor=2Kohm: CL: $\overline{SCLK}$/SOUT load capacitance.			0.36	μS
$\overline{R}$ (P26) P00 to 07	Output enable period	t_{dEN}	See figure 5. CL=150pF, CL: P00 to P07 load capacitance			0.22	μS
	Output disenable period	t_{dDE}	See figure 5			0.17	μS
V_{DM}	RAM standby current	I_{DMS}	V_{DM}=4.5V, $\overline{RES}$=L			30	mA
	RAM power supply current	I_{DM}	V_{DM}=5V±10%			30	mA
V_{DM} V_{DD}	Total power supply current	I_{DD} +I_{DM}	OSC oscillation mode, Open with output "H", Ta=10 to 40°C.		105	135	mA
Input	Pin capacitance	C_I	When 1MHz is selected as f.		10		pF

Fig. 1 X1 input waveform

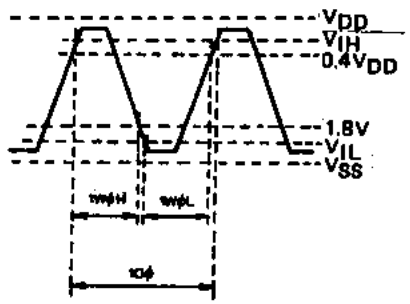
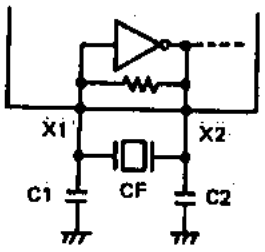


Fig. 2 Ceramic resonator oscillation circuit



CF: CSA 4.00MG (Murata)
KBR 4.0MS (Kyocera)
CSA 6.00MT (Murata)
KBR 6.0M (Kyocera)
CSA 7.00MT (Murata)

Fig. 3 Serial input/output timings

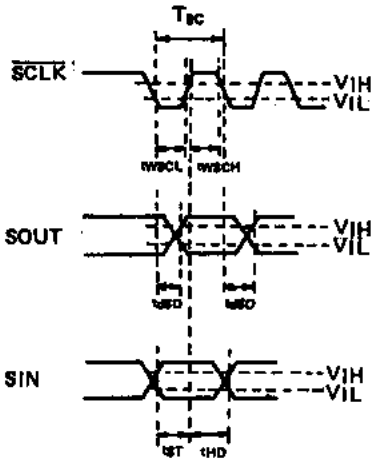


Fig. 4 $\overline{SCLK}$ rise/fall time

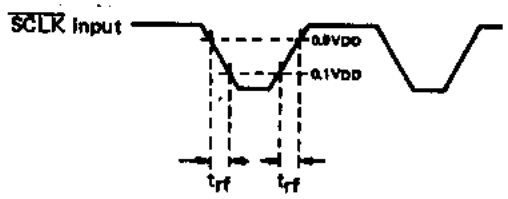


Fig. 5. 8-bit bus interface timings

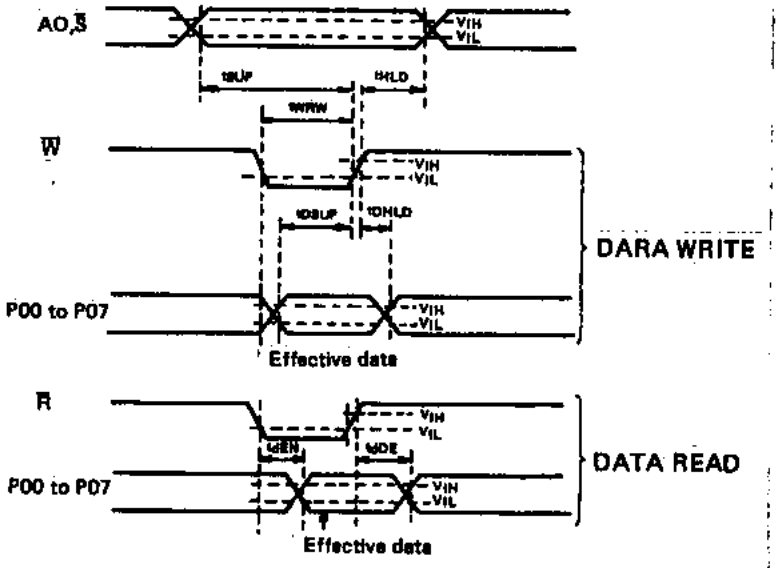
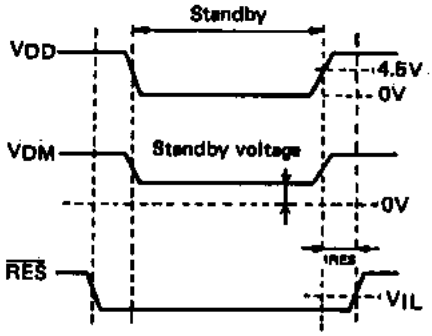


Fig. 6. Reset waveforms and power supply waveforms at the standby mode



(Note) When the $\overline{RES}$ signal level changes from "L" to "H", the condition (of $5.5 \geq V_{DD} \geq V_{DM} \geq 4.5$) must be satisfied. And the condition of reset release time (Tres) ≥ oscillation stabilizing period + 2 instruction cycles) must be also met.