Ordering number : ENN*6709

CMOS IC

LC868900/10/50/60

Column Driver IC for Dot Matrix Graphic LCD

Preliminary

Overview

The LC868900 is a column (segment) driver with the display RAM for the liquid crystal dot matrix-graphic display. It stores display data sent from the 8-bit microcontroller in the internal display RAM and generates dot matrix LCD signals.
The LC868900 can control the graphic mode, in which each bit of data from the internal RAM either lights or does not light a dot in the LCD.
As the LC868900 is fabricated using CMOS process technology, combining it with a CMOS microcontroller produces an LCD devices of low power demand.

Feature

(1) Classification

- Interfacing allowed with 80-family
  - LC868900 640×8-bit RAM
  - LC868910 1280×8-bit RAM
- Interfacing allowed with motorola-family
  - LC868950 640×8-bit RAM
  - LC868960 1280×8-bit RAM

(2) Segment outputs

- 80 segment outputs
- Segment display direction programmable

(3) Automatic LCD display controller

- Display duty : 1 / 1 - 1 / 65 duty
- Instruction functions
  - ON / OFF of display
  - Control of the horizontal display bits : (6 - 8 bits)×(horizontal display bytes)
  - Vertical display scroll function : Set of start address register
  - Selectable display data output : 'Logical-OR output' or 'Exclusive-OR output'
  - Read / Write display data
  - Read of busy flag

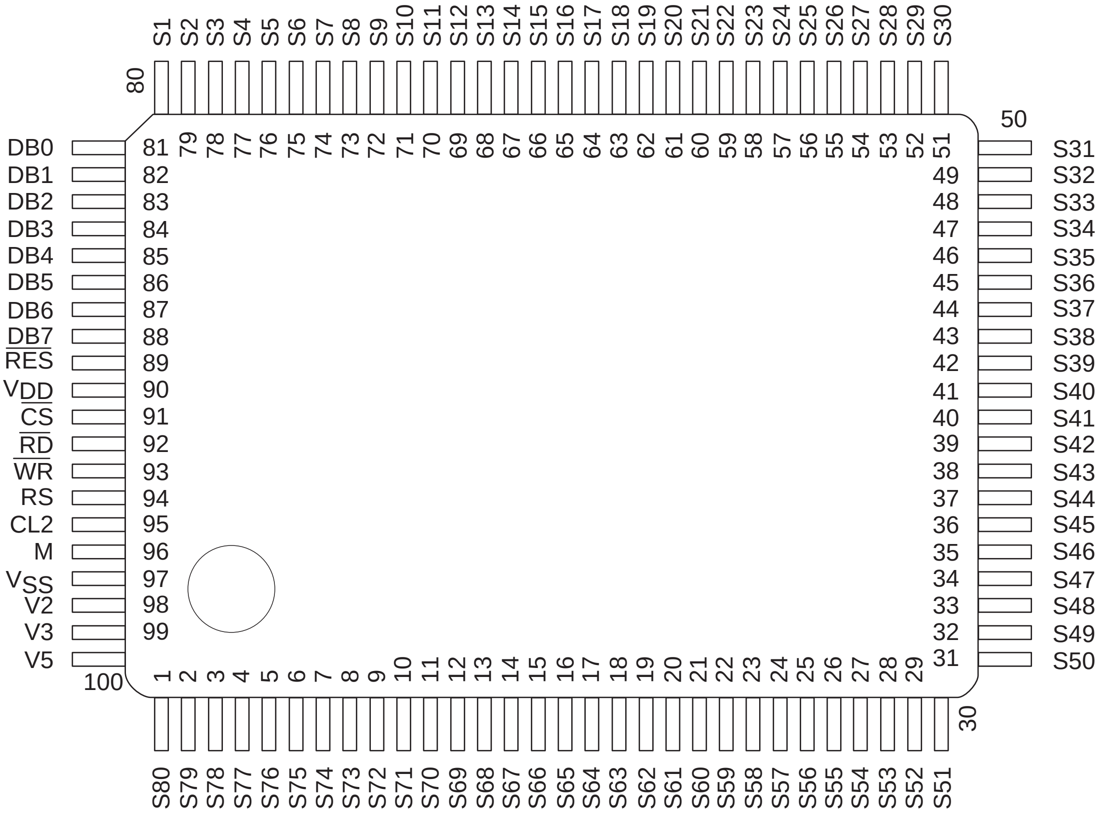
SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

(4) Power supply
- Logic circuit 3 to 5V (V_{DD})
- LCD drive circuit V_{DD} to V_{DD}-15V

(5) CMOS process

(6) Factory shipment
- Chip delivery form
- QFP100

Pin Assignment



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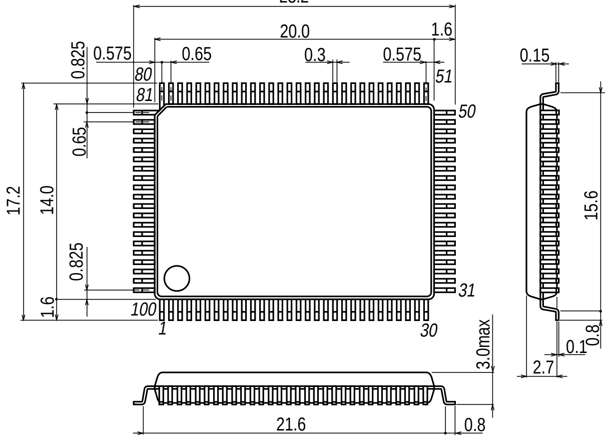
Package Dimensions

unit : mm

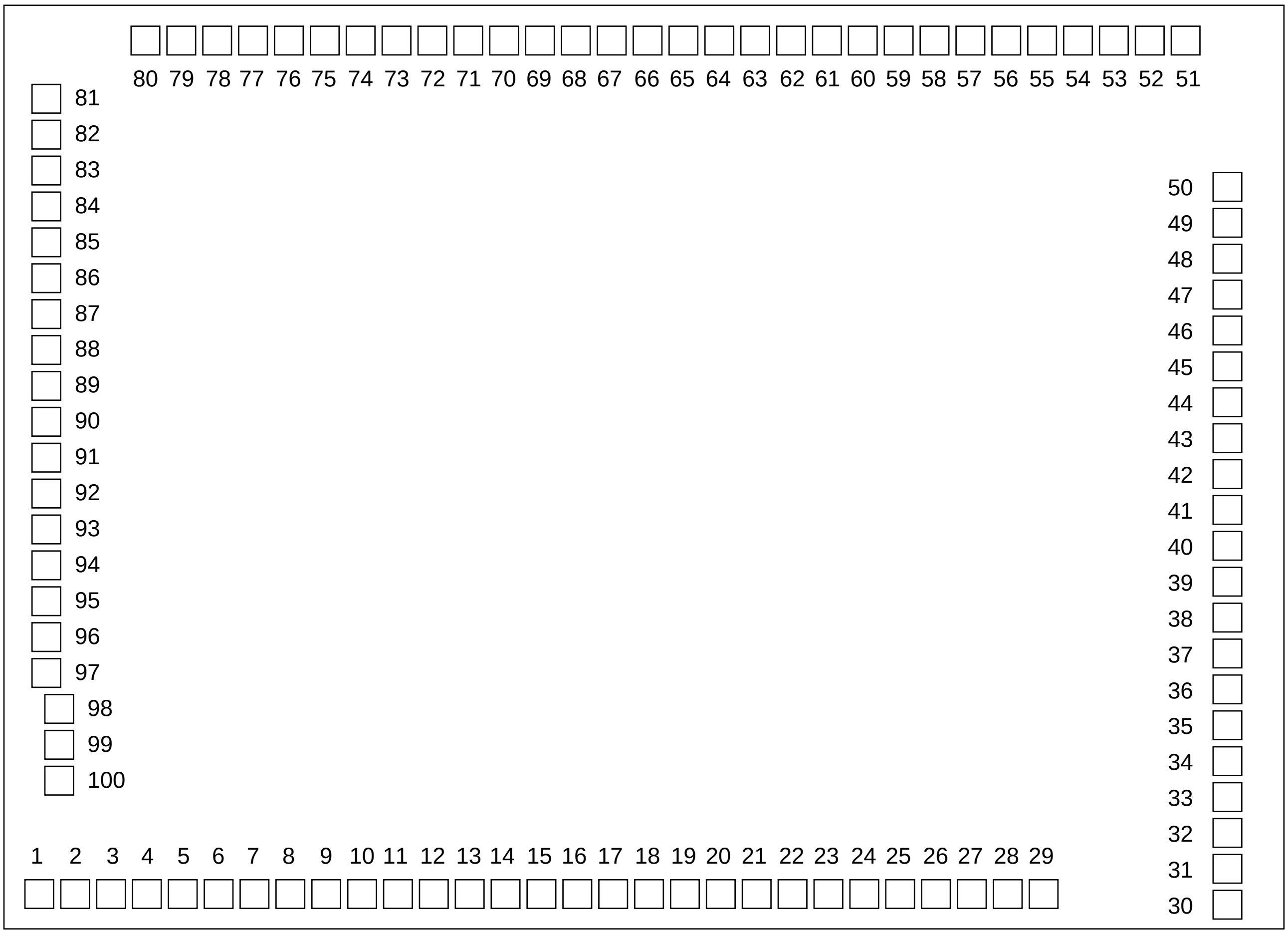
3151



SANYO : QIP-100E

Pad Layout

Chip size (X✕Y) : 5.71mm✕4.43mm
Thickness of chip : 480µs
Pad size : 120µm✕120µm



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Pad Name and cordinates table

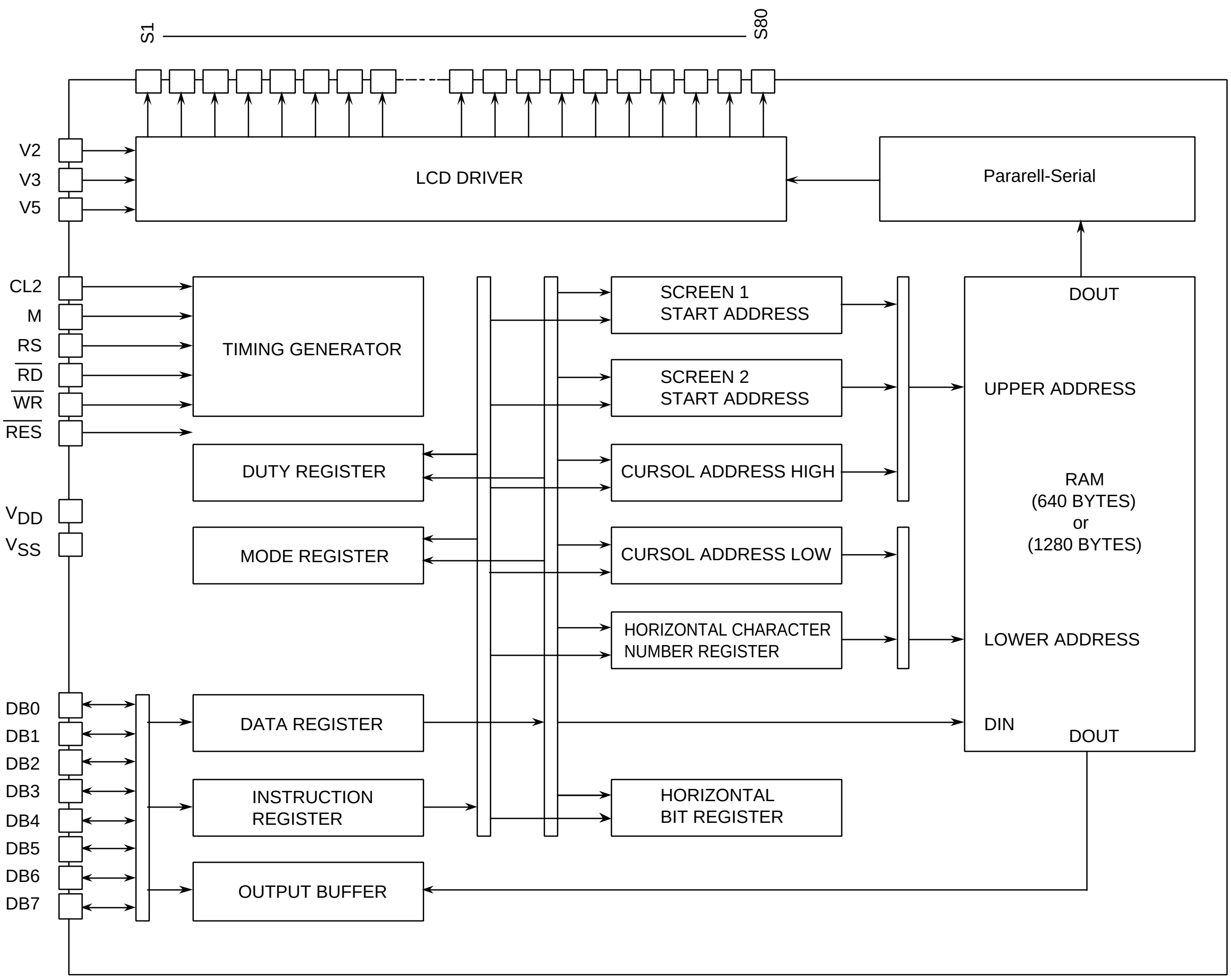
Pin No.	Pad No.	Name	Cordinates	
			Xμm	Yμm
1	1	S80	-2645	-1974
2	2	S79	-2483	-1974
3	3	S78	-2320	-1974
4	4	S77	-2158	-1974
5	5	S76	-1995	-1974
6	6	S75	-1833	-1974
7	7	S74	-1670	-1974
8	8	S73	-1508	-1974
9	9	S72	-1345	-1974
10	10	S71	-1183	-1974
11	11	S70	-1020	-1974
12	12	S69	-858	-1974
13	13	S68	-695	-1974
14	14	S67	-533	-1974
15	15	S66	-370	-1974
16	16	S65	-208	-1974
17	17	S64	-45	-1974
18	18	S63	117	-1974
19	19	S62	280	-1974
20	20	S61	442	-1974
21	21	S60	605	-1974
22	22	S59	767	-1974
23	23	S58	930	-1974
24	24	S57	1092	-1974
25	25	S56	1255	-1974
26	26	S55	1417	-1974
27	27	S54	1580	-1974
28	28	S53	1742	-1974
29	29	S52	1905	-1974
30	30	S51	2658	-1985
31	31	S50	2658	-1823
32	32	S49	2658	-1660
33	33	S48	2658	-1498
34	34	S47	2658	-1335
35	35	S46	2658	-1173
36	36	S45	2658	-1010
37	37	S44	2658	-848
38	38	S43	2658	-685
39	39	S42	2658	-523
40	40	S41	2658	-360
41	41	S40	2658	-198
42	42	S39	2658	-35
43	43	S38	2658	127
44	44	S37	2658	290
45	45	S36	2658	452
46	46	S35	2658	615
47	47	S34	2658	777
48	48	S33	2658	940
49	49	S32	2658	1102
50	50	S31	2658	1265

Pin No.	Pad No.	Name	Cordinates	
			Xμm	Yμm
51	51	S30	2572	2019
52	52	S29	2409	2019
53	53	S28	2247	2019
54	54	S27	2084	2019
55	55	S26	1922	2019
56	56	S25	1759	2019
57	57	S24	1597	2019
58	58	S23	1434	2019
59	59	S22	1272	2019
60	60	S21	1109	2019
61	61	S20	947	2019
62	62	S19	784	2019
63	63	S18	622	2019
64	64	S17	459	2019
65	65	S16	297	2019
66	66	S15	134	2019
67	67	S14	-28	2019
68	68	S13	-191	2019
69	69	S12	-353	2019
70	70	S11	-516	2019
71	71	S10	-678	2019
72	72	S9	-841	2019
73	73	S8	-1003	2019
74	74	S7	-1166	2019
75	75	S6	-1328	2019
76	76	S5	-1491	2019
77	77	S4	-1653	2019
78	78	S3	-1816	2019
79	79	S2	-1978	2019
80	80	S1	-2141	2019
81	81	DB0	-2540	1905
82	82	DB1	-2540	1734
83	83	DB2	-2540	1563
84	84	DB3	-2540	1392
85	85	DB4	-2540	1221
86	86	DB5	-2540	1051
87	87	DB6	-2540	880
88	88	DB7	-2540	709
89	89	$\overline{RES}$	-2540	538
90	90	V_{DD}	-2540	375
91	91	$\overline{CS}$	-2540	213
92	92	$\overline{RD}$	-2540	50
93	93	$\overline{WR}$	-2540	-112
94	94	RS	-2540	-275
95	95	CL2	-2540	437
96	96	M	2540	-600
97	97	V_{SS}	-2540	-762
98	98	V2	-2517	-943
99	99	V3	-2517	-1106
100	100	V5	-2571	-1268

Notes ;

- When the chip is used, connect the substrate of chip to V_{DD} (or open).
- If the package immerse in the solder tank when mounting the QFP on the substrate, inquire of our company about the conditions of it.

Block Diagram



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Pin Description

Pin	Pin No.	Input / Output	Function Description
V_{SS}	97	–	Should be connected with the negative supply voltage pin.
V_{DD}	90	-	Should be connected with the positive supply voltage pin.
DB0 to DB7	81 to 88	Input / Output	Built-in Data bus and pull-up resistor terminal for transmitting / receiving data to / from the MPU
$\overline{\text{RES}}$	89	Input	Reset, built-in pull-up resistor
$\overline{\text{CS}}$	91	Input	Chip select : Selection allowed when CS=0, built-in pull-up resistor
$\overline{\text{RD}}$	92	Input	Read signal : MPU ← LC868900 series, built-in pull-up resistor
$\overline{\text{WR}}$	93	Input	Write signal : MPU → LC868900 series, built-in pull-up resistor
RS	94	Input	Register select : RS=1 ; instruction register, RS=0 ; data register Built-in Pull-up resistor
CL2	95	Input	Signal for LCD display (clock signal), built-in pull-down resistor
M	96	Input	Signal for LCD display (synchronization), built-in pull-up resistor
V2 V3 V5	98 99 100	- - -	Voltage supply pins to LCD drivers
S1 to S80	80 to 1	Output	Segment driver pins for LCD display

1. Absolute Maximum Ratings at V_{SS}=0V and Ta=25°C

Parameter	Symbol	Pins	Conditions	V_{DD}[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Supply voltage	V_{DD} MAX	V_{DD}			−0.3		+7.0	V
Input voltage for LCD	VNMAX	V2, V3, V5			V_{DD}−12		V_{DD}+0.3	
Input voltage	V_I(1)	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RS CL2, M, $\overline{RES}$			−0.3		V_{DD}+0.3	
	VI(2)	DB0 to DB7 (Input mode)			−0.3		V_{DD}+0.3	
Output voltage	VO(1)	S1 to S80			V_{DD}−12		V_{DD}+0.3	
	VO(2)	DB0 to DB7 (Output mode)			−0.3		V_{DD}+0.3	
Power dissipation (max.)	Pdmax	QFP100E	Ta= −30 to + 70°C				200	mW
Operating temperature range	Topg				−30		70	°C
Storage temperature range	Tstg				−55		150	

*Satisfy the next condition : $V_{DD} \geq V2 \geq V3 \geq V5$

2. Recommended Operating Range at Ta= –30°C to +70°C, V_{SS}=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				V_{DD} [V]	min.	typ.	max.	
Operating supply voltage range	V_{DD}	V_{DD}	FCL2 ≤ 500kHz		2.5		6.0	V
HOLD voltage	V_{HD}	V_{DD}	RAMs and Registers hold voltage at standby mode.		2.0		6.0	
Input high voltage	$V_{IH}(1)$	DB0 to DB7	Input mode	4.5 to 6.0	2.2		V_{DD}	
				2.5 to 4.5	0.75V_{DD}		V_{DD}	
	$V_{IH}(2)$	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RS		4.5 to 6.0	2.2		V_{DD}	
				2.5 to 4.5	0.75V_{DD}		V_{DD}	
	$V_{IH}(3)$	CL2, M, $\overline{RES}$		4.5 to 6.0	0.75V_{DD}		V_{DD}	
				2.5 to 4.5	0.75V_{DD}		V_{DD}	
Input low voltage	$V_{IL}(1)$	DB0 to DB7	Input mode	4.5 to 6.0	0		0.8	
				2.5 to 4.5	0		0.25V_{DD}	
	$V_{IL}(2)$	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RS		4.5 to 6.0	0		0.8	
				2.5 to 4.5	0		0.25V_{DD}	
	$V_{IL}(3)$	CL2, M, $\overline{RES}$		4.5 to 6.0	0		0.25V_{DD}	
				2.5 to 4.5	0		0.25V_{DD}	
Input clock frequency	FCL2	CL2		2.5 to 6.0	0		500	kHz

[Notes]
The specifications above are for a die mounted in a QFP100E type package.
However, we ship this product as a die only, not a package chip.
Therefore, the operational characteristics may vary depending on the user's packaging techniques.

3. Electrical Characteristics at Ta= −30°C to +70°C, V_{SS}=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				V_{DD} [V]	min.	typ.	max.	
Output high voltage	I_{OH}(1)	DB80 to DB7	•Output mode •I_{OH}= −0.6mA	4.5 to 6.0	2.4		V_{DD}	V
			•Output mode •I_{OH}= −0.1mA	2.5 to 6.0	V_{DD} −0.5		V_{DD}	
Output low voltage	V_{OL}(1)	DB0 to DB7	•Output mode •I_{OH}=+0.6mA	4.5 to 6.0	0		0.4	
			•Output mode •I_{OH}=+0.1mA	2.5 to 6.0	0		0.4	
V_{DD}-Si drop voltage (i:1 to 80)	V_D(1)	S1 to S80	•Si terminal for −90μA •V_{DD} −V5=11V	4.5 to 6.0				mV
			•Si terminal for −15μA •V_{DD} −V5=11V	2.5 to 6.0			120	
VX-Si drop voltage (X:2, 3) (i:1 to 80)	V_D(2)	S1 to S80	•Si terminal for -90μA •V_{DD} −V5=11V	4.5 to 6.0				mV
			•Si terminal for −15μA •V_{DD} −V5=11V	2.5 to 6.0			120	
Pull-up resistor	Rpu(1)	DB0 to DB7	•Input mode •V_{IN}=0V	4.5 to 6.0	150	500	900	kΩ
			•Input mode •V_{IN}=0V	2.5 to 4.5	300	750	1500	
	Rpu(2)	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RS, $\overline{RES}$	V_{IN}=0V	4.5 to 6.0	150	500	900	
			V_{IN}=0V	2.5 to 4.5	300	750	1500	
Pull-down resistor	RPD(1)	CL2	V_{IN}=0V	4.5 to 6.0	150	500	900	kΩ
			V_{IN}=0V	2.5 to 4.5	300	750	1500	
Hysteresis voltage	VHIS	$\overline{RES}$		2.5 to 6.0		0.1V_{DD}		V
Current dissipation at operaion	I_{DD}(1)		•FCL2=500kHz •Figure 1	4.5 to 6.0				mA
			•FCL2=500kHz •Figure 1	2.5 to 4.5				
Current dissipation at stand-by mode	I_{DD}(2)		•FCL2=0Hz •V2=V3=V5=V_{DD} •Figure 2	4.5 to 6.0		0.05	30	μA
			•FCL2=0Hz •V2=V3=V5=V_{DD} •Figure 2	2.5 to 4.5		0.02	20	

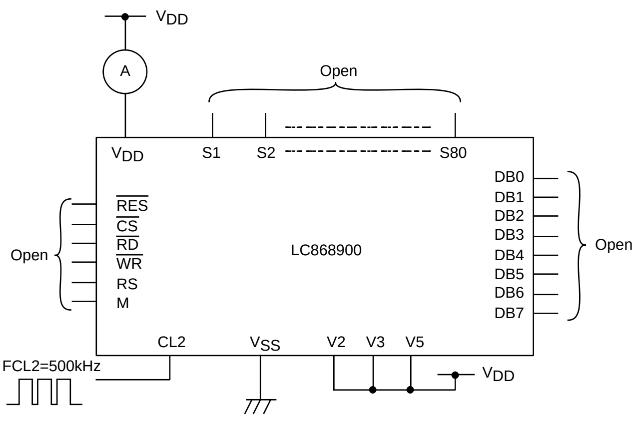


Figure1. Current dissipation measuring circuit at operation ILC00173

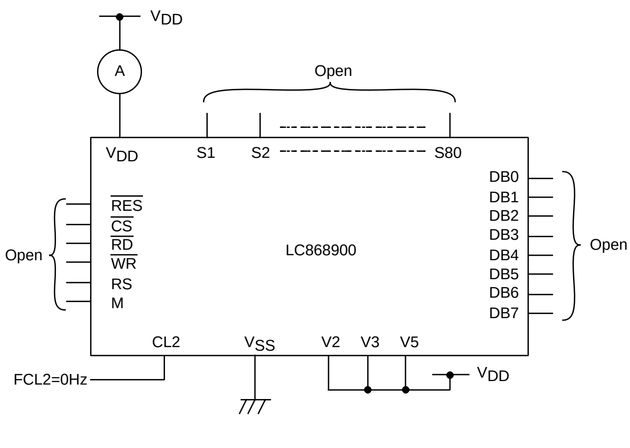
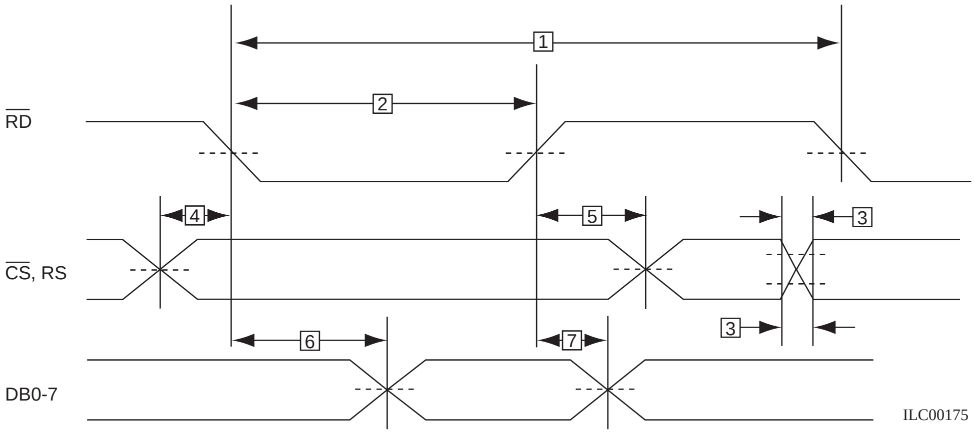


Figure2. Current dissipation measuring circuit at stand-by mode ILC00174

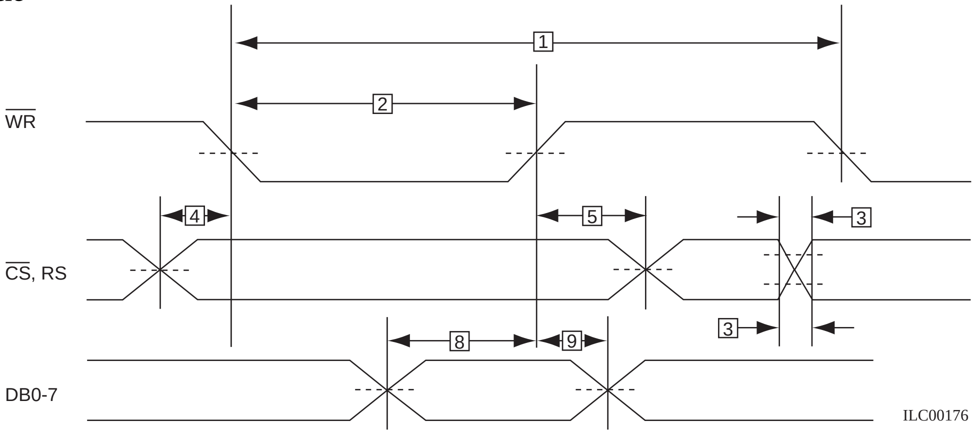
4. AC Characteristics at Ta= –30°C to +70°C, V_{SS}=0V

(1) MPU Interface

1. Reading cycle



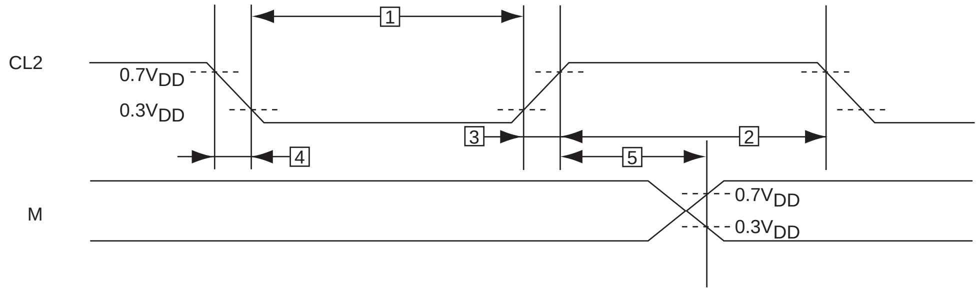
2. Writing cycle



No.	Item	Symbol	Conditions		Value		unit
				V_{DD} [V]	min.	max.	
1	$\overline{RD}$, $\overline{WR}$ cycle time	tcyc1	$\overline{RD}$	4.5 to 6.0	(500)		ns
				2.5 to 4.5			
		tcyc2	$\overline{WR}$	4.5 to 6.0	(500)		ns
				2.5 to 4.5			
2	$\overline{RD}$ pulse width $\overline{WR}$ pulse width	tpw1	$\overline{RD}$ $\overline{WR}$	4.5 to 6.0	(220)		ns
				2.5 to 4.5			
3	Rise / fall time	tr1, tf1	$\overline{RD}$	4.5 to 6.0		(20)	ns
				2.5 to 4.5			
4	Address set-up time	tAS1	$\overline{CS}$, RS, $\overline{RD}$	4.5 to 6.0	(40)		ns
				2.5 to 4.5			
		tAS2	$\overline{CS}$, RS, $\overline{WR}$	4.5 to 6.0	(40)		ns
				2.5 to 4.5			
5	Address hold time	tAH1	$\overline{CS}$, RS, $\overline{RD}$	4.5 to 6.0	(10)		ns
				2.5 to 4.5			
		tAH2	$\overline{CS}$, RS, $\overline{WR}$	4.5 to 6.0	(10)		ns
				2.5 to 4.5			
6	Data delay time	tDDR1	$\overline{RD}$, DB0 to DB7, CL=50pF	4.5 to 6.0		(120)	ns
				2.5 to 4.5			
7	Data hold time	tDHR1	$\overline{RD}$, DB0 to DB7, CL=50pF	4.5 to 6.0	(20)		ns
				2.5 to 4.5			
8	Data set-up time	tDSW1	$\overline{WR}$, DB0 to DB7, CL=50pF	4.5 to 6.0	(60)		ns
				2.5 to 4.5			
9	Data hold time	tDHW1	$\overline{WR}$, DB0 to DB7, CL=50pF	4.5 to 6.0	(10)		ns
				2.5 to 4.5			

CL=Load capacitance

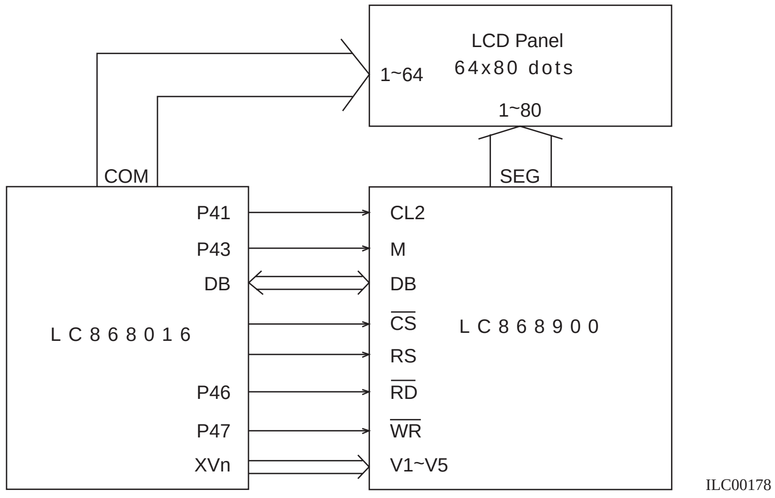
(2) Display Control Timing / Ta= –30°C to +70°C, V_{SS}=0V



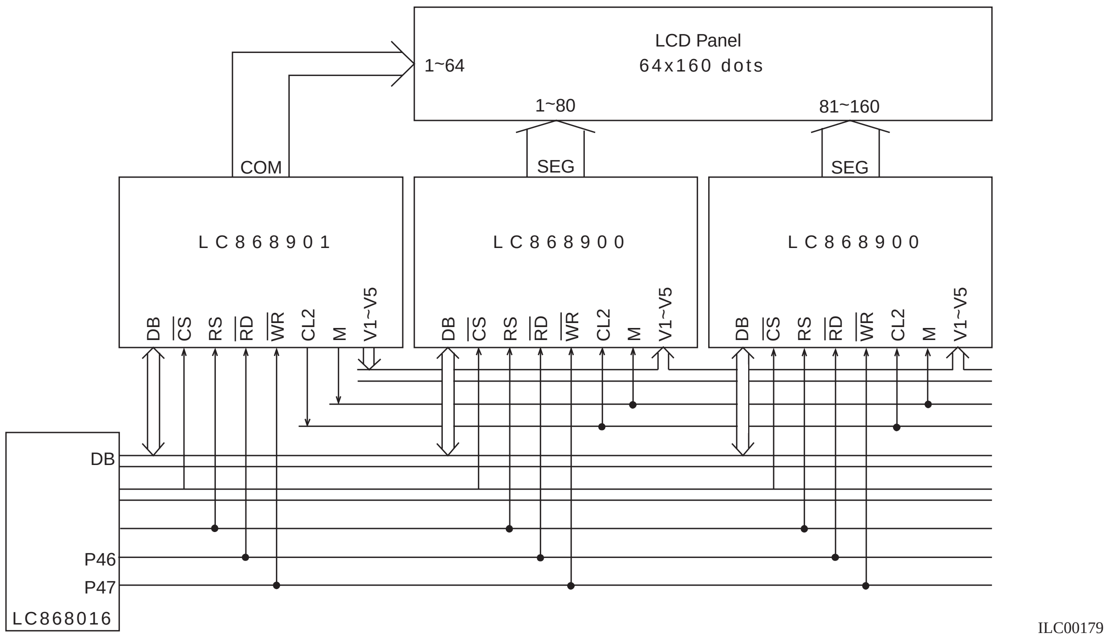
No.	Item	Symbol	Conditions		Value		unit
				V_{DD} [V]	min.	max.	
1	Low level pulse width	tWLCL2	LC2	4.5 to 6.0	(800)		ns
				2.5 to 4.5			
2	High level pulse width	tWLCL2	LC2	4.5 to 6.0	(800)		ns
				2.5 to 4.5			
3	Rise time	tr	CL2	4.5 to 6.0		(20)	ns
				2.5 to 4.5			
4	Fall time	tf	CL2	4.5 to 6.0		(20)	ns
				2.5 to 4.5			
5	M delay time	tDM	M	4.5 to 6.0		(60)	ns
				2.5 to 4.5			

• Example of the reference circuit

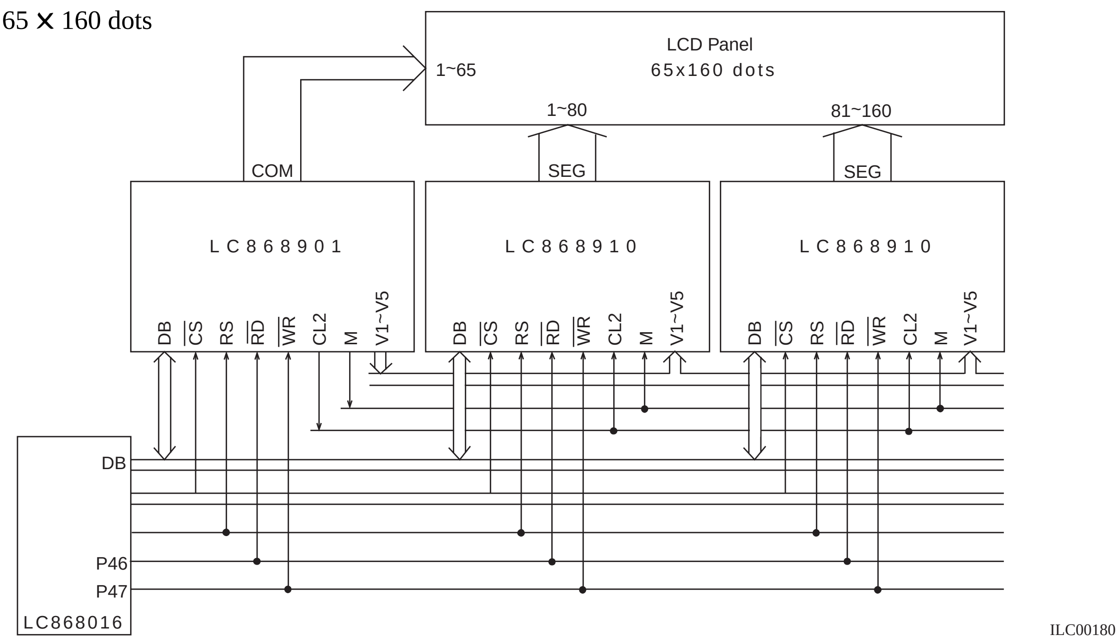
1. 64 × 80 dots



2. 64 × 160 dots



3. 65 × 160 dots



Functions

1. Display Control instructions
    - Display is controlled by writing data into the instruction register and 10 data registers.
    - The instruction register and the data register are distinguished by the RS signal.
    - First, write 4-bit data into the instruction register when RS=1, then specify the code of the data register. Next, with RS=0, write 8-bit data in the data register, which executes the specified instruction.
    - A new instruction cannnot be accepted while an old instruction is being excuted. As the BUSY flag is set under this condition, write an instruction only after reading the BUSY flag and making sure that it is '0'.
    - The BUSY flag does not change when data is written into the instruction register (RS=1). The flag is set when the data is written into the data register at RS=0. Therefore, the BUSY flag need not be checked immediately after writing data into the instruction register.

>< **Instruction register and 10 data registers** ><

1. Set display mode
   Write code '00H' (in hexadecimal notation) into the instruction register and specify the mode control register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	0	0	0	0
MODE	0	0	0	0	0	–	Mode data (MODE)			

- MODE0 bit0 of MODE
  MODE0=1 : Screen1 display ON
  MODE0=0 : Screen1 display OFF
- MODE1 bit1 of MODE
  MODE1=1 : Screen2 display ON
  MODE1=0 : Screen2 display OFF
- MODE2 bit2 of MODE
  MODE2=1 : Exclusive-OR display between Screen1 and Screen2
  MODE2=0 : OR display between Screen1 and Screen2
- MODE3 bit3 of MODE
  MODE3=1 : Output data right-shift (S1 to S80)
  MODE3=0 : Output data left-shift (S80 to S1)

[Note]
- MODE7 to MODE5 must take '0'. A malfunction occurs when one of these bits takes '1'.

2. Set display pitch
   Write code '01H' (in hexadecimal notation) into the instruction register and specify the Display Pitch register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	0	0	0	1
PITCH	0	0	–	–	–	–	–	Dp–1		

• Dp indicates how many bits (or dots) from RAM appear in a 1-byte display.
• Dp must take one of the following three value.

Dp	DB2	DB1	DB0	Display pitch
6	1	0	1	6
7	1	1	0	7
8	1	1	1	8

3. Set display number
Write code '02H' (in hexadecimal notation) into the instruction register and specify the Display Number register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	0	0	1	0
NUMBER	0	0	–	–	–	–	Dn–1			

• Dn indicates the number of bytes in the horizontal direction.
• The total number of dots positioned horizontally on the screen, N is given by the following formura.

$$N=Dp * Dn \ (N \leq 80)$$

• Numbers in the range 2 to 10 (in decimal) can be set as Dn.

4. Set number of time division
Write code '03H' (in hexadecimal notation) into the instruction register and specify the Time Division register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	0	0	1	1
Division	0	0	0	Nx–1						

• Nx represents the number of time divisions.
• Consequently, 1 / Nx is the display duty.
• Numbers in the range 2 to 65 (in decimal) can be set as Nx.

5. Set screen1 display start address
Write code '08H' (in hexadecimal notation) into the instruction register and specify the Screen1 Start Address register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	1	0	0	0
Screen1	0	0	0	Screen1 Start Address						

• This instruction writes the display-start upper address value in the Screen1 Start Address register.
• The display start address is the RAM address at whitch data to be displayed at the leftmost position (MODE3=0) or the rightmost position (MODE3=1) of the top line of the screen is stored.

MODE3=1 : Start the rightmost position
MODE3=0 : Start the leftmost position

- The start upper address counter is a 7-bit down-counter with preset function. The start upper address is decremented by one when a start lower address has an underflow. When the start upper address is decremented during 0 state, it is set the start addressvalue automatically.

Internal RAM=1280 bytes : Start upper address counter=7FH
Internal RAM= 640 bytes : Start upper address counter=3FH

6. Set screen2 display start address
Write code '09H' (in hexadecimal notation) into the instruction register and specify the Screen2 Start Address register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	1	0	0	1
Screen2	0	0	0	Screen2 Start Address						

- This instruction writes the display-start upper address value in the Screen2 Start Address register.
- The display start address is the RAM address at whitch data to be displayed at the leftmost position (MODE3=0) or the rightmost position (MODE3=1) of the top line of the screen is stored.

MODE3=1 : Start the rightmost position
MODE3=0 : Start the leftmost position

- The start upper address counter is a 7-bit down-counter with preset function. The start upper address is decremented by one when a start lower address has an underflow.When the start upper address is decremented during 0 state, it is set the start address value automatically.

Internal RAM=1280 bytes : Start upper address counter=7FH
Internal RAM= 640 bytes : Start upper address counter=3FH

7. Set cursor (lower) address (RAM read/write lower address)
Write code '0AH' (in hexadecimal notation) into the instruction register and the lower cursor address register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	1	0	1	0
Lower	0	0	0	0	0	0	Lower cursor address			

- This instruction writes the cursor address value in the cursor address counter. The curosr address indicates the address for exchanging display data with display RAM. In other words, data at the address specified by the cursor address is read form or written into display RAM. The cursor address in divided into a lower address (4 bits) .
The cursor lower address counter is a 4-bit down-counter with preset function. The cursor lower address is decreased by one every RAM read/write timing. When the cursor lower address is decreased during 0 state, it is set Dn-1 automatically.

8. Set cursor (upper) address (RAM read / write upper address)
Write code '0BH' (in hexadecimal notation) into the instruction register and the upper cursor address register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	1	0	1	1
Upper	0	0	0	Upper cursor address						

- This instruction writes the cursor address value in the cursor address counter. The curosr address indicates the address for exchanging display data with display RAM. In other words, data at the address specified by the cursor address is read form or written into display RAM. The cursor address in divided into an upper addres (7 bits).
The cursor upper address counter is a 7-bit down-counter with preset funciton. The cursor upper address is decreased by one when cursor lower address has an underflow. When the cursor upper address is decreased during 0 state, it is set cursor upper address number automatically.

9. Writing display data
Write code '0EH' (in hexadecimal notation) into the instruction register.

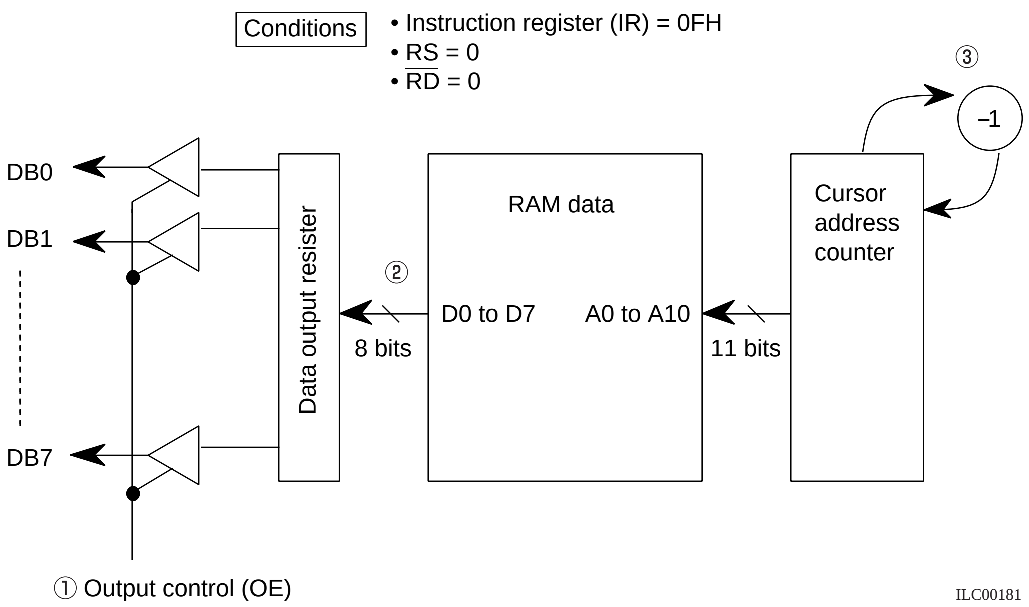
REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	1	1	1	0
RAM	0	0	MSB						LSB	

- After writing code '0EH' , write 8-bit data with RS=0, and the data is written into RAM as display data at the address specified by the cursor adress counter. After writing, the count of the cursor address counter decrements by one.

10. Reading display data
Write code '0FH' (in hexadecimal notation) into the instruction register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	1	1	1	1
RAM	1	0	MSB						LSB	

The read status is established with RS=0, and data in RAM can be read. The procedure for reading data is as follows:
1. The instruction outputs the contents of the data output register to DB0 to DB7.
2. Transfer the RAM data indicated by the cursor address to the data output registser.
3. It then decrements the cursor address by one. Refer to next figure.

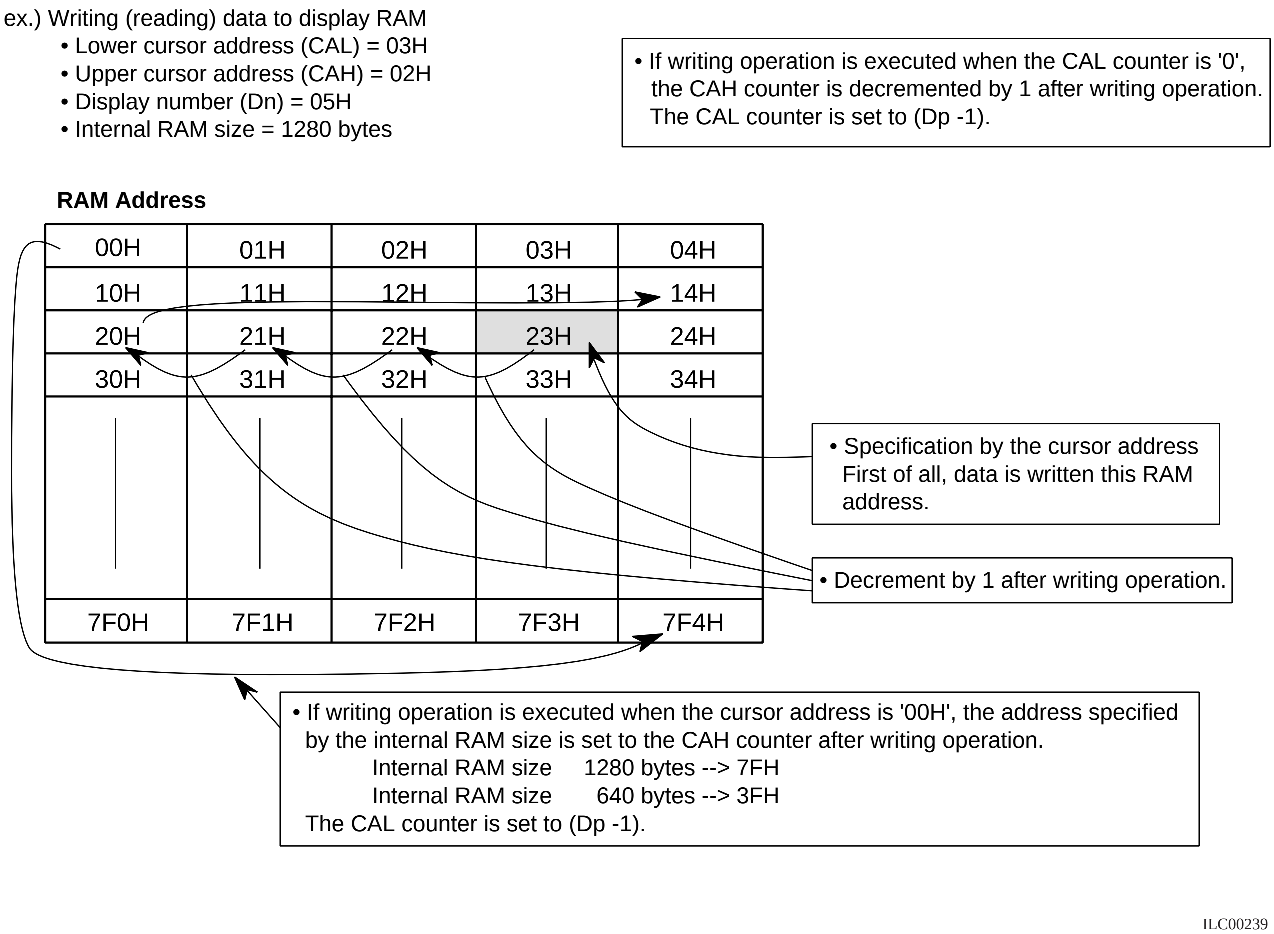


• The correct data cannot be read in the first read operation. The specified value is output in the second read operation. Accordingly, a dummy read operation must be performed once when reading data after setting the cursor address.

11. Read Busy flag

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	1	1	1	1
Busy	1	1	1 / 0	no meaning						

• The Busy flag is output to DB7 when read mode is extablished with RS=1. The Busy flag is set to 1 while any of the instructions (1) through (10) is being executed. It is set to 0 at the completion of the execution, allowing the next instruction to be accepted. No other instruction can be accepted when the Busy flag is 1. Accordingly, before writing an instruction and data, it is necessary to ensure that the Busy flag is 0. However, the next instruction can be executed without checking the Busy flag when the maximum read cycle time or the write cycle time has been exceeded after execution of the previous data read instruction or the data write instruction.
The Busy flag does not change when data is written into the instruction register (RS=1).
This flag is set when data is written into the data register (RS=0). Therefore, the Busy flag need not be checked immediately after writing data into the instruction register. Specification of the instruction register is unnecessary to read the Busy flag.



Display examples

1. Mode control register=01H (screen1 : ON, screen2 : OFF, S80 → S1)
   Dp=8, Dn=10, Nx=64, Screen1 start address register=3FH

	S1 --------- S8	S9 -------- S16	S17 ------ S24	S25 ------ S32	S33 ------ S40	S41 ------ S48	S49 ------ S56	S57 ------ S64	S65 ------ S72	S73 ------ S80
C1	LSB (3F9H) MSB	LSB (3F8H) MSB	LSB (3F7H) MSB	LSB (3F6H) MSB	LSB (3F5H) MSB	LSB (3F4H) MSB	LSB (3F3H) MSB	LSB (3F2H) MSB	LSB (3F1H) MSB	LSB (3F0H) MSB
C2	LSB (3E9H) MSB	LSB (3E8H) MSB	LSB (3E7H) MSB	LSB (3E6H) MSB	LSB (3E5H) MSB	LSB (3E4H) MSB	LSB (3E3H) MSB	LSB (3E2H) MSB	LSB (3E1H) MSB	LSB (3E0H) MSB
C3	LSB (3D9H) MSB	LSB (3D8H) MSB	LSB (3D7H) MSB	LSB (3D6H) MSB	LSB (3D5H) MSB	LSB (3D4H) MSB	LSB (3D3H) MSB	LSB (3D2H) MSB	LSB (3D1H) MSB	LSB (3D0H) MSB
C60	LSB (049H) MSB	LSB (048H) MSB	LSB (047H) MSB	LSB (046H) MSB	LSB (045H) MSB	LSB (044H) MSB	LSB (043H) MSB	LSB (042H) MSB	LSB (041H) MSB	LSB (040H) MSB
C61	LSB (039H) MSB	LSB (038H) MSB	LSB (037H) MSB	LSB (036H) MSB	LSB (035H) MSB	LSB (034H) MSB	LSB (033H) MSB	LSB (032H) MSB	LSB (031H) MSB	LSB (030H) MSB
C62	LSB (029H) MSB	LSB (028H) MSB	LSB (027H) MSB	LSB (026H) MSB	LSB (025H) MSB	LSB (024H) MSB	LSB (023H) MSB	LSB (022H) MSB	LSB (021H) MSB	LSB (020H) MSB
C63	LSB (019H) MSB	LSB (018H) MSB	LSB (017H) MSB	LSB (016H) MSB	LSB (015H) MSB	LSB (014H) MSB	LSB (013H) MSB	LSB (012H) MSB	LSB (011H) MSB	LSB (010H) MSB
C64	LSB (009H) MSB	LSB (008H) MSB	LSB (007H) MSB	LSB (006H) MSB	LSB (005H) MSB	LSB (004H) MSB	LSB (003H) MSB	LSB (002H) MSB	LSB (001H) MSB	LSB (000H) MSB

ILC00182

2. Mode control register=09H (screen1 : ON, screen2 : OFF, S1 → S80)
   Dp=8, Dn=10, Nx=64, Screen1 start address register=3FH

	S1 --------- S8	S9 -------- S16	S17 ------ S24	S25 ------ S32	S33 ------ S40	S41 ------ S48	S49 ------ S56	S57 ------ S64	S65 ------ S72	S73 ------ S80
C1	MSB (3F0H) LSB	MSB (3F1H) LSB	MSB (3F2H) LSB	MSB (3F3H) LSB	MSB (3F4H) LSB	MSB (3F5H) LSB	MSB (3F6H) LSB	MSB (3F7H) LSB	MSB (3F8H) LSB	MSB (3F9H) LSB
C2	MSB (3E0H) LSB	MSB (3E1H) LSB	MSB (3E2H) LSB	MSB (3E3H) LSB	MSB (3E4H) LSB	MSB (3E5H) LSB	MSB (3E6H) LSB	MSB (3E7H) LSB	MSB (3E8H) LSB	MSB (3E9H) LSB
C3	MSB (3D0H) LSB	MSB (3D1H) LSB	MSB (3D2H) LSB	MSB (3D3H) LSB	MSB (3D4H) LSB	MSB (3D5H) LSB	MSB (3D6H) LSB	MSB (3D7H) LSB	MSB (3D8H) LSB	MSB (3D9H) LSB
C60	MSB (040H) LSB	MSB (041H) LSB	MSB (042H) LSB	MSB (043H) LSB	MSB (044H) LSB	MSB (045H) LSB	MSB (046H) LSB	MSB (047H) LSB	MSB (048H) LSB	MSB (049H) LSB
C61	MSB (030H) LSB	MSB (031H) LSB	MSB (032H) LSB	MSB (033H) LSB	MSB (034H) LSB	MSB (035H) LSB	MSB (036H) LSB	MSB (037H) LSB	MSB (038H) LSB	MSB (039H) LSB
C62	MSB (020H) LSB	MSB (021H) LSB	MSB (022H) LSB	MSB (023H) LSB	MSB (024H) LSB	MSB (025H) LSB	MSB (026H) LSB	MSB (027H) LSB	MSB (028H) LSB	MSB (029H) LSB
C63	MSB (010H) LSB	MSB (011H) LSB	MSB (012H) LSB	MSB (013H) LSB	MSB (014H) LSB	MSB (015H) LSB	MSB (016H) LSB	MSB (017H) LSB	MSB (018H) LSB	MSB (019H) LSB
C64	MSB (000H) LSB	MSB (001H) LSB	MSB (002H) LSB	MSB (003H) LSB	MSB (004H) LSB	MSB (005H) LSB	MSB (006H) LSB	MSB (007H) LSB	MSB (008H) LSB	MSB (009H) LSB

ILC00183

3. Mode control register=09H (screen1 : ON, screen2 : OFF, S1 → S80)
   Dp=8, Dn=10, Nx=64, Screen1 start address register=3EH
   Internal display RAM : 1280 bytes

	S1 --------- S8	S9 -------- S16	S17 ------ S24	S25 ------ S32	S33 ------ S40	S41 ------ S48	S49 ------ S56	S57 ------ S64	S65 ------ S72	S73 ------ S80
C1	MSB (3E0H) LSB	MSB (3E1H) LSB	MSB (3E2H) LSB	MSB (3E3H) LSB	MSB (3E4H) LSB	MSB (3E5H) LSB	MSB (3E6H) LSB	MSB (3E7H) LSB	MSB (3E8H) LSB	MSB (3E9H) LSB
C2	MSB (3D0H) LSB	MSB (3D1H) LSB	MSB (3D2H) LSB	MSB (3D3H) LSB	MSB (3D4H) LSB	MSB (3D5H) LSB	MSB (3D6H) LSB	MSB (3D7H) LSB	MSB (3D8H) LSB	MSB (3D9H) LSB
C3	MSB (3C0H) LSB	MSB (3C1H) LSB	MSB (3C2H) LSB	MSB (3C3H) LSB	MSB (3C4H) LSB	MSB (3C5H) LSB	MSB (3C6H) LSB	MSB (3C7H) LSB	MSB (3C8H) LSB	MSB (3C9H) LSB
C60	MSB (030H) LSB	MSB (031H) LSB	MSB (032H) LSB	MSB (033H) LSB	MSB (034H) LSB	MSB (035H) LSB	MSB (036H) LSB	MSB (037H) LSB	MSB (038H) LSB	MSB (039H) LSB
C61	MSB (020H) LSB	MSB (021H) LSB	MSB (022H) LSB	MSB (023H) LSB	MSB (024H) LSB	MSB (025H) LSB	MSB (026H) LSB	MSB (027H) LSB	MSB (028H) LSB	MSB (029H) LSB
C62	MSB (010H) LSB	MSB (011H) LSB	MSB (012H) LSB	MSB (013H) LSB	MSB (014H) LSB	MSB (015H) LSB	MSB (016H) LSB	MSB (017H) LSB	MSB (018H) LSB	MSB (019H) LSB
C63	MSB (000H) LSB	MSB (001H) LSB	MSB (002H) LSB	MSB (003H) LSB	MSB (004H) LSB	MSB (005H) LSB	MSB (006H) LSB	MSB (007H) LSB	MSB (008H) LSB	MSB (009H) LSB
C64	MSB (7F0H) LSB	MSB (7F1H) LSB	MSB (7F2H) LSB	MSB (7F3H) LSB	MSB (7F4H) LSB	MSB (7F5H) LSB	MSB (7F6H) LSB	MSB (7F7H) LSB	MSB (7F8H) LSB	MSB (7F9H) LSB

ILC00184

4. Mode control register=09H (screen1 : ON, screen2 : OFF, S1 → S80)
Dp=8, Dn=10, Nx=64, Screen1 start address register=3EH
Internal display RAM : 640 bytes

	S1 --------- S8	S9 -------- S16	S17 ------ S24	S25 ------ S32	S33 ------ S40	S41 ------ S48	S49 ------ S56	S57 ------ S64	S65 ------ S72	S73 ------ S80
C1	MSB (3E0H) LSB	MSB (3E1H) LSB	MSB (3E2H) LSB	MSB (3E3H) LSB	MSB (3E4H) LSB	MSB (3E5H) LSB	MSB (3E6H) LSB	MSB (3E7H) LSB	MSB (3E8H) LSB	MSB (3E9H) LSB
C2	MSB (3D0H) LSB	MSB (3D1H) LSB	MSB (3D2H) LSB	MSB (3D3H) LSB	MSB (3D4H) LSB	MSB (3D5H) LSB	MSB (3D6H) LSB	MSB (3D7H) LSB	MSB (3D8H) LSB	MSB (3D9H) LSB
C3	MSB (3C0H) LSB	MSB (3C1H) LSB	MSB (3C2H) LSB	MSB (3C3H) LSB	MSB (3C4H) LSB	MSB (3C5H) LSB	MSB (3C6H) LSB	MSB (3C7H) LSB	MSB (3C8H) LSB	MSB (3C9H) LSB
C60	MSB (030H) LSB	MSB (031H) LSB	MSB (032H) LSB	MSB (033H) LSB	MSB (034H) LSB	MSB (035H) LSB	MSB (036H) LSB	MSB (037H) LSB	MSB (038H) LSB	MSB (039H) LSB
C61	MSB (020H) LSB	MSB (021H) LSB	MSB (022H) LSB	MSB (023H) LSB	MSB (024H) LSB	MSB (025H) LSB	MSB (026H) LSB	MSB (027H) LSB	MSB (028H) LSB	MSB (029H) LSB
C62	MSB (010H) LSB	MSB (011H) LSB	MSB (012H) LSB	MSB (013H) LSB	MSB (014H) LSB	MSB (015H) LSB	MSB (016H) LSB	MSB (017H) LSB	MSB (018H) LSB	MSB (019H) LSB
C63	MSB (000H) LSB	MSB (001H) LSB	MSB (002H) LSB	MSB (003H) LSB	MSB (004H) LSB	MSB (005H) LSB	MSB (006H) LSB	MSB (007H) LSB	MSB (008H) LSB	MSB (009H) LSB
C64	MSB (3F0H) LSB	MSB (3F1H) LSB	MSB (3F2H) LSB	MSB (3F3H) LSB	MSB (3F4H) LSB	MSB (3F5H) LSB	MSB (3F6H) LSB	MSB (3F7H) LSB	MSB (3F8H) LSB	MSB (3F9H) LSB

ILC00185

5. Mode control register=03H (screen1 : ON, screen2 : ON, logical or output of screen1 and screen2, S80 → S1)
Dp=8, Dn=10, Nx=64, Screen1 start address register=3FH
Screen2 start address register=7FH, Internal display RAM : 1280 bytes

	S1 ------------- S8	S9 ------------ S16	S17 ----------- S24	S25 ----------- S32		S65 ------------ S72	S73 ------------ S80
C1	LSB (3F9H OR 7F9H) MSB	LSB (3F8H OR 7F8H) MSB	LSB (3F7H OR 7F7H) MSB	LSB (3F6H OR 7F6H) MSB		LSB (3F1H OR 7F1H) MSB	LSB (3F0H OR 7F0H) MSB
C2	LSB (3E9H OR 7E9H) MSB	LSB (3E8H OR 7E8H) MSB	LSB (3E7H OR 7E7H) MSB	LSB (3E6H OR 7E6H) MSB		LSB (3E1H OR 7E1H) MSB	LSB (3E0H OR 7E0H) MSB
C3	LSB (3D9H OR 7D9H) MSB	LSB (3D8H OR 7D8H) MSB	LSB (3D7H OR 7D7H) MSB	LSB (3D6H OR 7D6H) MSB		LSB (3D1H OR 7D1H) MSB	LSB (3D0H OR 7D0H) MSB
C60	LSB (049H OR 449H) MSB	LSB (048H OR 448H) MSB	LSB (047H OR 447H) MSB	LSB (046H OR 446H) MSB		LSB (041H OR 441H) MSB	LSB (040H OR 440H) MSB
C61	LSB (039H OR 439H) MSB	LSB (038H OR 438H) MSB	LSB (037H OR 437H) MSB	LSB (036H OR 436H) MSB		LSB (031H OR 431H) MSB	LSB (030H OR 430H) MSB
C62	LSB (029H OR 429H) MSB	LSB (028H OR 428H) MSB	LSB (027H OR 427H) MSB	LSB (026H OR 426H) MSB		LSB (021H OR 421H) MSB	LSB (020H OR 420H) MSB
C63	LSB (019H OR 419H) MSB	LSB (018H OR 418H) MSB	LSB (017H OR 417H) MSB	LSB (016H OR 416H) MSB		LSB (011H OR 411H) MSB	LSB (010H OR 410H) MSB
C64	LSB (009H OR 409H) MSB	LSB (008H OR 408H) MSB	LSB (007H OR 407H) MSB	LSB (006H OR 406H) MSB		LSB (001H OR 401H) MSB	LSB (000H OR 400H) MSB

ILC00186

6. Mode control register=03H (screen1 : ON, screen2 : ON, logical or output of screen1 and screen2, S80 → S1)
Dp=8, Dn=10, Nx=32, Screen1 start address register=3FH
Screen2 start address register=1FH, Internal display RAM : 640 bytes

	S1 ------------- S8	S9 ------------ S16	S17 ----------- S24	S25 ----------- S32		S65 ------------ S72	S73 ------------ S80
C1	LSB (3F9H OR 1F9H) MSB	LSB (3F8H OR 1F8H) MSB	LSB (3F7H OR 1F7H) MSB	LSB (3F6H OR 1F6H) MSB		LSB (3F1H OR 1F1H) MSB	LSB (3F0H OR 1F0H) MSB
C2	LSB (3E9H OR 1E9H) MSB	LSB (3E8H OR 1E8H) MSB	LSB (3E7H OR 1E7H) MSB	LSB (3E6H OR 1E6H) MSB		LSB (3E1H OR 1E1H) MSB	LSB (3E0H OR 1E0H) MSB
C3	LSB (3D9H OR 1D9H) MSB	LSB (3D8H OR 1D8H) MSB	LSB (3D7H OR 1D7H) MSB	LSB (3D6H OR 1D6H) MSB		LSB (3D1H OR 1D1H) MSB	LSB (3D0H OR 1D0H) MSB
C28	LSB (249H OR 049H) MSB	LSB (248H OR 048H) MSB	LSB (247H OR 047H) MSB	LSB (246H OR 046H) MSB		LSB (241H OR 041H) MSB	LSB (240H OR 040H) MSB
C29	LSB (239H OR 039H) MSB	LSB (238H OR 038H) MSB	LSB (237H OR 037H) MSB	LSB (236H OR 036H) MSB		LSB (231H OR 031H) MSB	LSB (230H OR 030H) MSB
C30	LSB (229H OR 029H) MSB	LSB (228H OR 028H) MSB	LSB (227H OR 027H) MSB	LSB (226H OR 026H) MSB		LSB (221H OR 021H) MSB	LSB (220H OR 020H) MSB
C31	LSB (219H OR 019H) MSB	LSB (218H OR 018H) MSB	LSB (217H OR 017H) MSB	LSB (216H OR 016H) MSB		LSB (211H OR 011H) MSB	LSB (210H OR 010H) MSB
C32	LSB (209H OR 009H) MSB	LSB (208H OR 008H) MSB	LSB (207H OR 007H) MSB	LSB (206H OR 006H) MSB		LSB (201H OR 001H) MSB	LSB (200H OR 000H) MSB

ILC00187

7. Mode control register=07H (screen1 : ON, screen2 : ON, exclusive-OR output of screen1 and screen2, S80 → S1)
Dp=8, Dn=10, Nx=64, Screen1 start address register=3FH
Screen2 start address register=7FH, Internal display RAM : 1280 bytes

	S1 ------------ S8	S9 ------------ S16	S17 ----------- S24	S25 ----------- S32		S65 ------------ S72	S73 ------------ S80
C1	LSB (3F9H EOR 7F9H) MSB	LSB (3F8H EOR 7F8H) MSB	LSB (3F7H EOR 7F7H) MSB	LSB (3F6H EOR 7F6H) MSB		LSB (3F1H EOR 7F1H) MSB	LSB (3F0H EOR 7F0H) MSB
C2	LSB (3E9H EOR 7E9H) MSB	LSB (3E8H EOR 7E8H) MSB	LSB (3E7H EOR 7E7H) MSB	LSB (3E6H EOR 7E6H) MSB		LSB (3E1H EOR 7E1H) MSB	LSB (3E0H EOR 7E0H) MSB
C3	LSB (3D9H EOR 7D9H) MSB	LSB (3D8H EOR 7D8H) MSB	LSB (3D7H EOR 7D7H) MSB	LSB (3D6H EOR 7D6H) MSB		LSB (3D1H EOR 7D1H) MSB	LSB (3D0H EOR 7D0H) MSB
C60	LSB (049H EOR 449H) MSB	LSB (048H EOR 448H) MSB	LSB (047H EOR 447H) MSB	LSB (046H EOR 446H) MSB		LSB (041H EOR 441H) MSB	LSB (040H EOR 440H) MSB
C61	LSB (039H EOR 439H) MSB	LSB (038H EOR 438H) MSB	LSB (037H EOR 437H) MSB	LSB (036H EOR 436H) MSB		LSB (031H EOR 431H) MSB	LSB (030H EOR 430H) MSB
C62	LSB (029H EOR 429H) MSB	LSB (028H EOR 428H) MSB	LSB (027H EOR 427H) MSB	LSB (026H EOR 426H) MSB		LSB (021H EOR 421H) MSB	LSB (020H EOR 420H) MSB
C63	LSB (019H EOR 419H) MSB	LSB (018H EOR 418H) MSB	LSB (017H EOR 417H) MSB	LSB (016H EOR 416H) MSB		LSB (011H EOR 411H) MSB	LSB (010H EOR 410H) MSB
C64	LSB (009H EOR 409H) MSB	LSB (008H EOR 408H) MSB	LSB (007H EOR 407H) MSB	LSB (006H EOR 406H) MSB		LSB (001H EOR 401H) MSB	LSB (000H EOR 400H) MSB

ILC00188

8. Mode control register=07H (screen1 : ON, screen2 : ON, exclusive-OR output of screen1 and screen2, S80 → S1)
Dp=8, Dn=10, Nx=16, Screen1 start address register=3FH
Screen2 start address register=0FH

	S1 ------------ S8	S9 ------------ S16	S17 ----------- S24	S25 ----------- S32		S65 ------------ S72	S73 ------------ S80
C1	LSB (3F9H EOR 0F9H) MSB	LSB (3F8H EOR 0F8H) MSB	LSB (3F7H EOR 0F7H) MSB	LSB (3F6H EOR 0F6H) MSB		LSB (3F1H EOR 0F1H) MSB	LSB (3F0H EOR 0F0H) MSB
C2	LSB (3E9H EOR 0E9H) MSB	LSB (3E8H EOR 0E8H) MSB	LSB (3E7H EOR 0E7H) MSB	LSB (3E6H EOR 0E6H) MSB		LSB (3E1H EOR 0E1H) MSB	LSB (3E0H EOR 0E0H) MSB
C3	LSB (3D9H EOR 0D9H) MSB	LSB (3D8H EOR 0D8H) MSB	LSB (3D7H EOR 0D7H) MSB	LSB (3D6H EOR 0D6H) MSB		LSB (3D1H EOR 0D1H) MSB	LSB (3D0H EOR 0D0H) MSB
C12	LSB (349H EOR 049H) MSB	LSB (348H EOR 048H) MSB	LSB (347H EOR 047H) MSB	LSB (346H EOR 046H) MSB		LSB (341H EOR 041H) MSB	LSB (340H EOR 040H) MSB
C13	LSB (339H EOR 039H) MSB	LSB (338H EOR 038H) MSB	LSB (337H EOR 037H) MSB	LSB (336H EOR 036H) MSB		LSB (331H EOR 031H) MSB	LSB (330H EOR 030H) MSB
C14	LSB (329H EOR 029H) MSB	LSB (328H EOR 028H) MSB	LSB (327H EOR 027H) MSB	LSB (326H EOR 026H) MSB		LSB (321H EOR 021H) MSB	LSB (320H EOR 020H) MSB
C15	LSB (319H EOR 019H) MSB	LSB (318H EOR 018H) MSB	LSB (317H EOR 017H) MSB	LSB (316H EOR 016H) MSB		LSB (311H EOR 011H) MSB	LSB (310H EOR 010H) MSB
C16	LSB (309H EOR 009H) MSB	LSB (308H EOR 008H) MSB	LSB (307H EOR 007H) MSB	LSB (306H EOR 006H) MSB		LSB (301H EOR 001H) MSB	LSB (300H EOR 000H) MSB

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9. Mode control register=07H (screen1 : ON, screen2 : ON, OR output of screen1 and screen2, S80 → S1)
Dp=8, Dn=10, Nx=16, Screen1 start address register=3EH
Screen2 start address register=0FH

	S1 ------------ S8	S9 ------------ S16	S17 ----------- S24	S25 ----------- S32		S65 ------------ S72	S73 ------------ S80
C1	LSB (3E9H EOR 0F9H) MSB	LSB (3E8H EOR 0F8H) MSB	LSB (3E7H EOR 0F7H) MSB	LSB (3E6H EOR 0F6H) MSB		LSB (3E1H EOR 0F1H) MSB	LSB (3E0H EOR 0F0H) MSB
C2	LSB (3D9H EOR 0E9H) MSB	LSB (3D8H EOR 0E8H) MSB	LSB (3D7H EOR 0E7H) MSB	LSB (3D6H EOR 0E6H) MSB		LSB (3D1H EOR 0E1H) MSB	LSB (3D0H EOR 0E0H) MSB
C3	LSB (3C9H EOR 0D9H) MSB	LSB (3C8H EOR 0D8H) MSB	LSB (3C7H EOR 0D7H) MSB	LSB (3C6H EOR 0D6H) MSB		LSB (3C1H EOR 0D1H) MSB	LSB (3C0H EOR 0D0H) MSB
C12	LSB (339H EOR 049H) MSB	LSB (338H EOR 048H) MSB	LSB (337H EOR 047H) MSB	LSB (336H EOR 046H) MSB		LSB (331H EOR 041H) MSB	LSB (330H EOR 040H) MSB
C13	LSB (329H EOR 039H) MSB	LSB (328H EOR 038H) MSB	LSB (327H EOR 037H) MSB	LSB (326H EOR 036H) MSB		LSB (321H EOR 031H) MSB	LSB (320H EOR 030H) MSB
C14	LSB (319H EOR 029H) MSB	LSB (318H EOR 028H) MSB	LSB (317H EOR 027H) MSB	LSB (316H EOR 026H) MSB		LSB (311H EOR 021H) MSB	LSB (310H EOR 020H) MSB
C15	LSB (309H EOR 019H) MSB	LSB (308H EOR 018H) MSB	LSB (307H EOR 017H) MSB	LSB (306H EOR 016H) MSB		LSB (301H EOR 011H) MSB	LSB (300H EOR 010H) MSB
C16	LSB (2F9H EOR 009H) MSB	LSB (2F8H EOR 008H) MSB	LSB (2F7H EOR 007H) MSB	LSB (2F6H EOR 006H) MSB		LSB (2F1H EOR 001H) MSB	LSB (2F0H EOR 000H) MSB

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10. Mode control register=02H (screen1 : OFF, screen2 : ON, S80 $\rightarrow$ S1)
Dp=8, Dn=10, Nx=16, Screen2 start address register=0FH

	S1 --------- S8	S9 -------- S16	S17 ------ S24	S25 ------ S32	S33 ------ S40	S41 ------ S48	S49 ------ S56	S57 ------ S64	S65 ------ S72	S73 ------ S80
C1	LSB (0F9H) MSB	LSB (0F8H) MSB	LSB (0F7H) MSB	LSB (0F6H) MSB	LSB (0F5H) MSB	LSB (0F4H) MSB	LSB (0F3H) MSB	LSB (0F2H) MSB	LSB (0F1H) MSB	LSB (0F0H) MSB
C2	LSB (0E9H) MSB	LSB (0E8H) MSB	LSB (0E7H) MSB	LSB (0E6H) MSB	LSB (0E5H) MSB	LSB (0E4H) MSB	LSB (0E3H) MSB	LSB (0E2H) MSB	LSB (0E1H) MSB	LSB (0E0H) MSB
C3	LSB (0D9H) MSB	LSB (0D8H) MSB	LSB (0D7H) MSB	LSB (0D6H) MSB	LSB (0D5H) MSB	LSB (0D4H) MSB	LSB (0D3H) MSB	LSB (0D2H) MSB	LSB (0D1H) MSB	LSB (0D0H) MSB
C12	LSB (049H) MSB	LSB (048H) MSB	LSB (047H) MSB	LSB (046H) MSB	LSB (045H) MSB	LSB (044H) MSB	LSB (043H) MSB	LSB (042H) MSB	LSB (041H) MSB	LSB (040H) MSB
C13	LSB (039H) MSB	LSB (038H) MSB	LSB (037H) MSB	LSB (036H) MSB	LSB (035H) MSB	LSB (034H) MSB	LSB (033H) MSB	LSB (032H) MSB	LSB (031H) MSB	LSB (030H) MSB
C14	LSB (029H) MSB	LSB (028H) MSB	LSB (027H) MSB	LSB (026H) MSB	LSB (025H) MSB	LSB (024H) MSB	LSB (023H) MSB	LSB (022H) MSB	LSB (021H) MSB	LSB (020H) MSB
C15	LSB (019H) MSB	LSB (018H) MSB	LSB (017H) MSB	LSB (016H) MSB	LSB (015H) MSB	LSB (014H) MSB	LSB (013H) MSB	LSB (012H) MSB	LSB (011H) MSB	LSB (010H) MSB
C16	LSB (009H) MSB	LSB (008H) MSB	LSB (007H) MSB	LSB (006H) MSB	LSB (005H) MSB	LSB (004H) MSB	LSB (003H) MSB	LSB (002H) MSB	LSB (001H) MSB	LSB (000H) MSB

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11. Mode control register=09H (screen1 : ON, screen2 : OFF, S1 $\rightarrow$ S80)
Dp=6, Dn=8, Nx=16, Screen1 start address register=1FH

	S1 ---------- S6	S7 --------- S12	S13 --------- S18	S19 --------- S24	S25 --------- S30	S31 --------- S36	S37 --------- S42	S43 --------- S48
C1	MSB (1F0H) LSB	MSB (1F1H) LSB	MSB (1F2H) LSB	MSB (1F3H) LSB	MSB (1F4H) LSB	MSB (1F5H) LSB	MSB (1F6H) LSB	MSB (1F7H) LSB
C2	MSB (1E0H) LSB	MSB (1E1H) LSB	MSB (1E2H) LSB	MSB (1E3H) LSB	MSB (1E4H) LSB	MSB (1E5H) LSB	MSB (1E6H) LSB	MSB (1E7H) LSB
C3	MSB (1D0H) LSB	MSB (1D1H) LSB	MSB (1D2H) LSB	MSB (1D3H) LSB	MSB (1D4H) LSB	MSB (1D5H) LSB	MSB (1D6H) LSB	MSB (1D7H) LSB
C12	MSB (140H) LSB	MSB (141H) LSB	MSB (142H) LSB	MSB (143H) LSB	MSB (144H) LSB	MSB (145H) LSB	MSB (146H) LSB	MSB (147H) LSB
C13	MSB (130H) LSB	MSB (131H) LSB	MSB (132H) LSB	MSB (133H) LSB	MSB (134H) LSB	MSB (135H) LSB	MSB (136H) LSB	MSB (137H) LSB
C14	MSB (120H) LSB	MSB (121H) LSB	MSB (122H) LSB	MSB (123H) LSB	MSB (124H) LSB	MSB (125H) LSB	MSB (126H) LSB	MSB (127H) LSB
C15	MSB (110H) LSB	MSB (111H) LSB	MSB (112H) LSB	MSB (113H) LSB	MSB (114H) LSB	MSB (115H) LSB	MSB (116H) LSB	MSB (117H) LSB
C16	MSB (100H) LSB	MSB (101H) LSB	MSB (102H) LSB	MSB (103H) LSB	MSB (104H) LSB	MSB (105H) LSB	MSB (106H) LSB	MSB (107H) LSB

In this example, all RAM is constructed like the following.

bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
MSB					LSB

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This catalog provides information as of December, 2000. Specifications and information herein are subject to change without notice.