



LC866560/56B

8-Bit Single Chip Microcontroller with On-Chip 60/56K-Byte ROM, and 1152-Byte RAM

Preliminary

Overview

The LC866560B/56B microcontrollers are 8-bit single chip microcontrollers with the following on-chip functional blocks :

- CPU : Operable at a minimum bus cycle time of 0.5 μ s (microsecond)
- On-chip ROM maximum capacity : 60K bytes
- On-chip RAM capacity : 1152 bytes
- VFD automatic display controller/driver
- 16-bit timer/counter (or two 8-bit timers)
- 16-bit timer/ PWM (or two 8-bit timers)
- 8-channel $\times$ 8-bit AD converter
- Two 8-bit synchronous serial-interface circuits (1-channel $\times$ 16-bit, 1-channel $\times$ 8-bit)
- 14-source 10-vectored interrupt system

All of the above functions are fabricated on a single chip.

Features

(1) Read Only Memory (ROM)	: LC866560B	61440 $\times$ 8 bits
	: LC866556B	57344 $\times$ 8 bits

(2) Random Access Memory (RAM)	:	1152 $\times$ 8 bits
--------------------------------	---	----------------------

- Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.
- SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

(3) Bus Cycle Time/Instruction Cycle Time

The bus cycle time indicates the speed to read ROM.

Bus cycle time	cycle time	Clock divider	System clock oscillation	Oscillation Frequency	Voltage
0.5μs	1.0μs	1/1	Ceramic resonator oscillation	6MHz	4.5 - 6.0V
2 μs	4.0μs	1/2	Ceramic resonator oscillation	3MHz	4.5 - 6.0V
7.5μs	15.0μs	1/2	RC resonator oscillation	800MHZ	4.5 - 6.0V
183μs	366μs	1/2	Crystal oscillation	32.768kHz	4.5 - 6.0V

Note : External resistors (Rf, Rd) are required when X'tal oscillation is used.

(4) Ports

- Input / output ports : 3 ports (16 terminals : port 1,7,8)
Input/output port programmable in a bit
- 15V withstand Input / output ports : 2 ports (16 terminals)
Input/output port programmable nibble unit : 1 port (8 terminals : port 0)
(When the N-channel open drain output is selected, the data in a bit can be inputted.)
Input/output port programmable in a bit : 1 port (8 terminals : port 3)
- Input ports : 2 port (6 terminals : port 7,8)
- VFD output port : 52 terminals
Large current output for digit : 16 terminals
Pull-down resistor option available
- Other function
Input/output port : 2 ports (12 terminals : port F,G)
Input port : 3 ports (24 terminals : port C,D,E)

(5) VFD automatic display controller

- Segment/digit output pattern programmable
Any segment/digit combination available
VFD parallel-drive available
- 16-step dimmer function available

(6) AD converter

- 8 channels × 8-bit AD converters

(7) Serial-interface

- 1-channel × 16-bit serial-interface circuits
- 1-channel × 8-bit serial-interface circuits
- LSB first/MSB first function available
- Internal 8-bit baud-rate generator in common with two serial-interface circuits
- SIO automatic transmission available (2-32byte data can be transmitted with program automatically and continuously).

(8) Timers

- Timer0
16-bit timer / counter
2-bit prescaler + 8-bit programmable prescaler
Mode 0 : Two 8-bit timers with programmable prescaler
Mode 1 : 8-bit timer with a programmable prescaler + 8-bit counter
Mode 2 : 16-bit timer with a programmable prescaler
Mode 3 : 16-bit counter

The resolution of Timer is tCYC. (tCYC : cycle time)

- Timer1
 - 16-bit timer / PWM
 - Mode 0 : Two 8-bit timers
 - Mode 1 : 8-bit timer + 8-bit PWM
 - Mode 2 : 16-bit timer
 - Mode 3 : Variable-bit PWM (9-16 bits)
 - In Mode 0 and Mode 1, the resolution of Timer and PWM is tCYC.
 - In Mode 2 and Mode 3, the resolution of Timer and PWM selectable ; tCYC or 1/2tCYC by program
- Base timer
 - Every 500ms overflow system for a clock application (using 32.768kHz crystal oscillation for Base timer clock)
 - Every 976μs, 3.9ms, 15.6ms, 62.5ms overflow system (using 32.768kHz crystal oscillation for Base timer clock)
 - The Base timer clock selectable ; 32.768kHz crystal oscillation, System clock, and programmable prescaler output of Timer 0

(9) Buzzer output

- The Buzzer sound frequency selectable ; 4KHz, 2KHz (using 32.768kHz crystal oscillation for Base timer clock)

(10) Remote control receiver circuit (Shares with the P73/INT3/T0IN terminal)

- Noise rejection function (the time constant of noise rejection filter : 1 tCYC/16 tCYC/64 tCYC)
(tCYC : instruction cycle time)
- Switch polarity function

(11) Watchdog timer

- The watchdog timer is taken on RC outside
- Watchdog timer operation selectable : interrupt system, system reset

(12) Interrupts system

- 14-sources 10-vectored interrupts :
 1. External interrupt INT0 (include watchdog timer)
 2. External interrupt INT1
 3. External interrupt INT2, timer / counter T0L (Lower 8 bits)
 4. External interrupt INT3, base timer
 5. Timer / counter T0H (Upper 8-bit)
 6. Timer T1L, Timer T1H
 7. Serial interface SIO0
 8. Serial interface SIO1
 9. AD converter
 10. VFD automatic display controller, Port 0
- Built-in interrupt priority control register
 - Microcomputer allows 3 levels of interrupt; low level, high level, and highest level of multiplex interrupt. It can specify a low level or a high level interrupt priority from INT2/T0L through port 0 (i.e. the above interrupt number from three through ten). It can also specify a low level or the highest level interrupt priority to INT0 and INT1.

(13) Sub-routine stack levels

- 128 levels (Max.) : stack area included in RAM area

(14) Multiplication and division

- 16 bits $\times$ 8-bit (7 instruction cycle times)
- 16 bits $\div$ 8-bit (7 instruction cycle times)

(15) Three oscillation circuits

- On-chip RC oscillation circuit using for the system clock
- On-chip CF oscillation circuit using for the system clock
- On-chip crystal oscillation circuit using for the system clock and for time-base clock

Note : External resistors (Rf, Rd) are required

(16) Standby function

- HALT mode function

The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped.

This operation mode can be released by the interrupt request signals or the system reset request signal.

- HOLD Mode function

The HOLD mode is used to freeze all the oscillations ;

RC (internal), CF and Crystal oscillations. This mode can be released by the following operations.

- Reset terminal (RES) set to low level.
- Input a assigned level to P70/INT0/T0IN or P71/INT1/T0IN terminal
- Input a Port0 interrupt condition

(17) Factory shipment

- QFP100E delivery form

(18) Development support tools

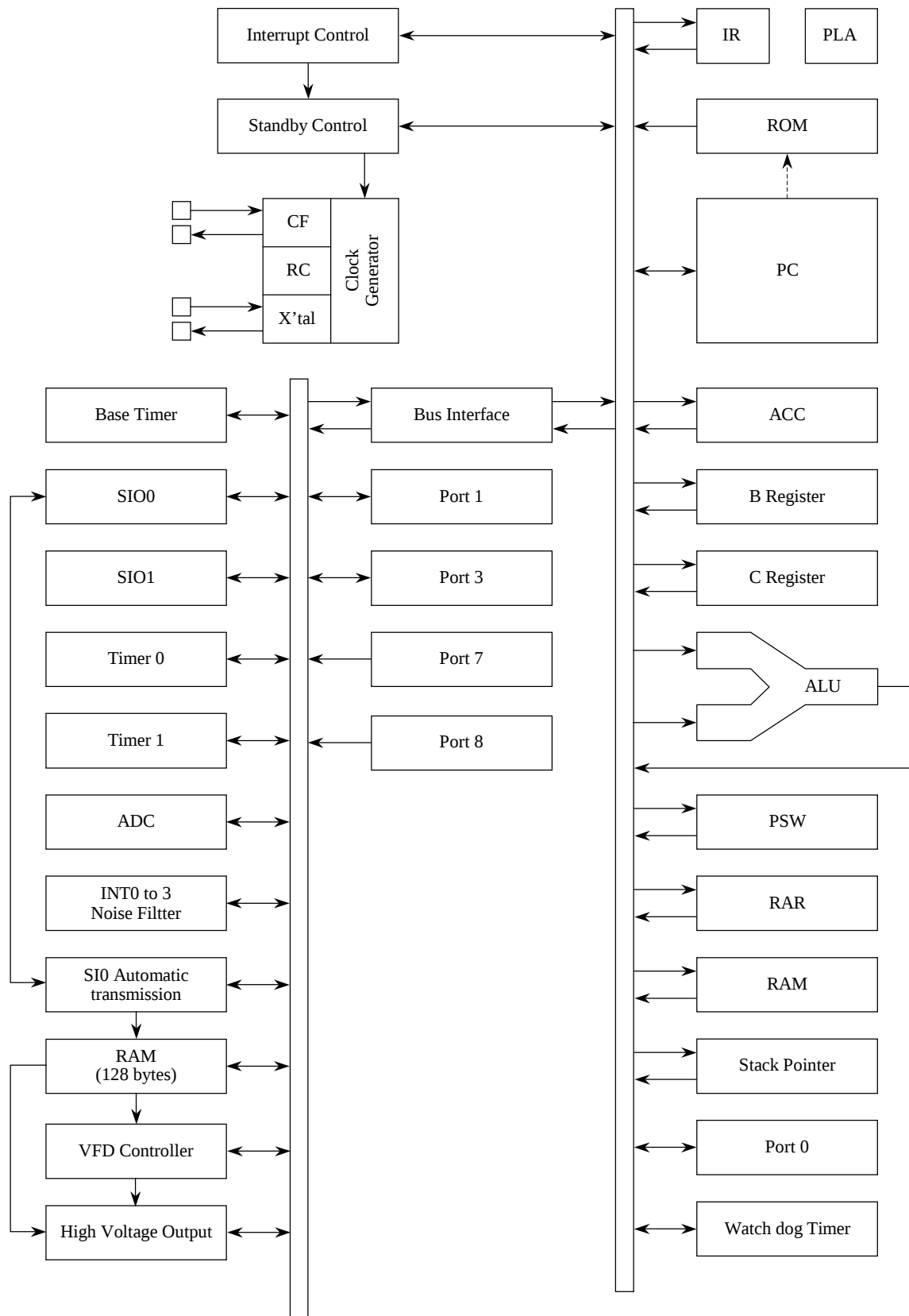
- Evaluation (EVA) chip : LC866094
- EPROM version : LC86E6560
- One time version : LC86P6560
- Emulator : EVA86000 + ECB866500 (Evaluation chip board) + POD866500 (Pod)

• Notes for use

Follow the under table

Frequency range of the system clock	Voltage range	Clock Divider	Note
15kHz to 3MHz	4.5V to 6.0V	1/1	Can not use 1/2 divider
30kHz to 6MHz		1/1, 1/2	
Internal RC oscillation		1/1, 1/2	

System Block Diagram



Pin Description

Pin name	I/O	Function description					Option	
VSS1, 2	-	Power pin (−) *1					-	
VDD1,2,3,4	-	Power pin (+) *1					-	
VP	-	Power pin (+) for the VFD output pull-down resist					-	
PORT0 P00 - P07	I/O	• 8-bit input/output port Input/output in nibble units • Input for port 0 interrupt • Input for HOLD release • 15V withstand at N-channel open drain output					• Pull-up resistor : Provided/Not provided (each nibble) • Output form : CMOS/N-channel open drain (each bit)	
PORT1 P10 - P17	I/O	• 8-bit input/output port Input/output can be specified in bit unit • Other pin functions P10 SIO0 data output P11 SIO0 data input/bus input/output P12 SIO0 clock input/output P13 SIO1 data output P14 SIO1 data input/bus input/output P15 SIO1 clock input/output P16 Buzzer output P17 Timer1 output (PWM0 output)					• Output form : CMOS/N-channel open drain (each bit)	
PORT3 P30 - P37	I/O	• 8-bit input/output port Input/output in bit unit • 15V withstand at N-channel open drain output					• Output form : CMOS/N-channel open drain (each bit)	
PORT7 P70 - P73 P74 - P75	I/O I	• 4-bit input/output port Input/output in bit unit • 2-bit input port • Other pin functions P70 : INT0 input/HOLD release/N-channel Tr. output for watchdog timer P71 : INT1 input/HOLD release input P72 : INT2 input/timer 0 event input P73 : INT3 input with noise filter/timer 0 event input P74 : 32.768kHz crystal oscillation terminal XT1 P75 : 32.768kHz crystal oscillation terminal XT2 • Interrupt received form, vector address					-	
		rising	falling	rising & falling	high level	low level	vector	
		INT0	enable	enable	disable	enable	enable	03H
		INT1	enable	enable	disable	enable	enable	0BH
		INT2	enable	enable	enable	disable	disable	13H
		INT3	enable	enable	enable	disable	disable	1BH

Pin name	I/O	Function description	Option
PORT8 P80 - P83 P84 - P87	I I/O	• 4-bit input/output port Input/output in bit unit • 4-bit input port • Other function AD input port (8 port pins)	-
S0/T0 to S6/T6	O	Output for VFD display controller segment/timing in common	Pull-down resistor : Provided/Not provided (each nibble)
S7/T7 to S15/T15	O	• Output for VFD display controller segment/timing with internal pull-down resistor in common • Internal pull-down resistor output	-
S16 to S31	I/O	• Output for VFD display controller segment • Other function S16 : High voltage input port PC0 S17 : High voltage input port PC1 S18 : High voltage input port PC2 S19 : High voltage input port PC3 S20 : High voltage input port PC4 S21 : High voltage input port PC5 S22 : High voltage input port PC6 S23 : High voltage input port PC7 S24 : High voltage input port PD0 S25 : High voltage input port PD1 S26 : High voltage input port PD2 S27 : High voltage input port PD3 S28 : High voltage input port PD4 S29 : High voltage input port PD5 S30 : High voltage input port PD6 S31 : High voltage input port PD7	Pull-down resistor : Provided/Not provided (each nibble)
S32 to S47	I/O	• Output for VFD display controller segment • Other function S32 : High voltage input port PE0 S33 : High voltage input port PE1 S34 : High voltage input port PE2 S35 : High voltage input port PE3 S36 : High voltage input port PE4 S37 : High voltage input port PE5 S38 : High voltage input port PE6 S39 : High voltage input port PE7 S40 : High voltage I/O port PF0 S41 : High voltage I/O port PF1 S42 : High voltage I/O port PF2 S43 : High voltage I/O port PF3 S44 : High voltage I/O port PF4 S45 : High voltage I/O port PF5 S46 : High voltage I/O port PF6 S47 : High voltage I/O port PF7	Pull-down resistor : Provided/Not provided (each nibble)

Pin name	I/O	Function description	Option
S48 to S51	I/O	- Output for VFD display controller segment - Other function S48 : High voltage I/O port PG0 S49 : High voltage I/O port PG1 S50 : High voltage I/O port PG2 S51 : High voltage I/O port PG3	-
$\overline{\text{RES}}$	I	Reset pin	-
XT1/ $\overline{\text{P74}}$	I	- Input pin for 32.768kHz crystal oscillation - Other function $\overline{\text{P74}}$ for input port In case of non use, connect to VDD1	-
XT2/P75	O	- Output pin for 32.768kHz crystal oscillation - Other function P75 for input port In case of non use, At using as oscillator, should be left opened. At using as a port, connect to VDD1.	-
CF1	I	Input pin for ceramic resonator oscillation	-
CF2	O	Output pin for ceramic resonator oscillation	-

* All of port options (except pull-up resistor of port 0) can be specified in bit unit.

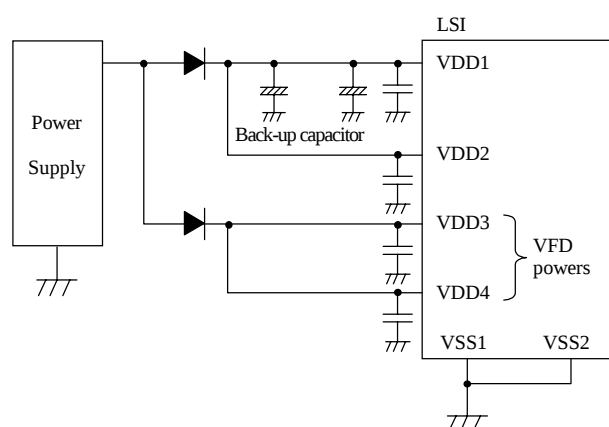
* A state of pins at reset

Pin name	Input/output mode	A state of pull-up resistor specified at pull-up option
Port 0	Input	Fixed pull-up resistor OFF
Ports 1, 3	Input	Programmable pull-up resistor OFF

S0/T0 to S15/T15	P channel Transistor OFF
S16 to S51	P channel Transistor OFF

*1 Connect like the following figure to reduce noise into a VDD1 terminal.

• Shorted the VSS1 terminal to the VSS2 terminal and to make the back-up time long.



1. Absolute Maximum Ratings at VSS1=VSS2=0V and Ta=25°C

Parameter		Symbol	Pins	Conditions	VDD[V]	Ratings			unit
						min.	typ.	max.	
Supply voltage		VDDMAX	VDD1, VDD2 VDD3, VDD4	VDD1=VDD2= VDD3=VDD4		-0.3		+7.0	V
Input voltage		VI(1)	•Ports 74, 75 •Ports 80,81,82,83 •Port 8 •RES			-0.3		VDD+0.3	
		VI(2)	VP			VDD-45		VDD+0.3	
Output voltage		VO	S0/T0 to S15/T15			VDD-45		VDD+0.3	
Input/output voltage		VIO(1)	•Port 1 •Ports 70,71,72,73 •Ports 84,85,86,87 •Ports 0, 3 at CMOS output option			-0.3		VDD+0.3	
		VIO(2)	Ports 0, 3 at N-ch open drain output option			-0.3		15	
		VIO(3)	S16 to S51			VDD-45		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 3	•CMOS output •At each pins		-10			mA
		IOPH(2)	S0/T0 to S15/T15	At each pins		-30			
		IOPH(3)	S16 to S51	At each pins		-15			
	Total output current	ΣIOAH(1)	Port 0	The total of all pins		-30			
		ΣIOAH(2)	Ports 1, 3	The total of all pins		-30			
		ΣIOAH(3)	S0/T0 to S15/T15	The total of all pins		-55			
		ΣIOAH(4)	S16 to S27	The total of all pins		-60			
		ΣIOAH(5)	S28 to S39	The total of all pins		-60			
Low level output current	Peak output current	IOPL(1)	•Ports 0, 1, 3	At each pins				20	
		IOPL(2)	•Ports 70,71,72,73 •Ports 84,85,86,87	At each pins				15	
	Total output current	ΣIOAL(1)	Port 0	The total of all pins				60	
		ΣIOAL(2)	Ports 1, 3, 70	The total of all pins				50	
		ΣIOAL(3)	•Ports 71,72,73 •Ports 84,85,86,87	The total of all pins				20	
	Maximum power dissipation		Pdmax	QFP100E	Ta=-30 to +70°C				500
Operating temperature range		Topr				-30		+70	°C
Storage temperature range		Tstg				-55		+125	

2. Recommended Operating Range at Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings			unit
					min.	typ.	max.	
Operating supply voltage range	VDD	VDD1=VDD2=VDD3=VDD4	$0.98\mu\text{s} \leq t_{CYC} \leq 400\mu\text{s}$		4.5		6.0	V
Hold voltage	VHD	VDD1=VDD2	RAMs and the registers hold voltage at HOLD mode.		2.0		6.0	
Pull-down voltage	VP	VP		4.5-6.0	-35		VDD	
Input high voltage	VIH(1)	Port 0 CMOS output option	Output disable	4.5-6.0	0.33VDD+1.0		VDD	
	VIH(2)	Port 0 at N-ch open drain output	Output disable	4.5-6.0	0.75VDD		13.5	
	VIH(3)	•Port 1 •Ports 72,73 •Port 3 at CMOS output option	Output disable	4.5-6.0	0.75VDD		VDD	
	VIH(4)	•Port 3 at N-ch open drain output	Output disable Tr. OFF	4.5-6.0	0.75VDD		13.5	
	VIH(5)	•Port 70 Port input/interrupt •Port 71 •RES	Output disable	4.5-6.0	0.75VDD		VDD	
	VIH(6)	Port 70 Watchdog timer	Output disable	4.5-6.0	0.9VDD		VDD	
	VIH(7)	•Port 8 •Ports 74,75	Output disable	4.5-6.0	0.75VDD		VDD	
	VIH(8)	S16 to S51	Output P-channel Tr. OFF	4.5-6.0	0.33VDD+1.0		VDD	
Input low voltage	VIL(1)	Port 0 at CMOS output option	Output disable	4.5-6.0	VSS		0.2VDD	
	VIL(2)	Port 0 at N-ch open drain output	Output disable	4.5-6.0	VSS		0.25VDD	
	VIL(3)	•Ports 1,3 •Ports 72,73	Output disable	4.5-6.0	VSS		0.25VDD	
	VIL(4)	•Port 70 Port input/interrupt •Port 71 •RES	Output disable	4.5-6.0	VSS		0.25VDD	
	VIL(5)	Port 70 Watchdog timer	Output disable	4.5-6.0	VSS		0.8VDD-1.0	
	VIL(6)	•Port 8 •Ports 74,75	Output disable	4.5-6.0	VSS		0.25VDD	
	VIL(7)	S16 to S51	Output P-channel Tr. OFF	4.5-6.0	VP		0.2VDD	
Operation cycle time	tCYC			4.5-6.0	0.98		400	μs

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings			unit
					min.	typ.	max.	
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 1	4.5-6.0		6		MHz
	FmCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 1	4.5-6.0		3		
	FmRC		RC oscillation	4.5-6.0	0.3	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 2	4.5-6.0		32.768		kHz
Oscillation stabilizing time period (Note 1)	tmsCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 3	4.5-6.0				ms
	tmsCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 3	4.5-6.0				
	tssXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 3	4.5-6.0				s

(Note 1) The oscillation constant is shown on table 1.

3. Electrical Characteristics at Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings			unit
					min.	typ.	max.	
Input high current	IIH(1)	Port 0,3 of open drain output	•Output disable •VIN=13.5V (including the off-leak current of the output Tr.)	4.5-6.0			5	μ A
	IIH(2)	•Port 0 without pull-up MOS Tr. •Ports 1,3	•Output disable •Pull-up MOS Tr. OFF. VIN=VDD (including the off-leak current of the output Tr.)	4.5-6.0			1	
	IIH(3)	•Ports 70,71,72,73 •Port 8	•Output disable •VIN=VDD (including the off-leak current of the output Tr.)	4.5-6.0			1	
	IIH(4)	$\overline{\text{RES}}$	VIN=VDD	4.5-6.0			1	
	IIH(5)	Ports $\overline{74}$,75	VIN=VDD	4.5-6.0			1	
	IIH(6)	•S16 to S51 without pull-down resistor (Ports C,D,E,F,G)	•Output P-channel Tr. OFF •VIN=VDD	4.5-6.0			1	
Input low current	IIL(1)	•Ports 1,3 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. VIN=VSS (including the off-leak current of the output Tr.)	4.5-6.0	-1			
	IIL(2)	•Ports 70,71,72,73 •Port 8	•Output disable •VIN=VSS (including the off-leak current of the output Tr.)	4.5-6.0	-1			
	IIL(3)	$\overline{\text{RES}}$	VIN=VSS	4.5-6.0	-1			
	IIL(4)	Ports $\overline{74}$,75	VIN=VSS	4.5-6.0	-1			
Output high voltage	VOH(1)	Ports 0,1,3 of CMOS output	IOH=-1.0mA	4.5-6.0	VDD-1			V
	VOH(2)		IOH=-0.1mA	4.5-6.0	VDD-0.5			
	VOH(3)	S0/T0 to S15/T15	IOH=-20mA	4.5-6.0	VDD-1.8			
	VOH(4)		•IOH=-1mA •The current of any unmeasurement pin is not over 1mA.	4.5-6.0	VDD-1			
	VOH(5)	S16 to S51	IOH=-5mA	4.5-6.0	VDD-1.8			
	VOH(6)		The current of any unmeasurement pin is not over 1mA.	4.5-6.0	VDD-1			
Output low voltage	VOL(1)	Ports 0, 1, 3	IOL=10mA	4.5-6.0			1.5	
	VOL(2)		IOL=1.6mA	4.5-6.0			0.4	
	VOL(3)	Port 70	IOL=1mA	4.5-6.0			0.4	
	VOL(4)	•Ports 71,72,73 •Ports 84,85,86,87	IOL=1.6mA	4.5-6.0			0.4	
Pull-up MOS Tr. resistor	Rpu	•Ports 0, 1, 3	VOH=0.9VDD	4.5-6.0	15	40	70	k Ω

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings			unit
					min.	typ.	max.	
Output off-leak current	IOFF(1)	S0/T0 to S6/T6, S16 to S51 without pull-down resistor	•Output P-ch Tr. OFF •VOUT=VSS	4.5-6.0	-1			μ A
	IOFF(2)		•Output P-ch Tr. OFF •VOUT=VDD-40V	4.5-6.0	-30			
Resistance of the low level hold Tr.	Rinpd	S16 to S51	•Output P-ch Tr. OFF •Using as input ports	4.5-6.0		200		k Ω
High voltage pull-down resistor	Rpd	S0/T0 to S15/T15, S16 to S51 with pull-down resistor	•Output P-ch Tr. OFF •VOUT=3V •Vp=-30V	5.0	60	100	200	
VP pull-down resistor	Rvppd	Vp	•VSS=GND •Vp=-30V	5.0	60	100	200	
Hysteresis voltage	VHIS	•Port 1 •Ports 70,71,72,73,75 •RES	Output disable	4.5-6.0		0.1VDD		V
Pin capacitance	CP	All pins	•f=1MHz •Unmeasurement terminals for the input are set to VSS level. •Ta=25°C	4.5-6.0		10		pF

4. Serial Input/Output Characteristics at Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Ratings			unit
							min.	typ.	max.	
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to figure 5.	4.5-6.0	2			tCYC
		Low Level pulse width	tCKL(1)				1			
		High Level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	•Use pull-up resistor (1kΩ) when opendrain output. •Refer to figure 5.	4.5-6.0	2			
		Low Level pulse width	tCKL(2)					1/2 tCKCY		
		High Level pulse width	tCKH(2)					1/2 tCKCY		
Serial input	Data set up time		tICK	•SI0,SI1 •SB0,SB1	•Data set-up to SCK0,1 •Data hold from SCK0,1 •Refer to figure 5.	4.5-6.0	0.1			μs
	Data hold time						tCKI	0.1		
Serial output	Output delay time (Serial clock is external clock)		tCKO(1)	•SO0,SO1 •SB0,SB1	•Use pull-up resistor (1kΩ) when open drain output. •Data hold from SCK0,1 •Refer to figure 5.	4.5-6.0			7/12 tCYC +0.2	
	Output delay time (Serial clock is internal clock)		tCKO(2)						1/3 tCYC +0.2	

5. Pulse Input Conditions at Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings			unit
					min.	typ.	max.	
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	4.5-6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock is selected to 1/1.)	•Interrupt acceptable •Timer0-countable	4.5-6.0	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock is selected to 1/16.)	•Interrupt acceptable •Timer0-countable	4.5-6.0	32			
	tPIH(4) tPIL(4)	INT3/T0IN (The noise rejection clock is selected to 1/64.)	•Interrupt acceptable •Timer0-countable	4.5-6.0	128			
	tPIL(5)	$\overline{\text{RES}}$	Reset acceptable	4.5-6.0	200			μs

6. AD Converter Characteristics at Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings			unit
					min.	typ.	max.	
Resolution	N			4.5-6.0		8		bit
Absolute precision (Note 2)	ET			4.5-6.0			±1.5	LSB
Conversion time	tCAD		AD conversion time = 16 × tCYC (ADCR2=0) (Note 3)	4.5-6.0	15.68 (tCYC=0.98μs)		65.28 (tCYC=4.08μs)	μs
			AD conversion time = 32 × tCYC (ADCR2=1) (Note 3)		31.36 (tCYC=0.98μs)		130.56 (tCYC=4.08μs)	
Analog input voltage range	VAIN	AN0 - AN7		4.5-6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5-6.0			1	μA
	IAINL		VAIN=VSS	4.5-6.0	-1			

(Note 2) Absolute precision excepts quantizing error (±1/2 LSB).

(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

7. Current Dissipation Characteristics at Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings			unit
					min.	typ.	max.	
Current dissipation during basic operation (Note 4)	IDDOP(1)		•FmCF=6MHz Ceramic resonator oscillation •Internal RC oscillation stops •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •1/1 divided	4.5-6.0		10	25	mA
	IDDOP(2)		•FmCF=3MHz Ceramic resonator oscillation •Internal RC oscillation stops •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •1/2 divided	4.5-6.0		3	9	
	IDDOP(3)		•FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation •1/2 divided	4.5-6.0		0.7	3.4	
	IDDOP(4)		•FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : crystal oscillation •Internal RC oscillation stops •1/2 divided	4.5-6.0		35	130	μA

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings			unit
					min.	typ.	max.	
Current dissipation in HALT mode (Note 4)	IDDHALT(1)		•HALT mode •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •Internal RC oscillation stops •System clock : CF oscillation •1/1 divided	4.5-6.0		5	14	mA
	IDDHALT(2)		•HALT mode •FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •Internal RC oscillation stops •System clock : CF oscillation •1/2 divided	4.5-6.0		2.2	7	
	IDDHALT(3)		•HALT mode FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation •1/2 divided	4.5-6.0		400	1600	μA
	IDDHALT(4)		•HALT mode FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : crystal oscillation •Internal RC oscillation stops •1/2 divided	4.5-6.0		25	100	
Current dissipation in HOLD mode (Note 4)	IDDHOLD		HOLD mode	4.5-6.0		0.05	30	

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation recommended constant (main clock)

Oscillation type	Maker	Oscillator	C1	C2
6MHz ceramic resonator oscillation	Murata	CSA6.00MG		
		CST6.00MGW		
	Kyocera	KBR-6.0MSB		
		PBRC6.00A (chip type)		
		KBR-6.0MKC		
		PBRC6.00B (chip type)		
3MHz ceramic resonator oscillation	Murata	CSA3.00MG		
		CST3.00MGW		
	Kyocera	KBR-3.0MS		

* Both C1 and C2 must use K rank ($\pm 10\%$) and SL characteristics.

Table 2. Crystal oscillation guaranteed constant (sub clock)

Oscillation type	Maker	Oscillator	C3	C4	Rf	Rd
32.768kHz crystal oscillation	EPSON	C-002RX				
	CITIZEN	CFS-308				
		CFS-206				

* Both C3 and C4 must use J rank ($\pm 5\%$) and CH characteristics.

(It is about the application which is not in need of high precision. Use K rank ($\pm 10\%$) and SL characteristics.)

- (Notes)
- Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
 - If you use other oscillators herein, we provide no guarantee for the characteristics.

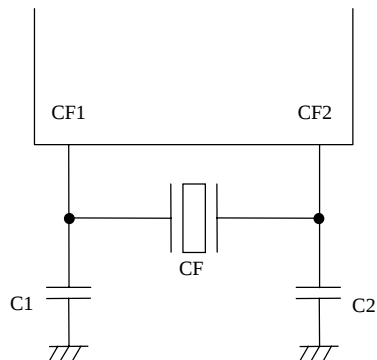


Figure 1 Ceramic oscillation circuit

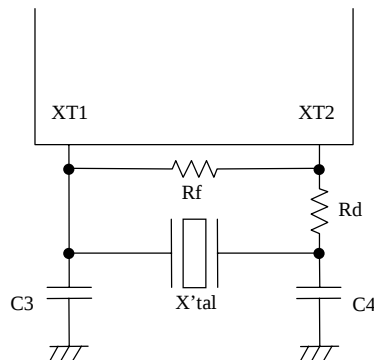


Figure 2 Crystal oscillation circuit

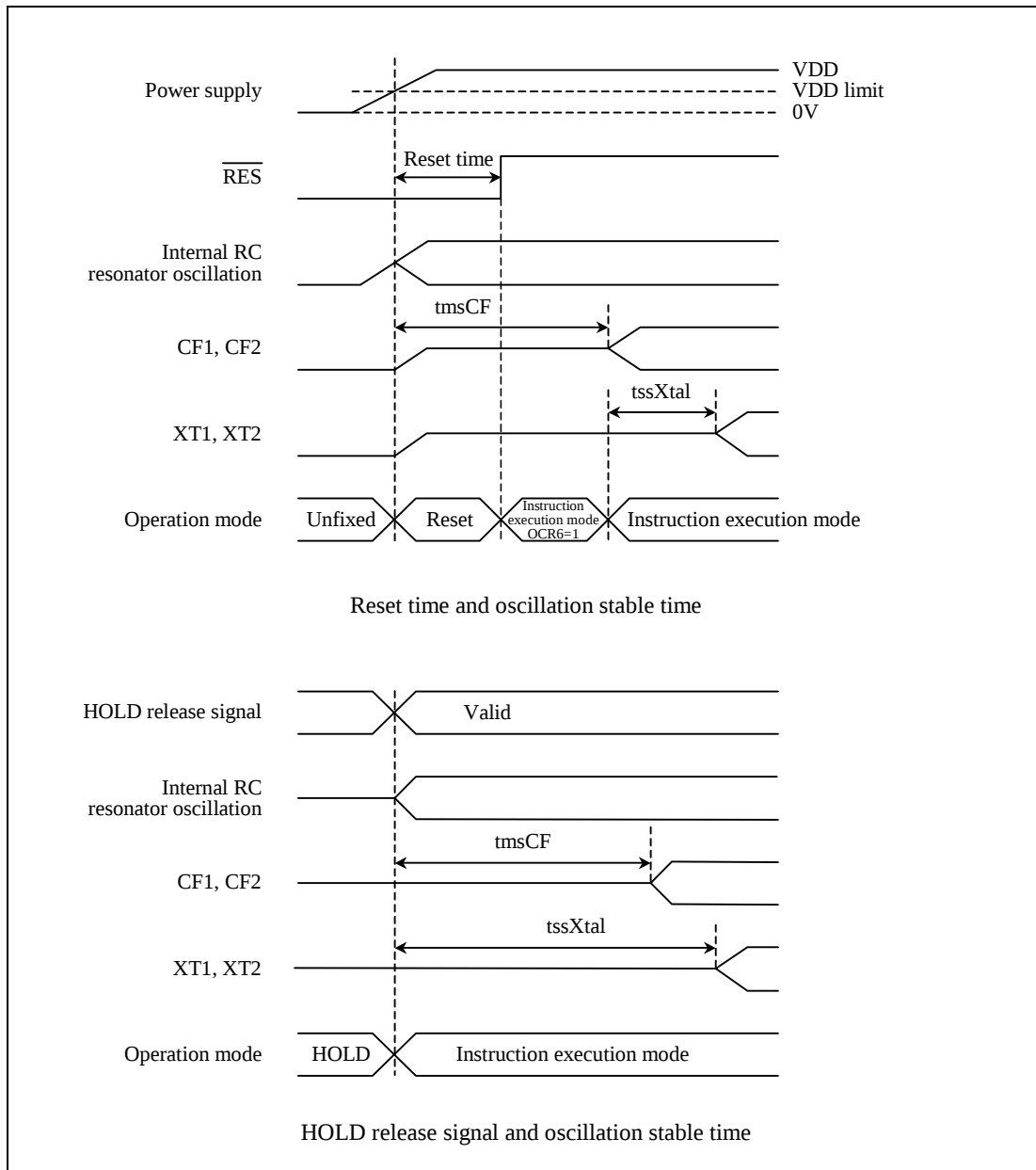
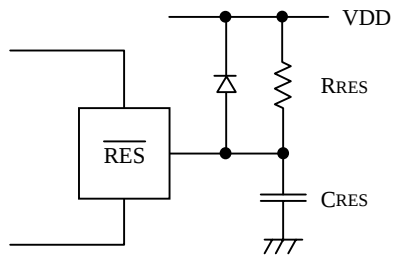


Figure 3 Oscillation stable time



(Note) Fix the value of CRES, RRES that is sure to reset until 200 μ s, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit

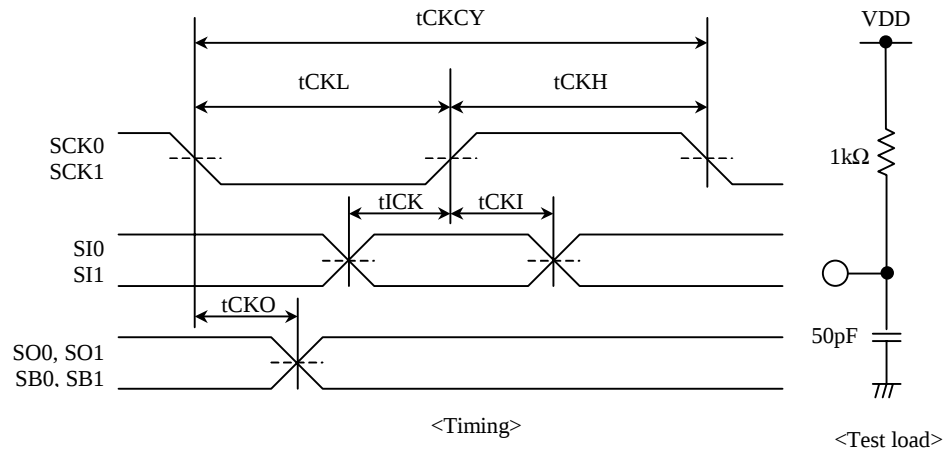
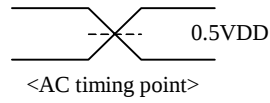


Figure 5 Serial input / output test condition

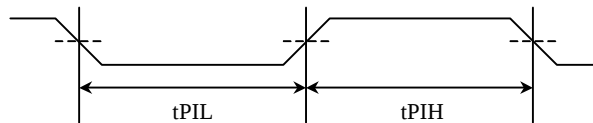


Figure 6 Pulse input timing condition

- Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of September, 2000. Specifications and information herein are subject to change without notice.