



LC866032B/28B/24B

8-Bit Single Chip Microcontroller On-Chip 32/28/24K-Byte ROM and On-Chip 512-Byte

Preliminary

Overview

The LC866032B / 28B / 24B microcontroller are 8-bit single chip microcontroller with the following on-chip functional blocks:

- CPU : Operable at a minimum bus cycle time of 0.5μs (microsecond)
- On-chip ROM Maximum Capacity : 32K bytes
- On-chip RAM Capacity : 512 bytes
- VFD automatic display controller / driver
- 16-bit timer / counter
- 16-bit timer / PWM
- 4 channel 8-bit AD converter
- Two 8-bit synchronous serial-interface circuits
- 14-source 10-level vectored interrupt system

All of the above functions are fabricated on a single chip.

Feature

- | | |
|--------------------------------------|---|
| (1) Read-Only Memory (ROM) : | LC866032B 32512×8 bits
LC866028B 28672×8 bits
LC866024B 24576×8 bits |
| (2) Random Access Memory (RAM) : | LC866032B / 28B / 24B 512×8 bits |
| (3) Minimum bus cycle time : | 0.5μs (using 12MHz CF resonator oscillation)
Bus cycle time means ROM-read period. |
| (4) Minimum instruction cycle time : | 1μs (using 12MHz CF resonator oscillation)
ROM data is accessed twice in a instruction cycle time.
The operation of the microcomputers herein is about 1.7 times that of LC66000 series, our products in the same specified cycle time. |

Bus cycle time	Cycle time	System clock oscillation	Frequency	Voltage
0.5μs	1μs	Ceramic (CF) oscillation	12MHz	4.5 to 6.0V
2μs	4μs	Ceramic (CF) oscillation	3MHz	2.5 to 6.0V
7.5μs	15μs	Internal RC oscillation	800kHz	2.5 to 6.0V
183μs	366μs	Crystal (X'tal) oscillation	32.768kHz	2.5 to 6.0V

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- (5) Ports :
 - Input / output ports : 2 ports (16 terminals)
 - Input / output port programmable in nibble units : 1 port (8 terminals)
 - Input / output port programmable in a bit : 1 port (8 terminals)
 - Input ports : 2 ports (8 terminals)
 - VFD output ports : 30 terminals
 - Large current output for digit : 16 terminals
 - Pull-down resistor option available
- (6) VFD automatic display controller
 - Segment / digit output pattern programmable
 - Any segment / digit combination available.
 - VFD parallel-drive available
 - 16-step dimmer function available
- (7) AD converter
 - 4-channel 8-bit AD converter
- (8) Serial-interface
 - Two 8-bit serial-interfaces
 - LSB first / MSB first function available
 - Internal 8-bit baud-rate generator in common with two serial-interface circuits
- (9) Timer
 - Timer 0
 - 16-bit timer / counter
 - 2-bit prescaler + 8-bit programmable prescaler
 - Mode 0 : Two 8-bit timers with programmable prescaler
 - Mode 1 : 8-bit timer with programmable prescaler + 8-bit counter
 - Mode 2 : 16-bit timer with programmable prescaler
 - Mode 3 : 16-bit counter
 - Resolution of Timer is tCYC. (tCYC : cycle time)
 - Timer 1
 - 16-bit timer / PWM
 - Mode 0 : Two 8-bit timers
 - Mode 1 : 8-bit timer + 8-bit PWM
 - Mode 2 : 16-bit timer
 - Mode 3 : Variable-bit PWM (9 to 16 bits)
 - In Mode 0 and Mode1, resolution of Timer and PWM is tCYC.
 - In Mode 2 and Mode 3, resolution of Timer and PWM selectable : tCYC or 1 / 2 tCYC by program
 - Base timer
 - Every 500ms overflow system for a clock application (using 32.768kHz crystal oscillation for Base timer clock)
 - Every 976μs, 3.9ms, 15.6ms, 62.5ms overflow system (using 32.768kHz crystal oscillation for Base timer clock)
 - The Base timer clock selectable; 32.768kHz crystal oscillation, System clock, and
 - Programmable prescaler output of Timer 0
- (10) Buzzer output
 - The Buzzer sound frequency selectable; 4kHz, 2kHz (using 32.768kHz crystal oscillation for timer clock)
- (11) Remote-control receiver (using P73 / INT3 / T0IN terminals)
 - Noise rejection available
 - The interrupt polarity selectable
- (12) Watchdog timer
 - The watchdog timer is taken on RC outside
 - Watchdog timer operation selectable : interrupt system, system reset.

(13) Interrupt system

- 14-source 10-level vectored interrupts :

1. External interrupt INT0 (includes watchdog timer)
2. External interrupt INT1
3. External interrupt INT2, timer / counter T0L (lower 8-bit)
4. External interrupt INT3, base timer
5. Timer / counter T0H (upper 8-bit)
6. Timer T1L, timer T1H
7. Serial-interface SIO0
8. Serial-interface SIO1
9. AD converter
10. VFD display controller, port 0

- Interrupt Priority control available

Interrupt Priority control register included.

These microcomputers are available to 3-level interrupt : low-level, high-level and highest-level of multiplex interrupt. It can specify a low level or a high-level interrupt priority from INT2 / T0L through VFD display controller / port 0 (the above interrupt number from 3 to 10).

It can also specify a low-level or the highest-level interrupt priority to INT0 and INT1.

(14) Real-time service operation

The Real-Time Service (RTS) functions the data-transfer between the Special Function Registers at acknowledging the interrupt request.

The RTS starts within 1 cycle-time and completes within 5 cycle-times after occurring the interrupt request.

(15) Sub-routine stack levels

- 128 levels (Max.) : Stack area included in the RAM area.

(16) Multiplication and division

16-bit $\times$ 8-bit (7 instruction cycle-times)

16-bit / 8-bit (7 instruction cycle-times)

(17) 3 oscillation circuits

- On-chip RC oscillation circuit using for the system clock
- On-chip CF oscillation circuit using for the system clock
- On-chip crystal oscillation circuit using for the system clock and for time-base clock

(18) Standby function

- HALT mode function

The HALT mode is used to reduce power dissipation. In this operation mode, program execution is stopped.

This operation mode can be released by interrupt request signals or the system reset.

- HOLD mode function

The HOLD mode is used to freeze all the oscillations ;

RC (internal), CF and Crystal oscillations. This mode can be released by the following operations.

- Reset terminal ($\overline{\text{RES}}$) set to Low level
- P70 / INT0, P71 / INT1 terminals set to assigned level (programmable)
- Port 0 terminal / terminals set to Low level (programmable)

(19) Factory shipment

DIP 64S delivery form

QIP 64E delivery form

(20) Development support tools

Evaluation (EVA) chip : LC866099

EPROM version : LC86E6032

One time version : LC86P6032

Emulator : EVA-86000 + ECB866000 (Evaluation chip board)
+ POD866000 (POD)

Pin Assignment

•DIP64S

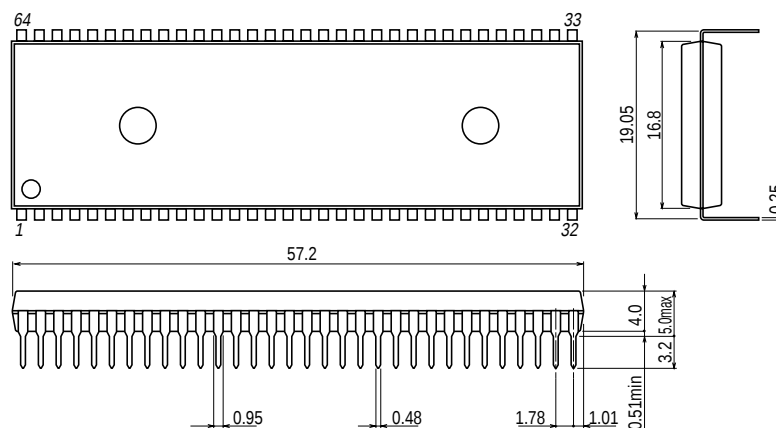
P10 / SO0	1	64	P07
P11 / SI0 / SB0	2	63	P06
P12 / SCK0	3	62	P05
P13 / SO1	4	61	P04
P14 / SI1 / SB1	5	60	P03
P15 / SCK1	6	59	P02
P16 / BUZ	7	58	P01
P17 / PWM	8	57	P00
TEST1	9	56	S29
$\overline{\text{RES}}$	10	55	S28
XT1	11	54	S27
XT2	12	53	S26
VSS	13	52	S25
CF1	14	51	S24
CF2	15	50	S23
VDD	16	49	S22
P80 / AN0	17	48	S21
P81 / AN1	18	47	S20
P82 / AN2	19	46	S19
P83 / AN3	20	45	S18
P70 / INT0	21	44	S17
P71 / INT1	22	43	S16
P72 / INT2 / TOIN	23	42	VP
P73 / INT3 / TOIN	24	41	VDDVPP
S0 / T0	25	40	S15 / T15
S1 / T1	26	39	S14 / T14
S2 / T2	27	38	S13 / T13
S3 / T3	28	37	S12 / T12
S4 / T4	29	36	S11 / T11
S5 / T5	30	35	P10 / T10
S6 / T6	31	34	S9 / T9
S7 / T7	32	33	P8 / T8

ILC00164

Package Dimensions

unit : mm

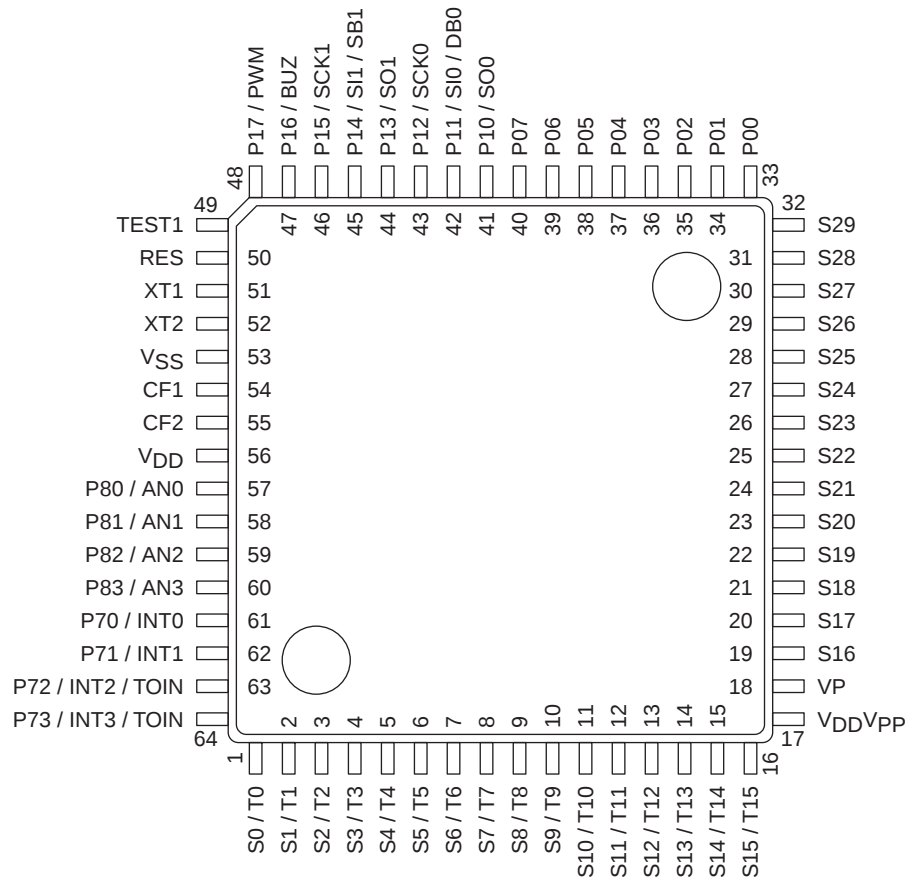
3071



SANYO : DIP64S

Pin Assignment

•QIP64E

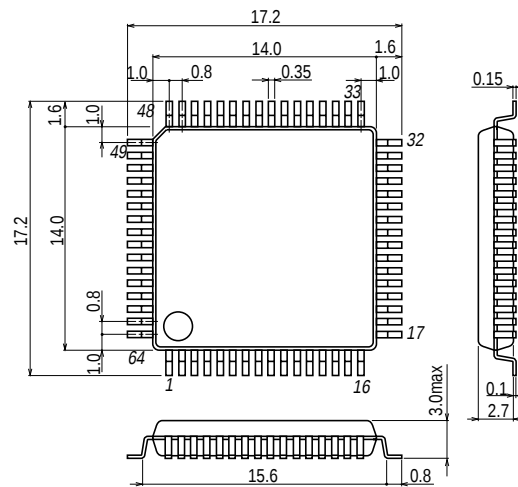


ILC00165

Package Dimensions

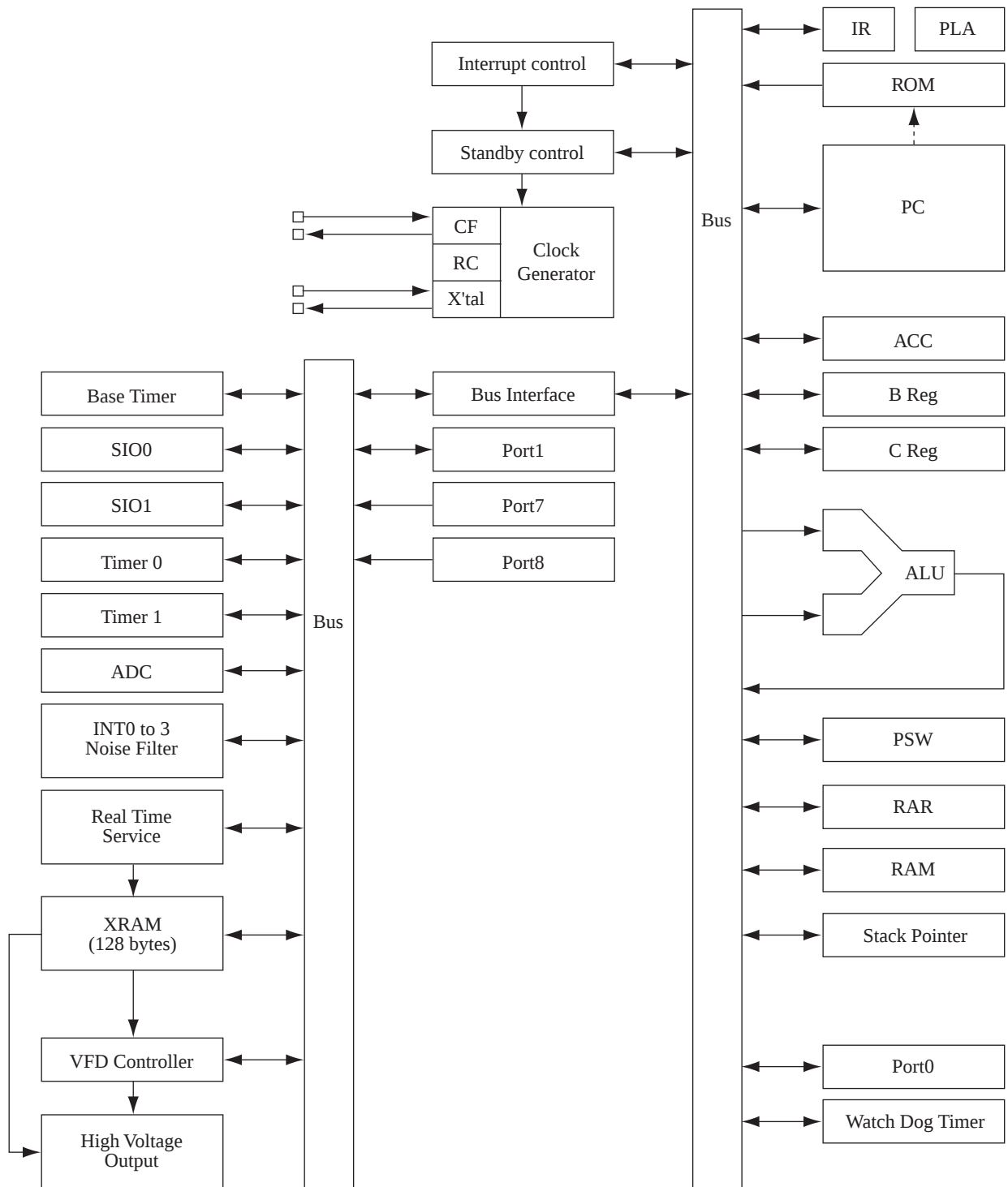
unit : mm

3159



SANYO : QIP64E

System Block Diagram



ILC00166

LC866032B/28B/24B Pin description

Pin name	I / O	Function description	Option																																			
VSS		Power pin (-)																																				
VDD		Power pin (+)																																				
VP		Power pin (-) for VFD output pull-down resistor																																				
VDDVPP		Power pin (+)																																				
PORT0 P00 to P07	I / O	•8-bit input / output port •Input for port 0 interrupt •Input / output in nibble units •Input for HOLD release	•Pull-up resistor : Provided / Not provided •Output form : CMOS / N-channel open drain																																			
PORT1 P10 to P17	I / O	•8-bit input / output port •Input / output can be specified in bit unit. •Other pin functions P10 : SIO0 data output P11 : SIO0 data input / bus input / output P12 : SIO0 clock input / output P13 : SIO1 data output P14 : SIO1 data input / bus input / output P15 : SIO1 clock input / output P16 : Buzzer output P17 : Timer 1 output (PWM output)	Output form : CMOS / N-channel open drain																																			
PORT7 P70 P71 to P73	I / O I	•4-bit input port •Other pin functions P70 : INT0 input / HOLD release / N-channel Tr. output for watchdog timer P71 : INT 1 input / HOLD release P72 : INT 2 input / timer 0 event input P73 : INT 3 input with noise filter / timer 0 event input •Interrupt received form, vector address.	Pull-up resistor : Provided / Not provided																																			
		<table><tr><td></td><td>Leading</td><td>Trailing</td><td>Leading & Trailing</td><td>HIGH Level</td><td>LOW Level</td><td>VECTOR</td></tr><tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr><tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr><tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr><tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr></table>		Leading	Trailing	Leading & Trailing	HIGH Level	LOW Level	VECTOR	INT0	enable	enable	disable	enable	enable	03H	INT1	enable	enable	disable	enable	enable	0BH	INT2	enable	enable	enable	disable	disable	13H	INT3	enable	enable	enable	disable	disable	1BH	
	Leading	Trailing	Leading & Trailing	HIGH Level	LOW Level	VECTOR																																
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INT2	enable	enable	enable	disable	disable	13H																																
INT3	enable	enable	enable	disable	disable	1BH																																
PORT8 P80 to P87	I	•4-bit input port •Other functions AD input port (4 port pins)																																				
S0 / T0 to S6 / T6	O	Output for VFD display controller segment / timing in common	Pull-down resistor : Provided / Not provided (Usable for static output port at pull-down resistor Not provided.)																																			
S7 / T7 to S15 / T15	O	Output for VFD display controller segment / timing with internal pull-down resistor in common																																				

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Pin name	I / O	Function description	Option
S16 to S29	O	Output for VFD display controller segment	Pull-down resistor : Provided / Not provided. (Usable for static output port at pull-down register Not provided.)
RES	I	Reset pin with pull-up resistor	
TEST1	O	•Test pin •Should be left unconnected.	
XT1	I	Input pin for 32.768kHz crystal oscillation In case of non use, connect to VDD.	
XT2	O	Output pin for 32.768kHz crystal oscillation In case of non use, should be left unconnected.	
CF1	I	Input pin for ceramic resonator oscillation	
CF2	O	Output pin for ceramic resonator oscillation	

*All of port options can be specified in bit unit.

*A state of pins at reset.

Pin name	Input / output mode	A state of pull-up resistor specified at pull-up option
Ports 0, 7	Input	Fixed pull-up resistor exist
Port 1	Input	Programmable pull-up resistor OFF

Pin name	A state of P-channel transistor
S0 / T0 to S15 / T15	P-channel transistor OFF
S16 to S29	P-channel transistor OFF

LC866032B/28B/24B

1. Absolute Maximum Ratings at V_{SS}=0V and Ta=25°C

Parameter		Symbol	Pins	Conditions	VDD[V]	Ratings			unit
						min.	typ.	max.	
Supply voltage		VDD MAX	VDD, VDDVPP	VDD=VDDVPP		-0.3		+7.0	V
Input voltage		VI(1)	•Ports 71, 72, 73 •Port 8 •RES			-0.3		VDD + 0.3	
		VI(2)	Vp			VDD-45		VDD + 0.3	
Output voltage		VO	•S0 / T0 to S15 / T15 •S16 to S29			VDD-45		VDD + 0.3	
Input / output voltage		VIO	Ports 0, 1, 70			-0.3		VDD + 0.3	
High Level output current	Peak output current	IOPH(1)	Ports 0, 1	•CMOS output •At each pins		-4			mA
		IOPH(2)	S0 / T0 to S15 / T15	At each pins		-30			
		IOPH(3)	S16 to S29	At each pins		-15			
	Total output current	ΣIOAH(1)	Port 0	The total all pins		-10			
		ΣIOAH(2)	Port 1	The total all pins		-10			
		ΣIOAH(3)	•S0 / T0 to S15 / T15 •S16 to S29	The total all pins		-130			
Low Level output current	Peak output current	IOPL(1)	Ports 0, 1	At each pins				20	
		IOPL(2)	Port 70	At each pins				15	
	Total output current	ΣIOAL(1)	Port 0	The total all pins				40	
		ΣIOAL(2)	Ports 1, 70	The total all pins				40	
Power dissipation (max.)		Pdmax(1)	DIP64S	Ta= -30 to +70°C				760	mW
		Pdmax(2)	QIP64E	Ta= -30 to +70°C				430	
Operating temperature range		Topg				-30		70	°C
Storage temperature range		Tstg				-65		150	°C

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2. Recommended Operating Range at Ta= -30°C to +70°C, VSS= 0V

Parameter	Symbol	Pins	Conditions	Ratings				unit
				VDD [V]	min.	typ.	max.	
Operating supply voltage range	VDD(1)	VDD	$0.98\mu s \leq t_{CYC}$ $t_{CYC} \leq 400\mu s$		4.5		6.0	V
	VDD(2)		$3.9\mu s \leq t_{CYC}$ $t_{CYC} \leq 400\mu s$		2.5		6.0	
HOLD voltage	VHD	VDD	RAMs and Registers hold voltage at HOLD mode.		2.0		6.0	
Pull-down voltage	Vp	Vp		2.5 to 6.0	−35		VDD	
Input high voltage	VIH(1)	Port 0 (Schmitt)	Output disable	2.5 to 6.0	$0.4V_{DD} + 0.9$		VDD	
	VIH(2)	•Port 1 •Ports 72, 73 (Schmitt)	Output disable	2.5 to 6.0	$0.75V_{DD}$		VDD	
	VIH(3)	•Port 70 port input / interrupt •Port 71 • $\overline{RES}$ (Schmitt)	Output N-channel Tr. OFF	2.5 to 6.0	$0.75V_{DD}$		VDD	
	VIH(4)	Port 70 Watchdog timer input	Output N-channel Tr. OFF	2.5 to 6.0	$0.9V_{DD}$		VDD	
	VIH(5)	Port 8		2.5 to 6.0	$0.75V_{DD}$		VDD	
Input low voltage	VIL(1)	Port 0 (Schmitt)	Output disable	2.5 to 6.0	VSS		$0.2V_{DD}$	
	VIL(2)	•Port 1 •Ports 72, 73 (Schmitt)	Output disable	2.5 to 6.0	VSS		$0.25V_{DD}$	
	VIL(3)	•Port 70 Port input / interrupt •Port 71 • $\overline{RES}$ (Schmitt)	N-channel Tr. OFF	2.5 to 6.0	VSS		$0.25V_{DD}$	
	VIL(4)	Port 70 Watchdog timer.	N-channel Tr. OFF	2.5 to 6.0	VSS		$0.8V_{DD} - 1.0$	
	VIL(5)	Port 8		2.5 to 6.0	VSS		$0.25V_{DD}$	
Operation cycle time	tCYC			4.5 to 6.0	0.98		400	μs
				2.5 to 6.0	3.9		400	

Parameter	Symbol	Pins	Conditions	VDD [V]	Ratings			unit
					min.	typ.	max.	
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•12MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0	11.76	12	12.24	MHz
	FmCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 1	2.5 to 6.0	2.94	3	3.06	
	FmRC		RC oscillation	2.5 to 6.0	0.4	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 2	2.5 to 6.0		32.768		kHz
Oscillation stable time period (Note 1)	tmsCF(1)	CF1,CF2	•12MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0		0.02	0.2	ms
	tmsCF(2)	CF1,CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0		0.1	1	
				2.5 to 6.0		0.1	3	
	tssXtal	XT1,XT2	•32.768kHz (crystal oscillation) •Refer to figure 3	4.5 to 6.0		1	1.5	s
				2.5 to 6.0		1	3	

(Note 1) The oscillation constant is shown on table 1 and table 2.

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3. Electrical Characteristics at Ta= -30°C to +70°C, VSS= 0V

Parameter	Symbol	Pins	Conditions	VDD [V]	Ratings			unit
					min.	typ.	max.	
Input high current	I _{IH} (1)	•Port •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. V _{IN} =V _{DD} (including off-leak current of output Tr.)	2.5 to 6.0			1	μA
	I _{IH} (2)	•Port 7 without pull-up MOS Tr. •Port 8	V _{IN} =V _{DD}	2.5 to 6.0			1	
	I _{IH} (3)	RES	V _{IN} =V _{DD}	2.5 to 6.0			1	
Input low current	I _{IL} (1)	•Port 1 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. V _{IN} =V _{SS} (including off-leak current of output Tr.)	2.5 to 6.0	-1			
	I _{IL} (2)	•Port 7 without pull-up MOS Tr. •Port 8	V _{IN} =V _{SS}	2.5 to 6.0	-1			
	I _{IL} (3)	RES	V _{IN} =V _{SS}	2.5 to 6.0	-1			
Output high voltage	V _{OH} (1)	CMOS output of ports 0,1 S0 / T0 to S15 / T15	I _{OH} = -1.0mA	4.5 to 6.0	V _{DD} -1			V
	V _{OH} (2)		I _{OH} = -0.1mA	2.5 to 6.0	V _{DD} -0.5			
	V _{OH} (3)		I _{OH} = -20mA	4.5 to 6.0	V _{DD} -1.8			
	V _{OH} (4)	S16 to S29	•I _{OH} = -1.0mA •The current of any unmeasurement pin is not over 1mA.	2.5 to 6.0	V _{DD} -1			
	V _{OH} (5)		I _{OH} = -5mA	4.5 to 6.0	V _{DD} -1.8			
	V _{OH} (6)		•I _{OH} = -1.0mA •The current of any unmeasurement pin is not over 1mA.	2.5 to 6.0	V _{DD} -1			
Output low voltage	V _{OL} (1)	Ports 0, 1	I _{OL} =10mA	4.5 to 6.0			1.5	
	V _{OL} (2)		•I _{OL} =1.6mA •The total current of port 0, 1 is not over 40mA.	4.5 to 6.0			0.4	
	V _{OL} (3)		•I _{OL} = -1mA •The current of any unmeasurement pin is not over 1mA.	2.5 to 6.0			0.4	
	V _{OL} (4)	Port 70	I _{OL} =1mA	4.5 to 6.0			0.4	
	V _{OL} (5)		I _{OL} =0.5mA	2.5 to 6.0			0.4	
Pull-up MOS Tr. resistor	R _{pu}	•Ports 0, 1 •Port 7	V _{OH} =0.9V _{DD}	4.5 to 6.0	15	40	70	kΩ
			V _{OH} =0.9V _{DD}	2.5 to 4.5	25	60	120	

Parameter	Symbol	Pins	Conditions	VDD [V]	Ratings			unit
					min.	typ.	max.	
Output offleakage current	I _{OFF} (1)	•S0 / T0 to S6 / T6 •S24 to S29 (Without pull-down resistor.)	•Output P-channel Tr. OFF. •V _{OUT} =V _{SS}	2.5 to 6.0	-1			μA
	I _{OFF} (2)		•Output P-channel Tr. OFF. •V _{OUT} =V _{DD} -40V	2.5 to 6.0	-30			
Pull-down transistor resistor	R _{pd}	•S7 / T7 to S15 / T15 •S16 to S23 (With pull-down resistor.)	•Output P-channel Tr. OFF. •V _{OUT} =3V •V _p = -30V	5.0	60	100	200	kΩ
Hysteresis voltage	V _{HIS}	•Ports 0, 1 •Port 7 • $\overline{\text{RES}}$	Output disable	2.5 to 6.0		0.1V _{DD}		V
Pin capacitance	C _P	All pins	•f=1MHz •Unmeasurement terminals for input are set to V _{SS} level. •T _a =25°C	2.5 to 6.0		10		pF

4. Serial Input / Output Characteristics at Ta= -30°C to +70°C, VSS= 0V

Parameter		Symbol	Pins	Conditions	VDD [V]	Ratings			unit		
						min.	typ.	max.			
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to figure 5	2.5 to 6.0	2		tCYC		
		Low level pulse width				tCKL(1)	2.5 to 6.0	1			
		High level pulse width					tCKH(1)	2.5 to 6.0		1	
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	•Use pull-up resistor (1kΩ) when open drain output. •Refer to figure 5	2.5 to 6.0	2				
		Low level pulse width				tCKL(2)	2.5 to 6.0			1 / 2tCKCY	
		High level pulse width					tCKH(2)	2.5 to 6.0			1 / 2tCKCY
Serial input	Data set up time	tICK	•SI0, SI1 •SB0, SB1	•Data set-up to SCK0, 1 •Data hold from SCK0, 1 •Refer to figure 5	4.5 to 6.0	0.1		μs			
					2.5 to 6.0	0.4					
	Data hold time	tCKI			4.5 to 6.0	0.1					
					2.5 to 6.0	0.4					
Serial output	Output delay time (Serial clock is extrnal clock)	tCKO(1)	•SO0, SO1 •SB0, SB1	•Use pull-up resistor (1kΩ) when open drain output.	4.5 to 6.0			7 / 12tCYC +0.2			
					2.5 to 6.0			7 / 12tCYC +1			
	Output delay time (Serial clock is internal clock)	tCKO(2)		•Data hold from SCK0, 1 •Refer to figure 5	4.5 to 6.0			1 / 3tCYC +0.2			
					2.5 to 6.0			1 / 3tCYC +1			

5. Pulse Input Conditions at Ta= -30°C to +70°C, VSS= 0V

Parameter	Symbol	Pins	Conditions	VDD [V]	Ratings			unit
					min.	typ.	max.	
High / low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2 / T0IN	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3 / T0IN (The noise rejection clock select to 1 / 1.)	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	2			
	tPIH(3) tPIL(3)	INT3 / T0IN (The noise rejection clock select to 1 / 64.)	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	128			
	tPIL(4)	RES	Reset acceptable	2.5 to 6.0	200			μs

6. A / D Converter Characteristics at Ta= -30°C to +70°C, VSS= 0V

Parameter	Symbol	Pins	Conditions	VDD [V]	Ratings			unit
					min.	typ.	max.	
Resolution	N			4.5 to 6.0		8		bit
Absolute precision	ET		(Note 2)	4.5 to 6.0			±1.5	LSB
Conversion time	tCAD		AD conversion time=16×tCYC (ADCR2=0) (Note 3)	4.5 to 6.0	15.68 (tCYC= 0.98μs)		65.28 (tCYC= 4.08μs)	μs
			AD conversion time=32×tCYC (ADCR2=1) (Note 3)		31.36 (tCYC= 0.98μs)		130.56 (tCYC= 4.08μs)	
Analog input voltage range	VAIN	AN0 to AN3		4.5 to 6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 to 6.0			1	μA
	IAINL		VAIN=VSS	4.5 to 6.0	-1			

(Note 2) Absolute precision excepts quantizing error (±1 / 2 LSB).

(Note 3) The conversion time means the time to set complete digital conversion value to register from execution of instruction to start conversion.

7. Current Dissipation Characteristics at Ta=-30°C to +70°C, V_{SS}= 0V

Parameter	Symbol	Pins	Conditions	VDD [V]	Ratings			unit
					min.	typ.	max.	
Current dissipation during basic operation (Note 4)	IDDOP(1)	VDD	•FmCF=12MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops.	4.5 to 6.0		10	20	mA
	IDDOP(2)		•FmCF=3MHz Ceramic resonator oscillation. •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops.	4.5 to 6.0		3	9	
	IDDOP(3)		oscillation stops.	2.5 to 4.5		1.5	5	
	IDDOP(4)		•FmCF=0Hz (when oscillation stops). •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation	4.5 to 6.0		0.7	2.3	
	IDDOP(5)		RC oscillation	2.5 to 4.5		0.4	1.6	μA
	IDDOP(6)		•FmCF=0Hz (when oscillation stops). •FsXtal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops.	4.5 to 6.0		35	130	
	IDDOP(7)		oscillation stops.	2.5 to 4.5		15	70	

Parameter	Symbol	Pins	Conditions	VDD [V]	Ratings			unit
					min.	typ.	max.	
Current dissipation HALT mode (Note 4)	IDDHALT(1)	VDD	•HALT mode •FmCF=12MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops.	4.5 to 6.0		5	10	mA
	IDDHALT(2)		•HALT mode •FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops.	4.5 to 6.0		2.2	7.4	
	IDDHALT(3)			2.5 to 4.5		0.8	3.6	
	IDDHALT(4)		•HALT mode •FmCF=0Hz (when oscillation stops). •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation	4.5 to 6.0		400	1100	μA
	IDDHALT(5)			2.5 to 4.5		200	700	
	IDDHALT(6)		•HALT mode •FmCF=0Hz (when oscillation stops). •FsXtal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops.	4.5 to 6.0		25	100	
	IDDHALT(7)			2.5 to 4.5		8	55	
Current dissipation HOLD mode (Note 4)	IDDHOLD(1)	VDD	HOLD mode	4.5 to 6.0		0.05	30	
	IDDHOLD(2)			2.5 to 4.5		0.02	20	

(Note 4) The currents of output transistors and pull-up transistors are ignored.

Table 1. Ceramic resonator oscillation guaranteed constant (main-clock)

A kind of oscillation	Producer	Oscillator	C1	C2
12MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33pF	33pF
		CSA12.0MT	33pF	33pF
		CST12.0MTW	on chip	
	Kyocera	KBR-12.0M	33pF	33pF
3MHz ceramic resonator oscillation	Murata	CSA3.00MG	33pF	33pF
		CST3.00MGW	on chip	
	Kyocera	KBR-3.0MS	47pF	47pF

* Both C1 and C2 must use K rank ($\pm 10\%$) and SL characteristics.

Table 2. Crystal oscillation guaranteed constant (sub clock)

A kind of oscillation	Producer	Oscillator	C3	C4
32.768kHz crystal oscillation	Dai Sinku	DT-38 (1TA252E00)	18pF	18pF
	Kyocera	KF-38G-13P0200	18pF	18pF

* Both C3 and C4 must use J rank ($\pm 5\%$) and CH characteristics.

(It is about the application which is not in need of high precision. Use K rank ($\pm 10\%$) and SL characteristics.)

- (Note) • Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
 • If you use other oscillators herein, we provide no guarantee for the characteristics.

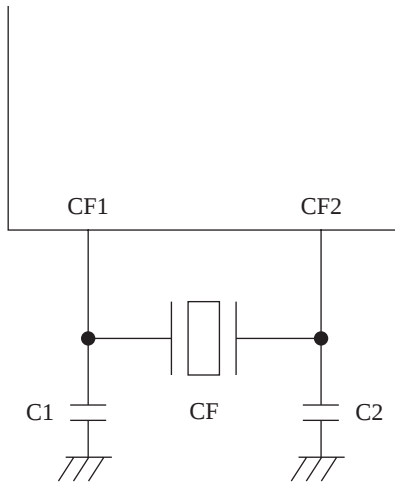


Figure1. Main-clock circuit
Ceramic resonator oscillation

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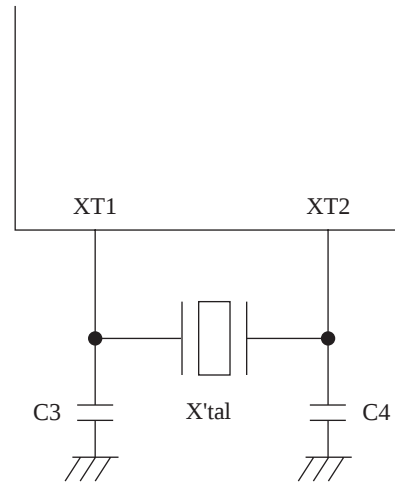


Figure2. Sub-clock circuit
Crystal oscillation

ILC00159

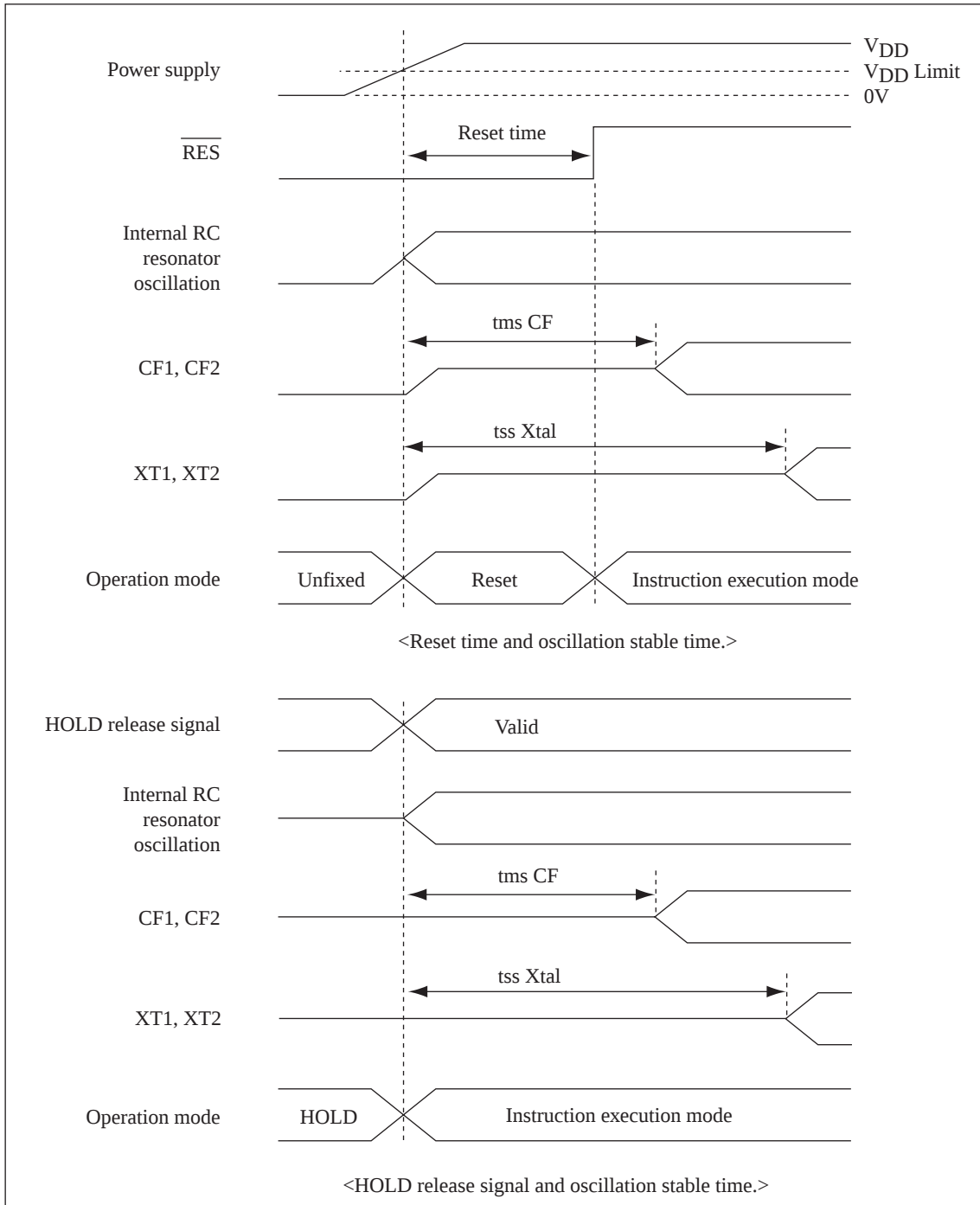
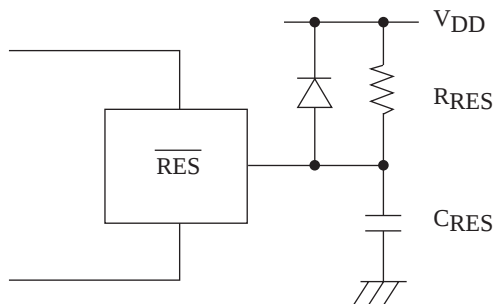


Figure3. Oscillation stable time

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(Note) Fix the value of R_{RES} , C_{RES} that is sure to reset until 200 μ s, after Power supply has been over inferior limit of supply voltage.

Figure4. Reset circuit

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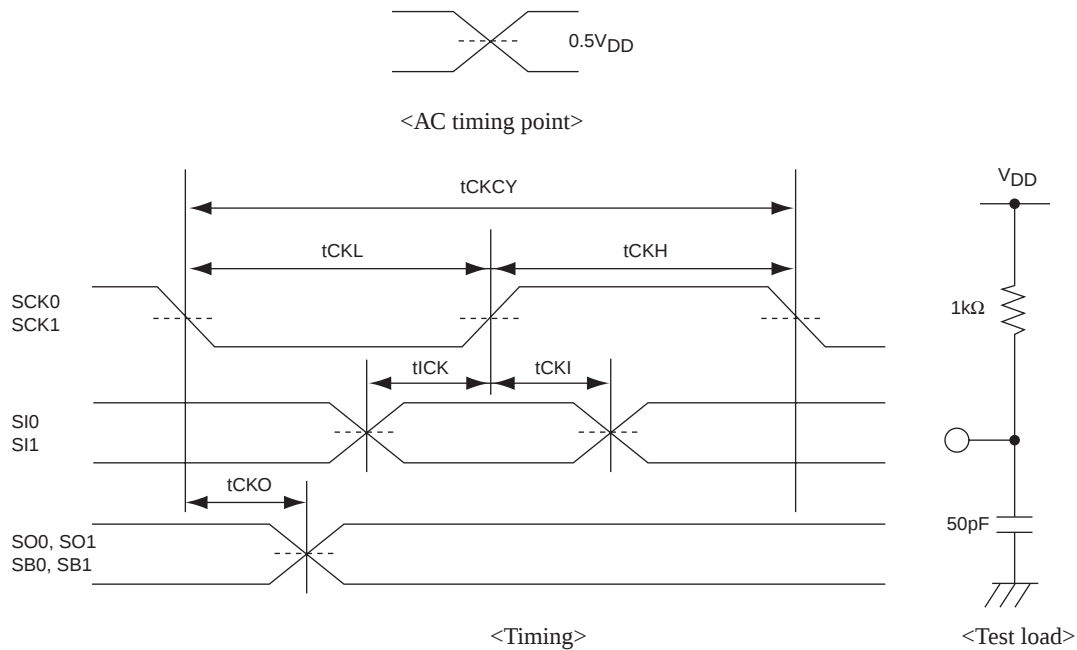


Figure5. Serial input / output test condition

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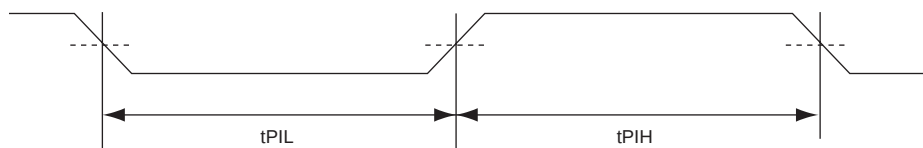


Figure6. Pulse input timing condition

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