# LC86216A, 86212A, 86208A

T-49-19-08

CMOS LSI

## 8-Bit Single Chip Microcomputer

### On-Chip LCD Controller/Driver, 16K-Byte ROM, 336-Byte RAM



TENTATIVE

**Overview**

The LC86216A, 86212A, 86208A microcomputers are 8-bit single chip microcomputers with the following on-chip functional blocks :

- CPU : Operable at a minimum cycle time of 1μs
- On-chip ROM : Capacity = 16K/12K/8K bytes
- On-chip RAM : Capacity = 336 bytes
- Dot matrix Liquid Crystal automatic display controller/driver
- Two 16-bit timers/counters
- Asynchronous serial interface
- 10-source 5-level vectored interrupt system
- External ROM/RAM mode

**Features**

(1) Read-Only Memory (ROM) : 16384×8 bits (LC86216A)
12288×8 bits (LC86212A)
8096×8 bits (LC86208A)

(2) Random Access Memory (RAM) : 256×8 bits For computation (general purpose RAM)
80×8 bits For data display (display RAM)

(3) Cycle Time : Cycle time varies depending on system clock sources. The selectable system clock sources are shown in the table below.

| Cycle Time | System Clock Source | Oscillation Frequency | Operating Voltage Range |
|---|---|---|---|
| 1μs | Ceramic (CF) resonator oscillation specification | 12MHz | 4.5 to 6.0V |
| 4μs | Ceramic (CF) resonator oscillation specification | 3MHz | 2.5 to 6.0V |

(4) Input/Output Ports : 6 ports (48 port pins)

(5) Liquid Crystal Display Drivers :
- Common driver pins : 16
- Segment driver pins : 40 (Extendable to 200 segments with LC7930×4)
- Display signal duty mode : 1/1 duty cycle to 1/16 duty cycle
- Display biasing mode : 1/1 bias to 1/5 bias

(6) Display Capacity : Graphic mode 640 dots max.
Character mode 640 dots max. (8 digits×2 lines)
3200 dots max. (40 digits×2 lines) available with LC7930×4

(7) Character Generator ROM : ROM capacity 8960 bits
Character font 5×7 dots max.
Number of characters 256

(8) Timer : 16-bit timer/counter×2
15-bit time base-timer×1

(9) Serial Interface : Full duplex
UART

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(10) External ROM/RAM Access Mode on Chip :

| | | |
|---|---|---|
| – External ROM space | External program ROM space | 64K bytes |
| | External data ROM space | 16M bytes |
| – External RAM space | 16M bytes | |
| – External RAM access instruction | (LDX, STX : 2-cycle instruction) | |

(11) Interrupt Mechanism : 10 sources and 5 vectored interrupts
External interrupt $\overline{\text{INT0}}/\overline{\text{INT1}}$
Timer/counter interrupt T0/T1
UART, divider, port 1/port 3

(12) Sub-routine Stack Level : 128 levels max. (Stack area included in the RAM area)

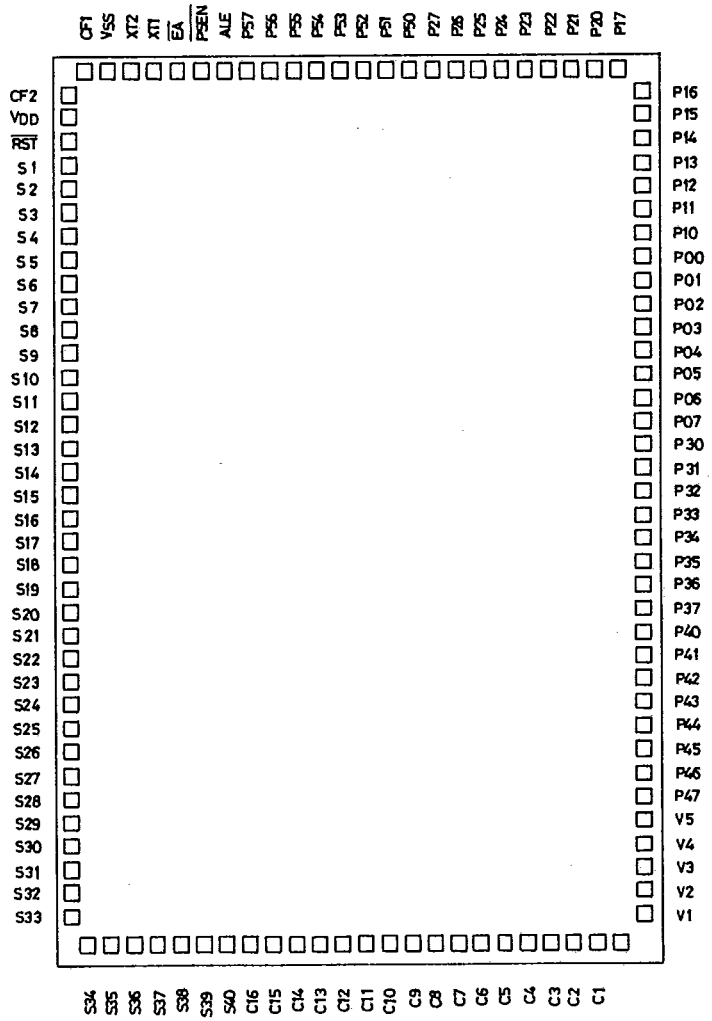
(13) Oscillator : 2 oscillators (CF/RC oscillation and crystal oscillation)

(14) Standby Function :

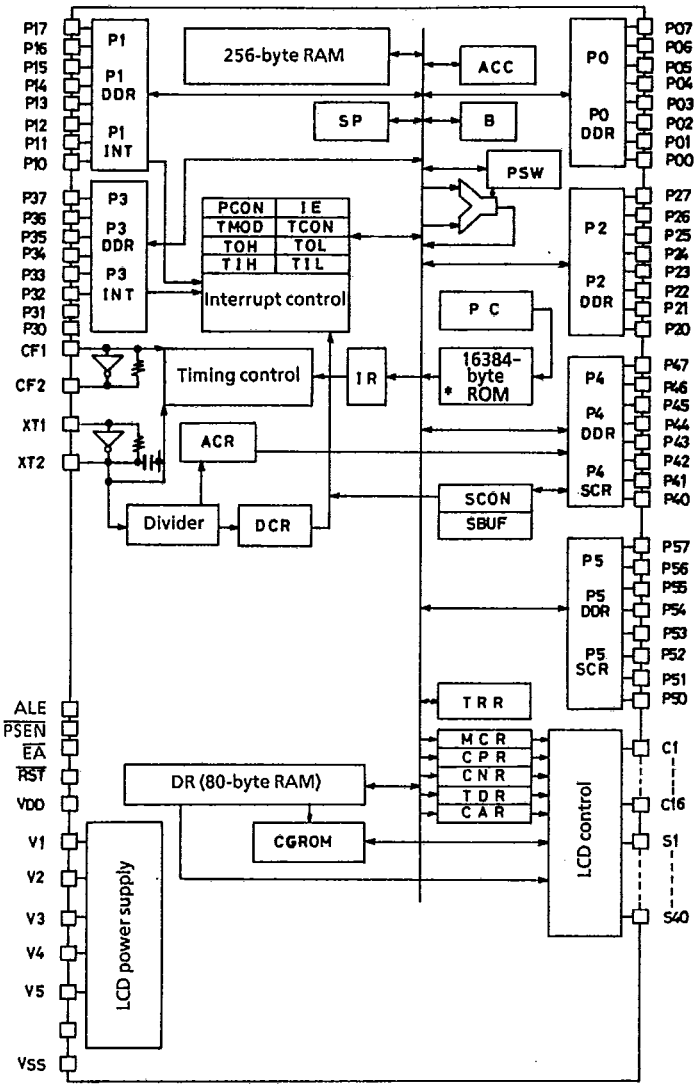
– HALT mode function : The HALT mode is used to reduce power dissipation. In this operation mode, program execution is stopped.

– HOLD mode function : The HOLD mode is used to freeze both of the CF/RC oscillation and crystal oscillation.

**LC86216A Pad Assignment**



**LC86216A System Block Diagram**




* Note Difference between Type Nos. LC86212A : ROM 12288 bytes
LC86208A : ROM 8096 bytes

## Pin Description

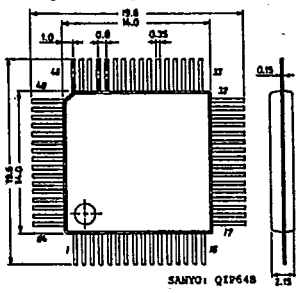
| Pin Name | I/O | Functional Description |
|---|---|---|
| $V_{SS}$ | — | Should be connected with the negative supply voltage pin. |
| $V_{DD}$ | — | Should be connected with the positive supply voltage pin. |
| P00 to 07 | Input/ Output | 8-bit input/output port with internal pull-up resistors.<br>Data can be input/output from/to the port in byte units.<br>Common with the following output pins having different functions. |
| P00 to 07 | Input/ Output | PAR0 to 7 : External ROM/RAM address output and data input/output pin |
| P10 to 17 | Input/ Output | 8-bit input/output port with internal pull-up resistors.<br>Data can be input/output from/to the port in bit units.<br>Common with the following output pins having different functions. |
| P10 to 17 | Output | PAR0 to 7 : External ROM/RAM address output (low-order 8 bits) |
| P20 to 27 | Input/ Output | 8-bit input/output port with internal pull-up resistors.<br>Data can be input/output from/to the port in bit units.<br>Common with the following output pins having different functions. |
| P20 to 27 | Output | PAR8 to 15 : External ROM/RAM address output (high-order 8 bits) |
| P30 to 37 | Input/ Output | 8-bit input/output port with internal pull-up resistors.<br>Data can be input/output from/to the port in bit units.<br>Common with the following output pins having different functions. |
| P36 | Output | $\overline{RD}$ : Read signal output to external RAM |
| P37 | Output | $\overline{WR}$ : Write signal output to external RAM |
| P40 to 47 | Input/ Output | 8-bit input/output port with internal pull-up resistors.<br>Data can be input/output from/to the port in bit units.<br>Common with the following output pins having different functions. |
| P40 | Output | CL1 : Latch signal output to external Liquid Crystal Display driver circuit |
| P41 | Output | CL2 : Shift signal output to external Liquid Crystal Display driver circuit |
| P42 | Output | D0 : Data signal output to external Liquid Crystal Display driver circuit |
| P43 | Output | M : Synchronization signal output to external Liquid Crystal Display driver circuit |
| P44 | Output | ALM : Alarm signal output to the ALM output pin |
| P45 | Output | PLS : Pulse signal output to the pulse output pin |
| P46 | Input/ Output | P30OUT : Serial port input/output pins |
| P47 | Output | P31OUT : Serial port output pin |
| P50 to 57 | Input/ Output | 8-bit input/output port with internal pull-up resistors.<br>Data can be input/output from/to the port in bit units.<br>Common with the following output pins having different functions. |
| P50 to 57 | Output | EXBNK0 to 7 : External ROM bank address |
| V1 to 5 | — | Voltage supply pins for Liquid Crystal Display drivers |
| C1 to 16 | Output | Common driver pins for Liquid Crystal Display drivers |
| S1 to 40 | Output | Segment driver pins for Liquid Crystal Display drivers |
| $\overline{RST}$ | Input | Reset signal input pin with an internal pull-up resistor |
| $\overline{PSEN}$ | Output | Pin used to control the external ROM output in the external ROM mode |
| ALE | Output | Pin used to output the external latch pulse when addresses are output at port 0 in the external ROM/RAM mode |
| $\overline{EA}$ | Input | Should be connected with $V_{DD}$ in the internal ROM mode. Should be connected with $V_{SS}$ in the external ROM mode. |
| XT1 | Input | Crystal oscillation input pin |
| XT2 | Output | Crystal oscillation input pin<br>The internal 20pF capacitor is provided between the XT2 and the $V_{DD}$ pin. |
| CF1 | Input | Ceramic resonator oscillation input pin, or RC (Resistor and Capacitor) oscillation input pin |
| CF2 | Output | Ceramic resonator oscillation output pin, or RC (Resistor and Capacitor) oscillation output pin |

T-90-20

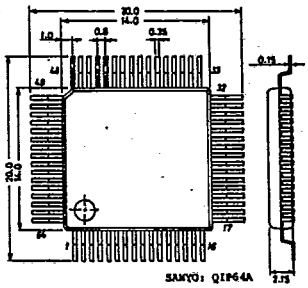
# CASE OUTLINES OF 8/4-BIT MICROCOMPUTERS WITH LCD DRIVER

- All of Sanyo microcomputer case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

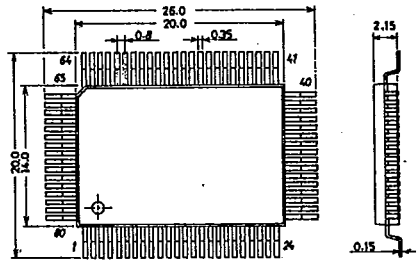
Case Outline—[3026B] unit:mm




Case Outline—[3057] unit:mm




Case Outline—[3044B] unit:mm




Case Outline—[3089] unit:mm