Ordering number: EN 4490A

CMOS LSI

SANYO

No. 4490A

LC74780, LC74780M

On-screen Video Display Controllers for VCRs

Overview

The LC74780 and LC74780M are CMOS, video display controllers for superimposing text and low-level graphics onto an NTSC, PAL or PAL-M compatible television receiver. Up to 288, 12 × 18-pixel characters can be displayed under microprocessor control on a 24-character by 12-line display.

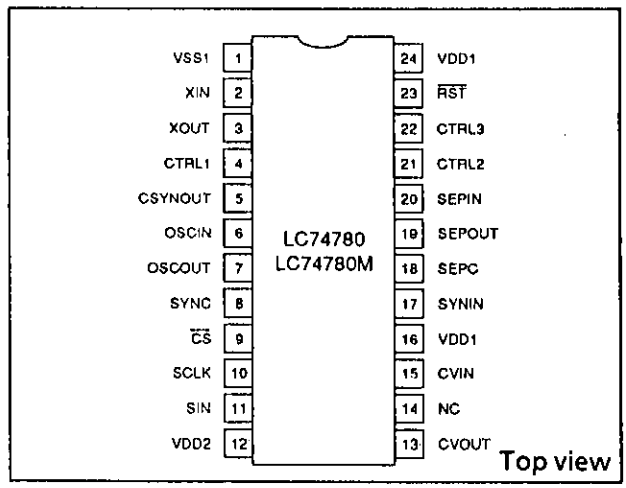
The LC74780 and LC74780M feature selectable pixel width and height, and 64 vertical and 64 horizontal display start positions. It also features a flashing enable bit for each character position.

The LC74780 and LC74780M operate from a 5 V supply. The LC74780 is available in 24-pin DIPs, and the LC74780M, in 24-pin MFPs.

Features

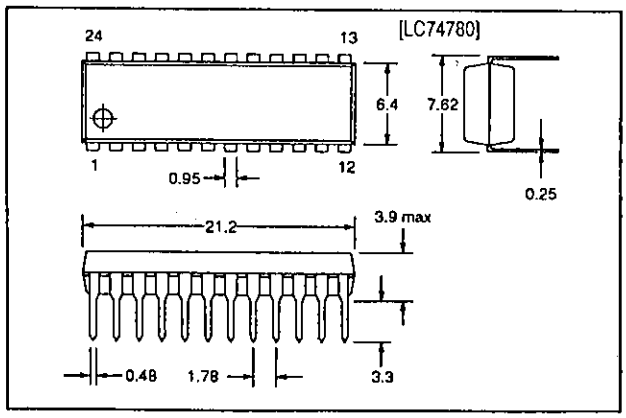
- Complete text and graphics video overlay circuitry
- 128-character internal character generator ROM
- 12 × 18-pixel characters
- Three pixel widths and three pixel heights
- Selectable background color
  - 8 colors at $4f_{SC}$ (NTSC/PAL/PAL-M)
  - 4 colors at $2f_{SC}$ (NTSC)
- Built-in synchronization check and separation circuitry
- Approximately 0.5 or 1 s period character flashing option
- Screen blanking
- NTSC, PAL and PAL-M format compatibility
- 8-bit serial input format
- 5 V supply
- 24-pin plastic DIP and 24-pin plastic MFP

Pin Assignment



Package Dimensions

3067-DIP24S



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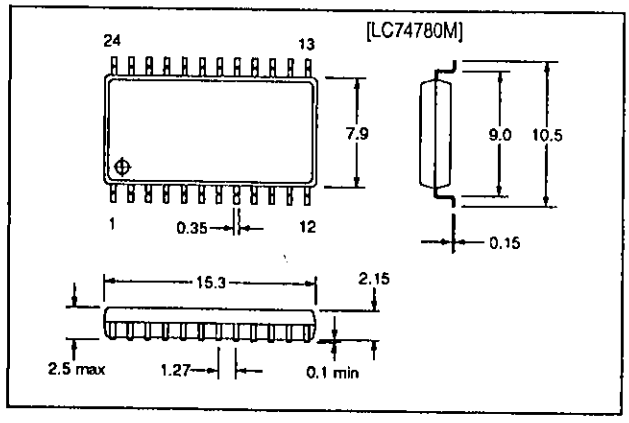

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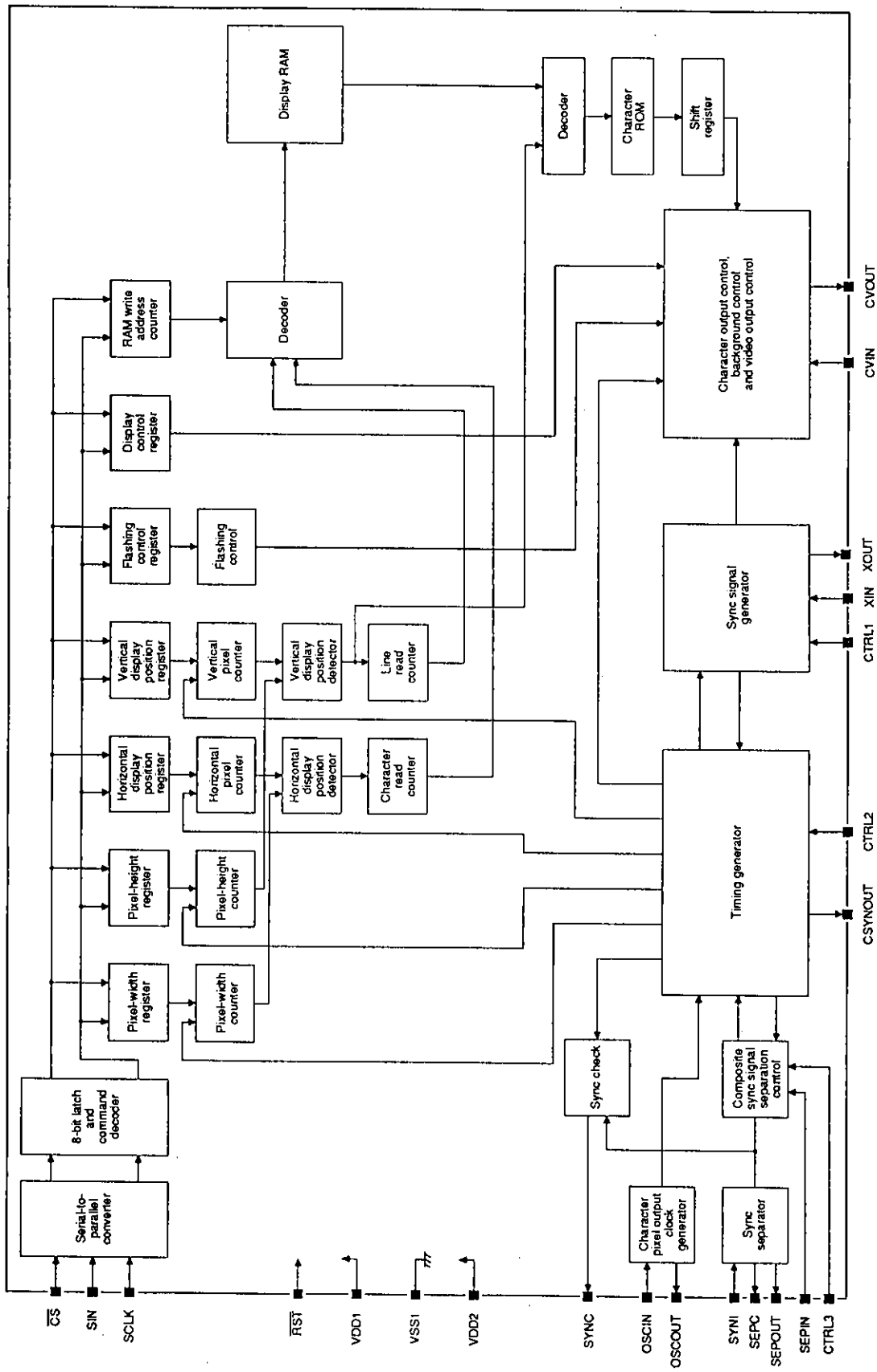
Block Diagram



Pin Functions

Number	Name	Function
1	VSS1	Ground
2	XIN	Internal sync signal crystal oscillator capacitor connections or external clock input ($2f_{SC}$ or $4f_{SC}$)
3	XOUT	
4	CTRL1	Clock input mode select. HIGH for external clock input mode, and LOW for crystal oscillator mode
5	CSYNOUT	Composite synchronization signal output. During reset ($\overline{RST}$ LOW), crystal oscillator clock is output. No output for internal reset command
6	OSCIN	LC oscillator input. LC circuit for pixel clock generation character output
7	OSCOUT	LC oscillator output. LC circuit for pixel clock generation character output
8	SYNC	External synchronization signal check output. HIGH when sync is detected. During reset ($\overline{RST}$ LOW), pixel clock is output. No output for internal reset command
9	$\overline{CS}$	Serial data input enable when LOW, with pull-up resistance (hysteresis input)
10	SCLK	Clock input for serial data input, with pull-up resistance (hysteresis input)
11	SIN	Serial data input, with pull-up resistance (hysteresis input)
12	VDD2	Power supply for composite video image signal level modulation (for analog system)
13	CVOUT	Composite video image signal output
14	NC	No connection
15	CVIN	Composite video image signal input
16	VDD1	5 V power supply for digital system
17	SYNCIN	Synchronization separation circuit input. If internal sync separation circuit is not used, use SYNCIN to input an external horizontal or composite synchronization signal.
18	SEPC	Synchronization separation circuit modulator capacitor connection. Leave open if not used.
19	SEPOUT	Composite synchronization separation circuit output. Outputs SYNCIN signal if internal sync separation is not used.
20	SEPIN	Vertical synchronization signal input. Tie to VDD1 if not used.
21	CTRL2	NTSC/PAL/PAL-M sync signal generation method select input. PAL-M when HIGH. NTSC/PAL/PAL-M selected by command when LOW.
22	CTRL3	SEPIN input control. $\overline{VSYNC}$ input signal when LOW, and not input when HIGH
23	$\overline{RST}$	System reset input, with pull-up resistance (hysteresis input)
24	VDD1	5 V power supply for digital system

Specifications

Absolute Maximum Ratings

T_a = 25 °C

Parameter	Symbol	Ratings	Unit
VDD1 AND VDD2 supply voltage range	V_{DD} max	V_{SS} – 0.3 to V_{SS} + 7.0	V
Input voltage range for all inputs	V_{IN} max	V_{SS} – 0.3 to V_{DD} + 0.3	V
CSYNOUT, SYNC and SEPOUT output voltage range	V_{OUT} max	V_{SS} – 0.3 to V_{DD} + 0.3	V
Power dissipation (T_a = 25 °C)	P_d max	350	mW
Operating temperature range	Topr	–30 to +70	°C
Storage temperature range	T_{stg}	–40 to +125	°C

Allowable Operating Ranges

T_a = −30 to +70 °C

Parameter	Symbol	Ratings	Unit
Logic supply voltage	V_{DD1}	5.0	V
Analog supply voltage	V_{DD2}	5.0	V
Logic supply voltage range	V_{DD1}	4.5 to 5.5	V
Analog supply voltage range	V_{DD2}	4.5 to 1.27V_{DD1}	V

Electrical Characteristics

T_a = −30 to +70 °C, unless otherwise noted V_{DD1} = 5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
VDD1 logic supply current	I_{DD1}	All outputs open, 7.159 MHz crystal oscillator, 8 MHz LC oscillator	–	–	15	mA
VDD2 analog supply current	I_{DD2}	V_{DD2} = 5 V	–	–	20	mA
CVIN input leakage current	I_{leak1}		–	–	1	μA
CVOUT output leakage current	I_{leak2}		–	–	1	μA
CTRL1, CTRL2, CTRL3 and OSCIN LOW-level input current	I_{IL}	V_{IN} = V_{SS1}	−1	–	–	μA
$\overline{RST}$, $\overline{CS}$, SIN, SCLK, CTRL1, SEPIN, CTRL2 and CTRL3 HIGH-level input current	I_{IH}	V_{IN} = V_{DD1}	–	–	1	μA
$\overline{RST}$, $\overline{CS}$, SIN and SCLK LOW-level input voltage	V_{IL1}		V_{SS} − 0.3	–	0.2V_{DD1}	V
CTRL1, CTRL2, CTRL3 and SEPIN LOW-level input voltage	V_{IL2}		V_{SS} − 0.3	–	0.3V_{DD1}	V
$\overline{RST}$, $\overline{CS}$, SIN and SCLK HIGH-level input voltage	V_{IH1}		0.8V_{DD1}	–	V_{DD1} + 0.3	V
CTRL1, CTRL2, CTRL3 and SEPIN HIGH-level input voltage	V_{IH2}		0.7V_{DD1}	–	V_{DD1} + 0.3	V
CVIN composite video input voltage	V_{IN1}		–	2.0	–	V_{p-p}
SYNCIN composite video input voltage	V_{IN2}		–	2.0	2.5	V_{p-p}
XIN input voltage	V_{IN3}	External clock input, f_{IN} = 2f_{SC} or 4f_{SC}	0.20	–	5.0	V_{p-p}
CSYNOUT, SYNC and SEPOUT LOW-level output voltage	V_{OL1}	V_{DD1} = 4.5 V, I_{OL} = 1.0 mA	–	–	1.0	V
CSYNOUT, SYNC and SEPOUT HIGH-level output voltage	V_{OH1}	V_{DD1} = 4.5 V, I_{OH} = −1.0 mA	3.5	–	–	V
CVOUT sync voltage	V_{SN}	See note 1.	0.70	0.82	0.94	V
		See note 2.	0.95	1.07	1.19	V
CVOUT pedestal voltage	V_{PD}	See note 1.	1.30	1.42	1.54	V
		See note 2.	1.54	1.66	1.78	V
CVOUT LOW-level color burst voltage	V_{CBL}	See note 1.	1.00	1.12	1.24	V
		See note 2.	1.25	1.37	1.49	V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
CVOUT HIGH-level color burst voltage	V_{CBH}	See note 1.	1.62	1.74	1.86	V
		See note 2.	1.85	1.97	2.09	V
CVOUT LOW-level background color voltage	V_{RSL}	See note 1.	1.45	1.57	1.69	V
		See note 2.	1.69	1.81	1.93	V
CVOUT HIGH-level background color voltage	V_{RSH}	See note 1.	1.98	2.10	2.22	V
		See note 2.	2.21	2.33	2.45	V
CVOUT border voltage	V_{BK}	See note 1.	1.52	1.64	1.76	V
		See note 2.	1.66	1.78	1.90	V
CVOUT character voltage	V_{CHA}	See note 1.	2.63	2.75	2.87	V
		See note 2.	2.79	2.91	3.03	V
$\overline{RST}$, $\overline{CS}$, SIN and SCLK pull-up resistance	R_{PU}	Depends on optional settings at pins	25	50	90	kΩ
XIN and XOUT oscillator frequency	f_{OSC1}	NTSC ($2f_{SC}$)	–	7.159	–	MHz
		NTSC ($4f_{SC}$)	–	14.318	–	MHz
		PAL ($4f_{SC}$)	–	17.734	–	MHz
		PAL-M ($4f_{SC}$)	–	14.302	–	MHz
OSCIN and OSCOUT oscillator frequency	f_{OSC2}	LC oscillator	5	–	10	MHz

Notes

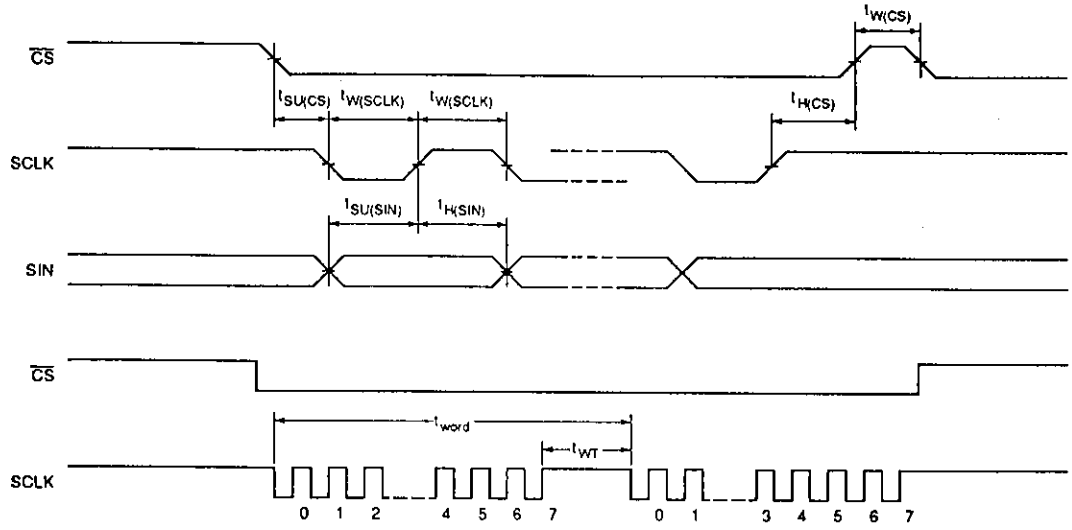
1. CV_{OUT} at $V_{DD1} = V_{DD2} = 5.0$ V, 0.8 V sync level
2. CV_{OUT} at $V_{DD1} = V_{DD2} = 5.0$ V, 1.0 V sync level

Timing Characteristics

$V_{DD1} = 5 \pm 0.5$ V, $T_a = -30$ to $+70$ °C

Parameter	Symbol	Ratings			Unit
		min	typ	max	
SCLK input pulsewidth	$t_{W(SCLK)}$	200	–	–	ns
$\overline{CS}$ HIGH-level input pulsewidth	$t_{W(CS)}$	1	–	–	µs
$\overline{CS}$ input setup time	$t_{SU(CS)}$	200	–	–	ns
SIN data input setup time	$t_{SU(SIN)}$	200	–	–	ns
$\overline{CS}$ input hold time	$t_{H(CS)}$	2	–	–	µs
SIN data input hold time	$t_{H(SIN)}$	200	–	–	ns
8-bit data word write time	t_{WORD}	4.2	–	–	µs
RAM data write time	t_{WT}	1	–	–	µs

Serial data input timing



Display Control Features and Characteristics

Display Control Command Structure

The display control commands, COMMAND0 to COMMAND7, are shifted in 8-bit serial units. The first byte of a command consists of an identification code and data. The second byte consists of data only. Once the command identification code in byte 1 has been written, it is saved until the next time the first byte is written. If COMMAND1 is written, the display character write mode begins and the first byte does not change. When $\overline{CS}$ is HIGH, COMMAND0 is set.

Display Control Command Data

Command	First byte								Second byte							
	Command code				Data or register storing data				Data or register storing data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 Display memory (VRAM) write address setting command	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND1 Display character data write command	1	0	0	1	0	0	0	0	at	C6	C5	C4	C3	C2	C1	C0
COMMAND2 Vertical display position and character size setting command	1	0	1	0	VS21	VS20	VS11	VS10	0	FS	VP5	VP4	VP3	VP2	VP1	VP0
COMMAND3 Horizontal display position and character size setting command	1	0	1	1	HS21	HS20	HS11	HS10	0	LC	HP5	HP4	HP3	HP2	HP1	HP0
COMMAND4 Display control setting command	1	1	0	0	TST MOD	RAM ERS	OSC STP	SYS RST	0	BLK2	BLK1	BLK0	BK1	BK0	RV	DSP ON
COMMAND5 Display control setting command	1	1	0	1	NP1	NP0	NON	INT	0	0	0	BCL	CB	PH2	PH1	PH0
COMMAND6 Synchronization signal control setting command	1	1	1	0	MOD1	MOD0	DIS LIN	MUT	0	RN2	RN1	RN0	SN3	SN2	SN1	SN0
COMMAND7 Display control setting command	1	1	1	1	EX1	PDI	EX0	PD0	-	-	-	-	-	-	-	-

COMMAND0: Display Memory Write Address Setting Command

COMMAND0: first byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	V0	0	Display memory line address 0 to BH	
		1		
1	V1	0		
		1		
2	V2	0		
		1		
3	V3	0		
		1		
4	–	0	COMMAND0 identification code	
5	–	0		
6	–	0		
7	–	1		

COMMAND0: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	H0	0	Display memory address 0 to 17H	
		1		
1	H1	0		
		1		
2	H2	0		
		1		
3	H3	0		
		1		
4	H4	0		
		1		
5	–	0		
6	–	0		
7	–	0	Second byte identification bit	

Note

On system reset with $\overline{RST}$, the status of all registers is set to 0.

COMMAND1: Display Character Data Write Command

COMMAND1: first byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	–	0		
1	–	0		
2	–	0		
3	–	0		
4	–	1	COMMAND1 identification code	After command is input, display character data write mode is set until $\overline{CS}$ is set HIGH.
5	–	0		
6	–	0		
7	–	1		

COMMAND1: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	C0	0	Character code 0 to 7FH	
		1		
1	C1	0		
		1		
2	C2	0		
		1		
3	C3	0		
		1		
4	C4	0		
		1		
5	C5	0		
		1		
6	C6	0		
		1		
7	at	0	Character attribute OFF	
		1	Character attribute ON	

Note

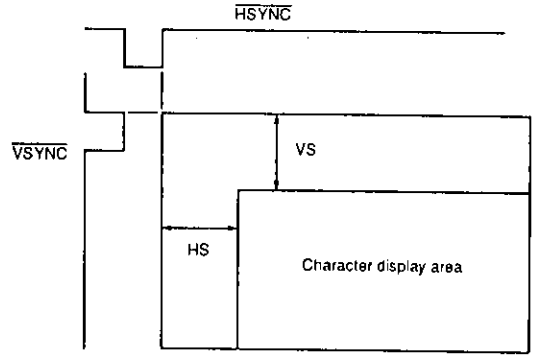
On system reset with $\overline{RST}$, the status of all registers is set to 0.

COMMAND2: Vertical Display Position and Character Size Setting Command

COMMAND2: first byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	VS10	0	VS11 = 0, VS10 = 0: 1H/pixel VS11 = 0, VS10 = 1: 2H/pixel VS11 = 1, VS10 = 0: 3H/pixel VS11 = 1, VS10 = 1: 1H/pixel	First line vertical character size
		1		
1	VS11	0		
		1		
2	VS20	0	VS21 = 0, VS20 = 0: 1H/pixel VS21 = 0, VS20 = 1: 2H/pixel VS21 = 1, VS20 = 0: 3H/pixel VS21 = 1, VS20 = 1: 1H/pixel	Second line vertical character size
		1		
3	VS21	0		
		1		
4	–	0	COMMAND2 identification code	
5	–	1		
6	–	0		
7	–	1		

COMMAND2: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	VP0 (LSB)	0	Initial vertical coordinate position determined by $VS = H \times \left(2 \sum_{n=0}^{5} 2^n VPn\right)$ where H is the horizontal synchronization pulse period. 	The initial vertical coordinate position is set in 6 bits, VP0 to VP5, where the LSB, VP0, corresponds to 2H.
		1		
1	VP1	0		
		1		
2	VP2	0		
		1		
3	VP3	0		
		1		
4	VP4	0		
		1		
5	VP5 (MSB)	0		
		1		
6	FS	0	$2f_{SC}$ crystal oscillator frequency	
		1	$4f_{SC}$ crystal oscillator frequency	
7	–	0	Second byte identification bit	

Note

On system reset with $\overline{RST}$, the status of all registers is set to 0.

COMMAND3: Horizontal Display Position and Character Size Setting Command

COMMAND3: first byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	HS10	0	HS11 = 0, HS10 = 0: 1Tc/pixel HS11 = 0, HS10 = 1: 2Tc/pixel HS11 = 1, HS10 = 0: 3Tc/pixel HS11 = 1, HS10 = 1: 1Tc/pixel	First line horizontal character size
		1		
1	HS11	0		
		1		
2	HS20	0	HS21 = 0, HS20 = 0: 1Tc/pixel HS21 = 0, HS20 = 1: 2Tc/pixel HS21 = 1, HS20 = 0: 3Tc/pixel HS21 = 1, HS20 = 1: 1Tc/pixel	Second line horizontal character size
		1		
3	HS21	0		
		1		
4	–	1	COMMAND3 identification code	
5	–	1		
6	–	0		
7	–	1		

COMMAND3: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	HP0 (LSB)	0	The initial horizontal coordinate position is given by $HS = T_C \times \left(2 \sum_{n=0}^{5} 2^n \, HPn\right)$ where T_c is the OSCIN and OSCOUT operation mode oscillation period.	The initial horizontal coordinate position is set in 6 bits, HP0 to HP5, where the LSB, HP0, corresponds to 2Tc.
		1		
1	HP1	0		
		1		
2	HP2	0		
		1		
3	HP3	0		
		1		
4	HP4	0		
		1		
5	HP5 (MSB)	0		
		1		
6	LC	0	LC oscillator dot clock	Selects the dot clock used for the character display transverse direction
		1	Crystal oscillator dot clock	
7	–	0	Second byte identification bit	

Note

On system reset with $\overline{RST}$, the status of all registers is set to 0.

COMMAND 4: Display Control Setting Command

COMMAND4: first byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	SYSRST	0		A system reset also occurs when $\overline{CS}$ goes LOW.
		1	Resets all registers and turns the display OFF	
1	OSCSTP	0	Crystal and LC oscillator stop disable	External sync mode character display
		1	Crystal and LC oscillator circuitry stop enable	
2	RAMERS	0		Approximately 500 µs are required to erase RAM (with display OFF)
		1	Erases display RAM (set to 7FH)	
3	TSTMOD	0	Normal operating mode	Test mode should not be selected during normal operation.
		1	Test mode	
4	–	0	COMMAND4 identification code	
5	–	0		
6	–	1		
7	–	1		

COMMAND4: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	DSPON	0	Character display OFF	
		1	Character display ON	
1	RV	0	Reverse characters OFF	
		1	Reverse characters ON	
2	BK0	0	Blinking OFF	When blinking inverse characters, characters alternate between normal and inverse.
		1	Blinking ON	
3	BK1	0	Blinking period approximately 0.5 s	Selects blinking period.
		1	Blinking period approximately 1.0 s	
4	BLK0	0		Selects the blanking area size.
		1		
5	BLK1	0		
		1		
6	BLK2	0	Character display	Full size selection
		1	Video display	
7	–	0	Second byte identification bit	

BLK1	BLK0	Blanking select
0	0	Blanking OFF
0	1	Character size
1	0	Border size
1	1	Full size

Note

On system reset with $\overline{RST}$, the status of all registers is set to 0.

COMMAND5: Display Control Setting Command

COMMAND5: first byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	INT	0	External synchronization	Switches between external and internal synchronization.
		1	Internal synchronization	
1	NON	0	Interlaced	Switches between interlaced and non-interlaced
		1	Non-interlaced	
2	NP0	0	See table below	Switches between NTSC, PAL and PAL-M modes.
		1		
3	NP1	0		
		1		
4	–	1	COMMAND5 identification code	
5	–	0		
6	–	1		
7	–	1		

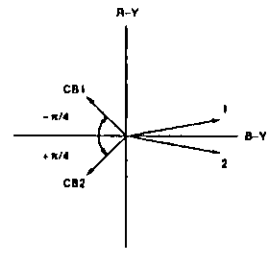
NP1	NP0	Mode select
0	0	NTSC
0	1	PAL-M
1	0	PAL
1	1	NTSC

COMMAND5: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	PH0	0	See table below	PAL color burst, background color phase diagram
		1		
1	PH1	0		
		1		
2	PH2	0		
		1		
3	CB	0	Color burst signal is output.	Applies when BCL = 1.
		1	Color burst signal output is halted.	
4	BCL	0	Background color present	Applies for internal synchronization only.
		1	Background color not present (background level only is set)	
5	–	0		
6	–	0		
7	–	0	Second byte identification bit	

PH2	PH1	PH0	Background color phase	
			NTSC	PAL
0	0	0	$\pi/2^*$	$\pm\pi/2$
0	0	1	In phase*	In phase
0	1	0	$3\pi/2^*$	$\mp\pi/2$
0	1	1	π^*	$\pm\pi$
1	0	0	$3\pi/4$	$\pm3\pi/4$
1	0	1	$\pi/4$	$\pm\pi/4$
1	1	0	$7\pi/4$	$\mp\pi/4$
1	1	1	$5\pi/4$	$\mp3\pi/4$

* NTSC at $2f_{SC}$



Note
On system reset with $\overline{RST}$, the status of all registers is set to 0.

COMMAND6: Synchronization Signal Control Setting Command

COMMAND6: first byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	MUT	0	Normal output	Switches CVOUT
		1	CVIN is cut and CVOUT is fixed at the pedestal level	
1	DISLIN	0	12 lines	Selects the number of display lines
		1	10 lines	
2	MOD0	0	Composite sync signal	Switches CSYNOUT
		1	Character and border OR-signal output	
3	MOD1	0	Composite synchronization separation signal	Switches SEPOUT
		1	HIGH-level output for internal sync	
4	–	0	COMMAND6 identification code	
5	–	1		
6	–	1		
7	–	1		

COMMAND6: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	SN0	0		External sync signal detection control Determines when the signal goes from ON to OFF. Selects the sampling period, in units of the horizontal sync signal cycle (1 H), for which the sync continues and cannot be detected.
		1		
1	SN1	0		
		1		
2	SN2	0		
		1		
3	SN3	0		
		1		
4	RN0	0		External sync signal detection control Determines when the signal goes from OFF to ON. Selects the sampling period, in units of the horizontal sync signal cycle (1 H), for which the sync continues and can be detected.
		1		
5	RN1	0		
		1		
6	RN2	0		
		1		
7	–	0	Second byte identification bit	

SN3	SN2	SN1	SN0	Detection frequency
0	0	0	0	No detection
0	0	0	1	32 times
0	0	1	0	64 times
0	1	0	0	128 times
1	0	0	0	256 times

RN2	RN1	RN0	Detection frequency
0	0	0	0 times
0	0	1	4 times
0	1	0	8 times
1	0	0	16 times

Note
On system reset with $\overline{RST}$, the status of all registers is set to 0.

COMMAND7: Display Control Setting Command

COMMAND7: first byte

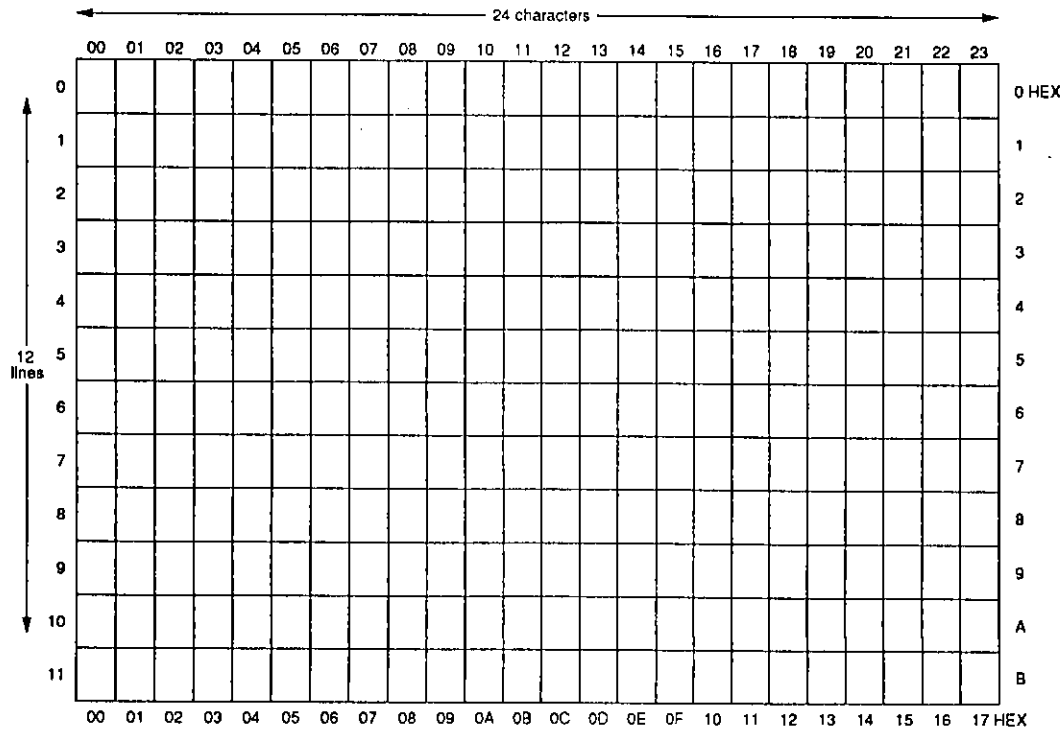
DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	PD0	0	LOW-level output	
		1	HIGH-level output	
1	EX0	0	MODE0 settings output	Switches CSYNOUT
		1	PORT DATA0 settings output	
2	PD1	0	LOW-level output	
		1	HIGH-level output	
3	EX1	0	MODE1 settings output	Switches SEPOUT
		1	PORT DATA1 settings output	
4	–	1	COMMAND7 identification code	
5	–	1		
6	–	1		
7	–	1		

Note

On system reset with $\overline{RST}$, the status of all registers is set to 0.

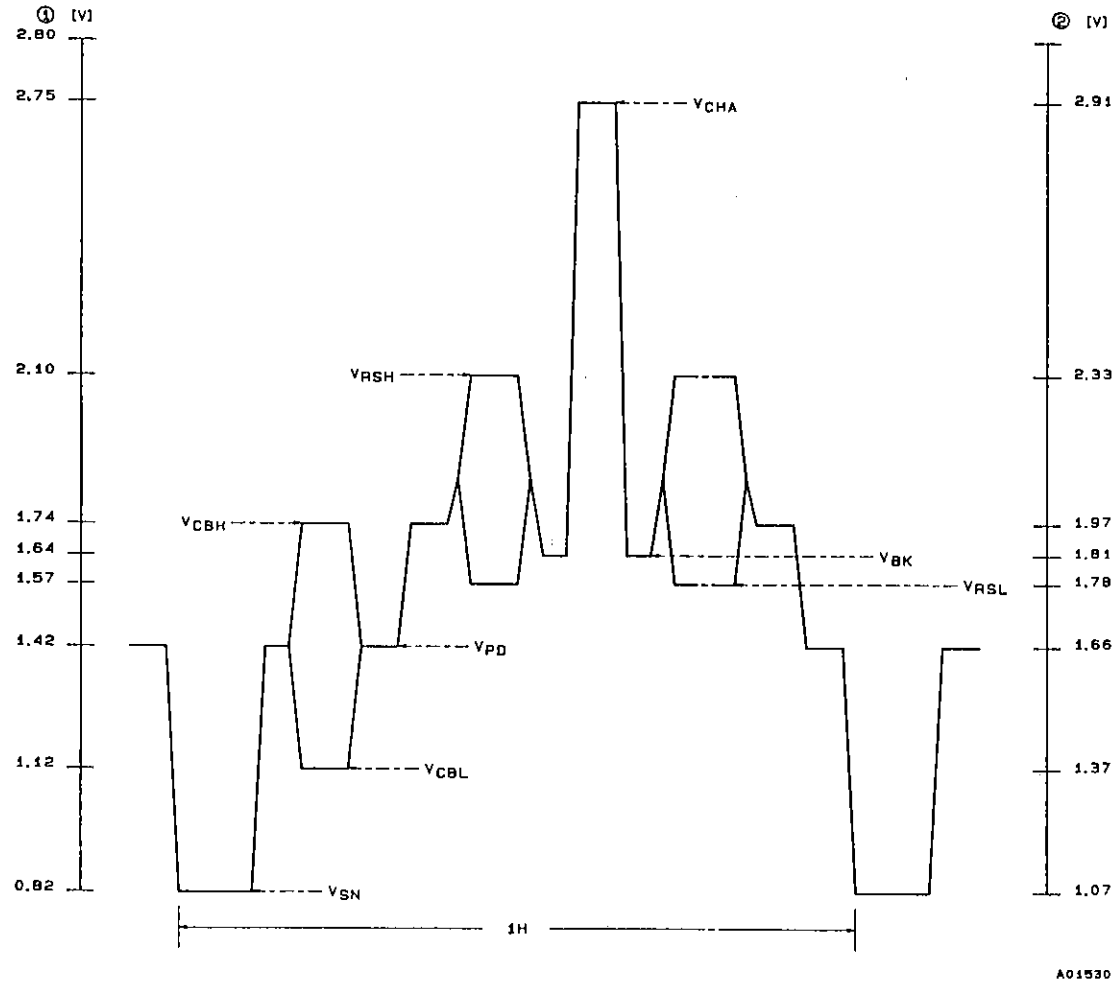
Display Configuration

The display is 24 characters by 12 rows large. Up to 288 characters can be displayed, unless the character size is expanded. The display memory address is set as a row address in the range 0 to 11 and a column address in the range 0 to 23.



Composite Video Output

CVOUT output waveform (V_{DD2} = 5.00 V)



Output voltage level	Symbol	Output voltage at 0.8 V sync (V)	Output voltage at 1.0 V sync (V)
Character	V_{CHA}	2.75	2.91
HIGH-level background color	V_{RSH}	2.10	2.33
HIGH-level color burst	V_{CBH}	1.74	1.97
LOW-level background color	V_{RSL}	1.57	1.81
Border	V_{BK}	1.64	1.78
Pedestal	V_{PD}	1.42	1.66
LOW-level color burst	V_{CBL}	1.12	1.37
Sync	V_{SN}	0.82	1.07

Note

V_{DD2} = 5.00 V