Ordering number:ENN5336

CMOS IC

LC7041

ID LOGIC® Interface with PLL

Overview

The LC7041 is the central IC to the ID LOGIC Module and Electronic Tuning Radio.

It performs the interface between the receiver's main microprocessor and ID LOGIC's 256kB database ROM and its 2kB update RAM. The LC7041 also contains the Phase-Locked Loop (PLL) circuitry responsible for electronic tuning and it offers several I/O ports.

The LC7041 permits the easy integration of the ID LOGIC Module in a receiver. It contains all the appropriate software to send and receive serial instructions and data to and from the receiver's main microprocessor. An instruction is given simply by having the main microprocessor send a one byte-long function code followed, when necessary, by the appropriate data. Upon execution, the LC7041 returns its response data, if any, to the microprocessor for display or other processing. Further the SUPER DX search control function is added to the LC7041.

Note

It is necessary to enter into an "ID LOGIC Licensing Contract" with PRS. Corp. before sample devices can be shipped.

Functions

- ID LOGIC Status read
  - · Read current (receiver) location.
  - · Read broadcast station location.
- State/province set
  - · Set/read state up.
  - · Set/read state down.
- City set (in current state)
  - · Set/read city up.
  - · Set/read city down.
- Travel
  - · 1 grid move north.
  - · 1 grid move east.
  - · 1 grid move south.
  - · 1 grid move west
  - · Set preset location (1 of 8).
  - · Return to preset location (1 to 8).
  - · Display main (largest) city in grid.
- DX status and search control
  - · Set LCL ON (Local=1 grid search).
  - · Set DX ON (DX=9 grid search).
  - · Set SUPER DX ON (25 grid search).
- Format scanning
  - · Format search up (1 of 7 general format keys) in selected LCL/DX.
  - · Search up another format.
  - · Write to RAM last station format.
  - · Read from RAM last station format.
- User formats
  - · Read user format in key (1 of 8 user keys).
  - · User format search up (1 of 8 user keys).
  - · Search up another user format.
  - · Search down anoter user format.
  - · Display user format up (1 of 32 formats).
  - · Display user format down.
  - · Set user format (1 of 32 formats in 1 of 8 user keys).
  - · Write to RAM last station user format.
  - · Read from RAM last station user format.
- Prior multi-station
  - · Set prior multi-station.
  - · Reset prior multi-station.
- Updates (tuning changes)
  - · Update mode ON.
  - · Update mode cancel.
  - · Update mode OFF (completed).
  - · Change frequency.
  - · Change call sign.
  - · Change format up/down.
  - · Enter new station.
  - · Reset 1 updated station (cancel update).
  - · Reset all update stations memories (cancel all updates).
- Tuning (seek or manual)
  - · Tune 1 channel up.
  - · Tune 1 channel down.
  - · Read status upon tuning change (Can be canceled midway by applying a LOW pulse signal (10μs or longer) to the $\overline{\text{INT}}$ pin).

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· IF count start.
· Multi-station check.
· Read station status.

• Band change
· Switch to AM.
· Switch to FM.

• I/O port and RAM
· OUT1 to OUT5 High/Low control.
· IN1 to IN5 input/read.
· Read ADC data.
· Read INFF data.

• Preset memory
· Write to preset memory with ID LOGIG mode ON.
· Read from preset memory with ID LOGIC mode ON.

• Initialization
· Set initial data :
- IF or IF counter.
- FM channel separation.
- FM low frequency.
- FM channel number.
· Read hot/cold status.
· Load frequency.
· Load AM and FM frequencies.
· Set initial location (grid + largest city in grid).

• Other
· ROM data (version) read

Addtion item from LC7040N
· Super DX ON
· Next user format search down.

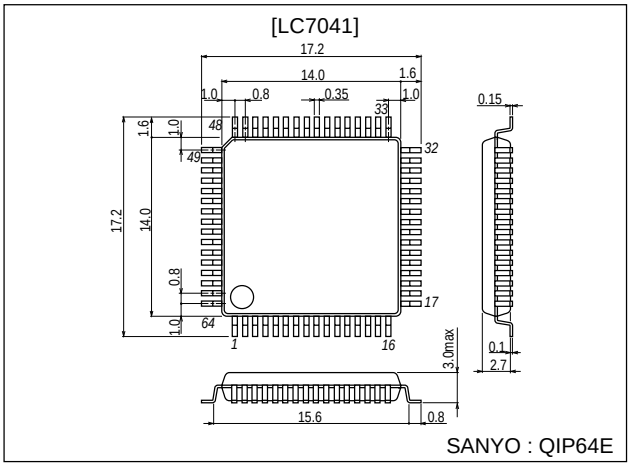
Elimination item from LC7040N
· ID LOGIC ON/OFF.
· Preset memory with ID LOGIC mode OFF.
· ROM data.
· Initiate user set format.

Alteration item from LC7040N
· Read user format (Unentry is represented by “F-No. – “FF” ”, with format No. being “don’t care”.)
· Set user format (A format enterd can be cleared by setting “FF” to F-No.)
· The search method has been changed as follows : The earlier method that 1 of 32 formats is entered for searching has been changed to a new method that 10 of 32 formats are selected and if at least 1 of these 10 formats matches a broadcast station is assumed to exist.

Package Dimensions

unit:mm

3159-QIP64E



Test Circuit

Backup Mode

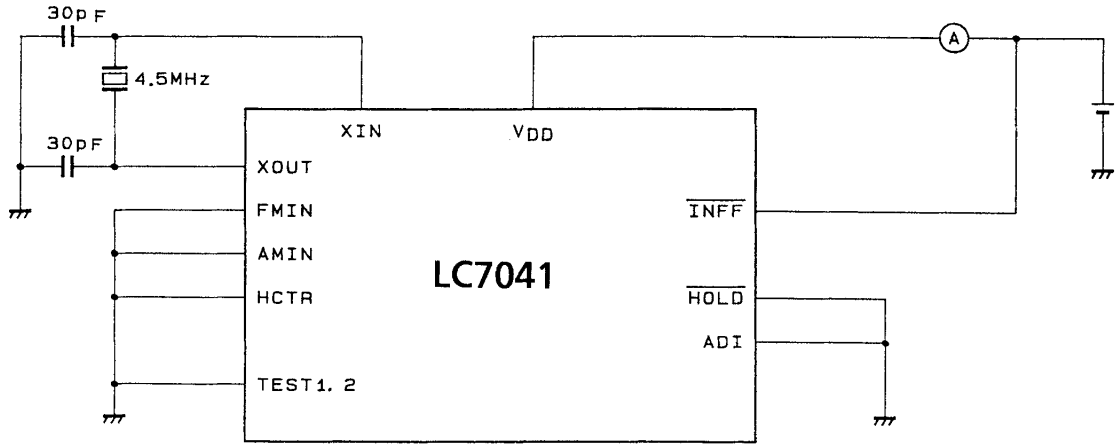
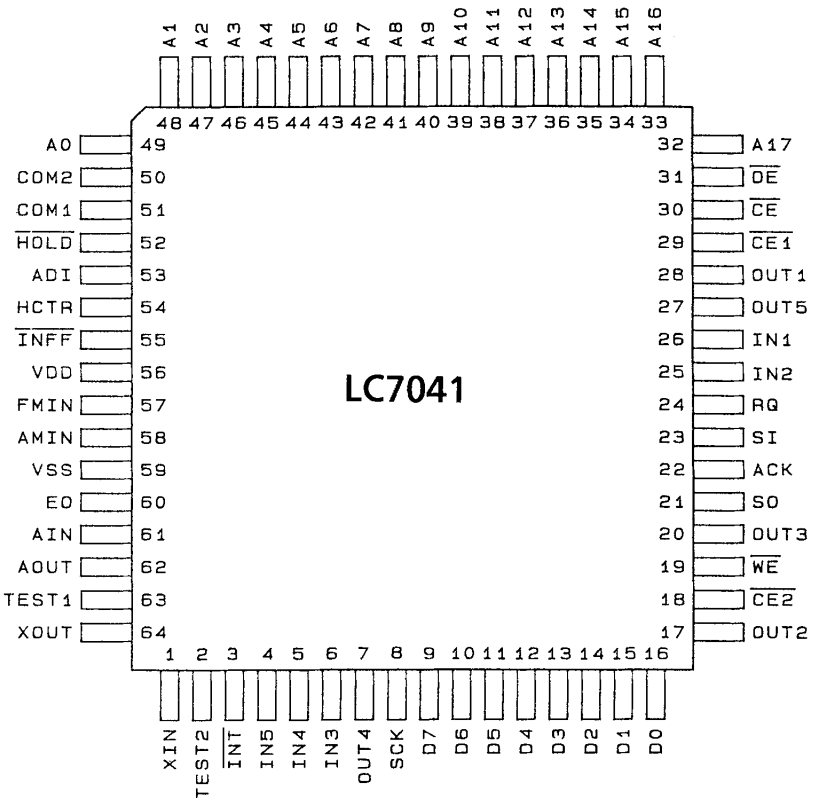


Figure 1

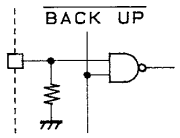
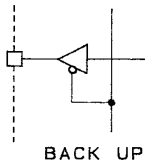
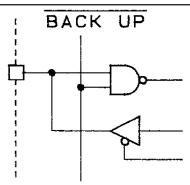
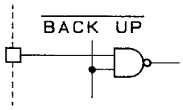
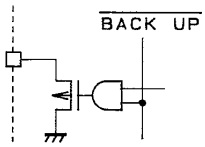
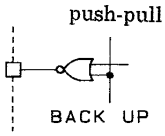
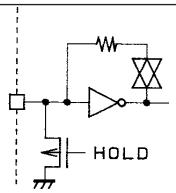
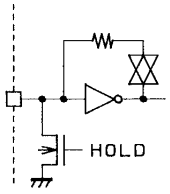
Note
Pins IN1 to IN5, OUT1 to OUT5, D0 to D7, RQ, SI, SO, SCK, ACK and $\overline{WE}$ are all left open.

Pin Assignment



Top view

Pin Functions

Number	Name	I/O	Equivalent circuit	Description	
26	IN1	I		Low-threshold input ports. Built-in 100kΩ (typ) pull-down resistance. Input is prohibited when $\overline{HOLD}$ is LOW.	
25	IN2				
24	RQ			Main microcontroller serial communications request signal.	
23	SI			Main microcontroller serial communications data input signal.	
22	ACK	O		Main microcontroller serial communications acknowledge signal.	Input is prohibited when $\overline{HOLD}$ is LOW.
21	SO			Main microcontroller serial communications data output signal.	
20	OUT3			General-purpose output port.	
19	$\overline{WE}$			RAM write enable signal.	
18	$\overline{CE2}$			RAM control signal.	
17	OUT2			General-purpose output port.	
16 to 9	D0 to D7	I		ROM and RAM data input pins. Input is prohibited when $\overline{HOLD}$ is LOW.	
6 to 4	IN3 to IN5	I		General-purpose input ports. Input is prohibited when $\overline{HOLD}$ is LOW.	
3	$\overline{INT}$			Processor intterrupt input. Valid for LOW-level pulses of 10 µs or longer. Interrupts are prohibited during backup mode.	
8	SCK	O		Main microcontroller serial communications clock signal. N-channel open-drain, high-voltage port for use with a pull-up resistor. High impedance when $\overline{HOLD}$ goes LOW.	
7	OUT4			General-purpose output port. N-channel open-drain, high-voltage port for use with a pull-up resistor. High impedance when $\overline{HOLD}$ goes LOW.	
32 to 49	A17 to A0	O		ROM and RAM address signal.	Input is prohibited when $\overline{HOLD}$ is LOW.
27	OUT5			General-purpose output ports.	
28	OUT1				
29	$\overline{CE1}$			ROM and RAM control signals.	
30	$\overline{CE}$				
31	$\overline{OE}$				
51	COM1	O	–	Leave open for normal use.	
50	COM2				
57	FMIN	I		FM VCO input. Capacitively couple for normal use.	
58	AMIN			AM VCO input. Capacitively couple for normal use.	
54	HCTR	I		IF counter input. Capacitively couple for normal use. 0.4 to 12MHz input frequency.	

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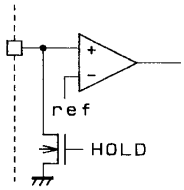
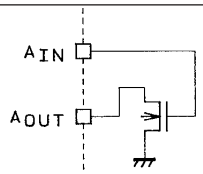
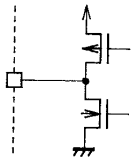
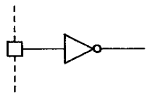
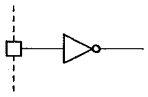
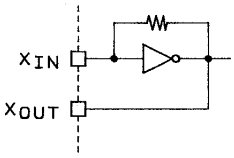
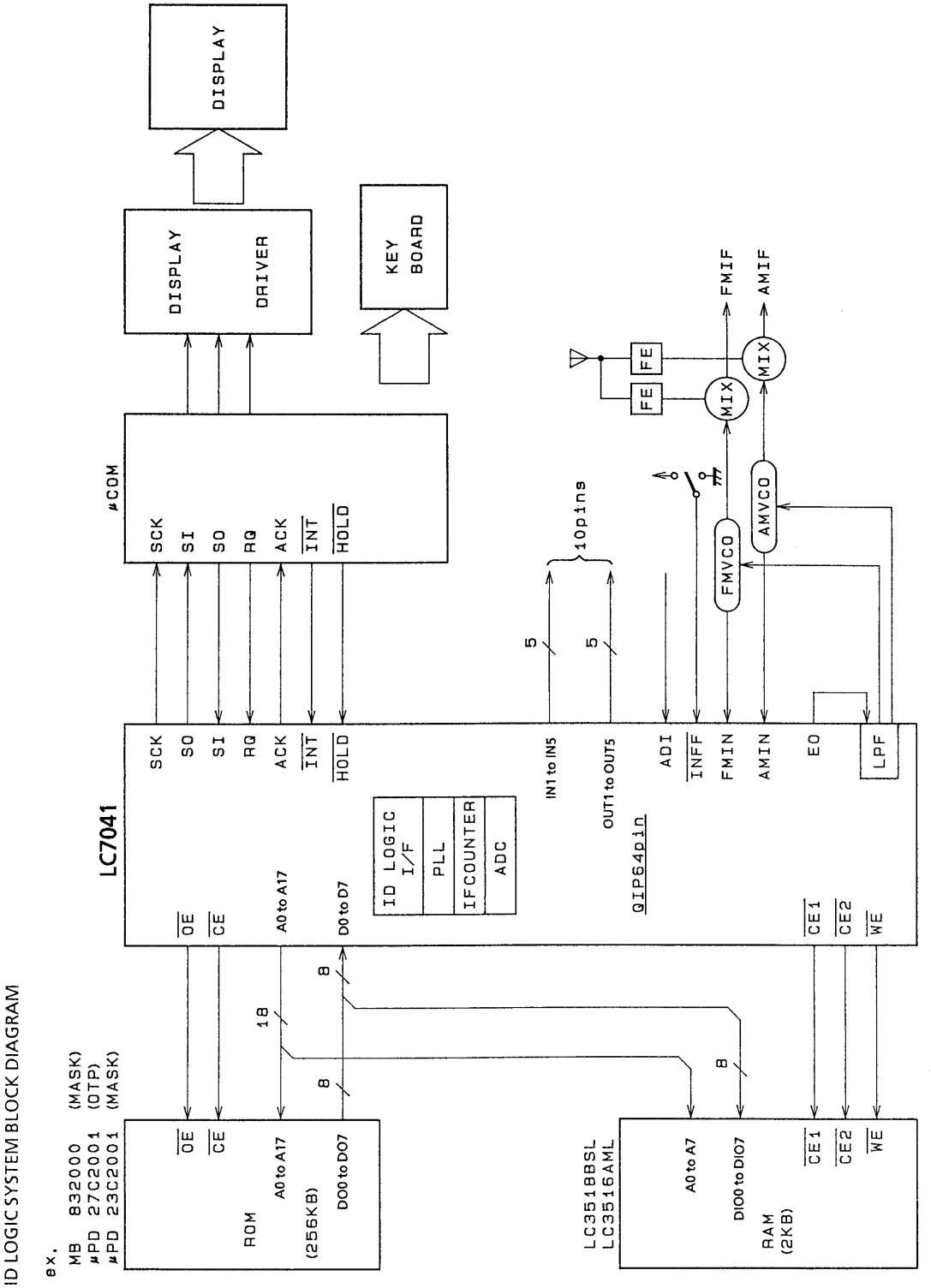
Number	Name	I/O	Equivalent circuit	Description
53	ADI	I		A/D converter input. 6-bit sequential approximation type with full scale (3FH data) of (63/96) $\times V_{DD}$.
61	AIN	I		LPF amplifier transistor connections.
62	AOUT	O		
60	EO	O		Standard frequency, programmable divider output, phase comparison error output. With built-in charge pump.
55	$\overline{\text{INFF}}$	I		Serial communications speed select. High-speed mode when HIGH, and low-speed mode when LOW.
52	$\overline{\text{HOLD}}$	I		Backup-mode select. Backup mode is selected when LOW. High withstand voltage when synchronized to the main power switch.
1	XIN	I		4.5MHz crystal oscillator connections. With built-in feedback resistor.
64	XOUT	O		
63	TEST1		–	Test pins. Leave open or tie to V_{SS} for normal use.
2	TEST2			
56	V_{DD}		–	Supply pins.
59	V_{SS}			

Block Diagram



Note

$\overline{\text{HOLD}}$ can be placed under microprocessor control to implement time control, immediately after device wake-up, and stable reception.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD} max		–0.3 to +6.5	V
IN3 to IN5, $\overline{HOLD}$, ADI, $\overline{INT}$ and $\overline{INFF}$ input voltage	V_{IN1}		–0.3 to +13	V
Input voltage for all other inputs	V_{IN2}		–0.3 to V_{DD}+0.3	V
OUT4, SCK and AOUT output voltage	V_{OUT1}		–0.3 to +15	V
Output voltage for all other outputs	V_{OUT2}		–0.3 to V_{DD}+0.3	V
OUT4 and SCK output current	I_{OUT1}		0 to 5	mA
D0 to D7 output current	I_{OUT2}		0 to3	mA
OUT2, OUT3, ACK, SO, $\overline{WE}$ and $\overline{CE2}$ output current	I_{OUT3}		0 to 1	mA
AOUT output current	I_{OUT4}		0 to 2	mA
Power dissipation	Pd max	Topr=–40 to +85°C	400	mW
Operating temperature	Topr		–40 to +85	˚C
Storage temperature	Tstg		–45 to +125	˚C

Allowable Operating Ranges at Ta = –40 to +85˚C, V_{DD}=4.5 to 5.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD1}	CPU and PLL operating	4.5		5.5	V
	V_{DD2}	For RAM data backup	1.3		5.5	V
IN3 to IN5 HIGH-level input voltage	V_{IH1}		$0.7V_{DD}$		8.0	V
$\overline{INFF}$ HIGH-level input voltage	V_{IH2}		2.5		8.0	V
IN1, IN2, RQ and SI HIGH-level input voltage	V_{IH3}		$0.6V_{DD}$		V_{DD}	V
D0 to D7 HIGH-level input voltage	V_{IH4}		$0.7V_{DD}$		V_{DD}	V
$\overline{HOLD}$ and $\overline{INT}$ HIGH-level input voltage	V_{IH5}		$0.8V_{DD}$		8.0	V
IN3 to IN5 LOW-level input voltage	V_{IL1}		0		$0.3V_{DD}$	V
$\overline{HOLD}$ LOW-level input voltage	V_{IL2}		0		$0.4V_{DD}$	V
$\overline{INFF}$ LOW-level input voltage	V_{IL3}		0		1.3	V
IN1, IN2, RQ, SI and $\overline{INT}$ LOW-level input voltage	V_{IL4}		0		$0.2V_{DD}$	V
D0 to D7 LOW-level input voltage	V_{IL5}		0		$0.3V_{DD}$	V
XIN input frequency	f_{IN1}	V_{IN1}, V_{DD1}	4.0	4.5	5.0	MHz
FMIN input frequency	f_{IN2}	V_{IN2}, V_{DD1}	10		130	MHz
AMIN input frequency	f_{IN3}	V_{IN3}, V_{DD1}	0.5		10	MHz
HCTR input frequency	f_{IN4}	V_{IN4}, V_{DD1}	0.4		12	MHz
XIN input amplitude	V_{IN1}		0.5		1.5	Vrms
FMIN input amplitude	V_{IN2}		0.1		1.5	Vrms
AMIN input amplitude	V_{IN3}		0.1		1.5	Vrms
HCTR input amplitude	V_{IN4}		0.1		1.5	Vrms
ADI input amplitude	V_{IN5}		0		V_{DD}	V

Electrical Characteristics at Ta = –40 to +85˚C, V_{DD}=4.5 to 5.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
$\overline{INFF}$ rejection pulsewidth	P_{rej}				50	µs
Power-down detector voltage	V_{DET}		2.7	3.0	3.3	V
$\overline{HOLD}$, ADI, $\overline{INFF}$, $\overline{INT}$ and IN3 to IN5 HIGH-level input current	I_{IH1}	V_{IH}=5.5V			3.0	µA
D0 to D7 HIGH-level input current	I_{IH2}	V_{IN}=V_{DD}			3.0	µA
XIN HIGH-level input current	I_{IH3}	V_{IN}=V_{DD}=5.0V	2.0	5.0	15	µA
FMIN, AMIN and HCTR HIGH-level input current	I_{IH4}	V_{IN}=V_{DD}=5.0V	4.0	10	30	µA
IN1, IN2, RQ and SI HIGH-level input current	I_{IH5}	V_{IN}=V_{DD}=5.0V		50		µA
AIN HIGH-level input current	I_{IH6}	V_{IN}=V_{DD}		0.01	10.0	µA

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
$\overline{HOLD}$, ADI, $\overline{INFF}$, $\overline{INT}$ and IN2 to IN4 LOW-level input current	I_{IL1}	$V_{IN}=V_{SS}$			3.0	µA
D0 to D7 LOW-level input current	I_{IL2}	$V_{IN}=V_{SS}$			3.0	µA
XIN LOW-level input current	I_{IL3}	$V_{IN}=V_{SS}$	2.0	5.0	15	µA
FMIN, AMIN and HCTR LOW-level input current	I_{IL4}	$V_{IN}=V_{SS}$	4.0	10	30	µA
AIN LOW-level input current	I_{IL5}	$V_{IN}=V_{SS}$		0.01	10	nA
IN1, IN2, RQ and SI pull-down resistance	R_{PD}	V_{DD}=5V	75	100	200	kΩ
EO HIGH-level output leakage current	I_{OFFH1}	$V_O=V_{DD}$		0.01	10	nA
ACK, SO, $\overline{WE}$ $\overline{CE2}$, OUT2, OUT3 and D0 to D7 HIGH-level output leakage current	I_{OFFH2}	$V_O=V_{DD}$			3.0	µA
SCK and OUT4 HIGH-level output leakage current	I_{OFFH3}	V_O=13V			5.0	µA
AOUT HIGH-level output leakage current	I_{OFFH4}	V_O=13V			1.0	µA
EO LOW-level output leakage current	I_{OFFL1}	$V_O=V_{SS}$		0.01	10	µA
ACK, SO, $\overline{WE}$ $\overline{CE2}$, OUT2, OUT3 and D0 to D7 LOW-level output leakage current	I_{OFFL2}	$V_O=V_{SS}$			3.0	µA
ACK, SO, $\overline{WE}$ $\overline{CE2}$, OUT2, OUT3 and D0 to D7 HIGH-level output voltage	V_{OH1}	I_O=1mA	V_{DD}–2.0	V_{DD}–1.0	V_{DD}–0.5	V
D0 to D7 HIGH-level output voltage	V_{OH2}	I_O=1mA	V_{DD}–1.0			V
EO HIGH-level output voltage	V_{OH3}	I_O=500µA	V_{DD}–1.0			V
XOUT HIGH-level output voltage	V_{OH4}	I_O=200µA	V_{DD}–1.0			V
A0 to A17, $\overline{OE}$, $\overline{CE}$, $\overline{CE1}$, OUT1 and OUT5 HIGH-level output voltage	V_{OH5}	I_O=–1mA	V_{DD}–1.0			V
COM1 and COM2 HIGH-level output voltage	V_{OH6}	I_O=25µA	V_{DD}–0.75	V_{DD}–0.5	V_{DD}–0.3	V
ACK, SO, $\overline{WE}$, $\overline{CE2}$, OUT2 and OUT3 LOW-level output voltage	V_{OL1}	I_O=50µA	0.5	1.0	2.0	V
D0 to D7 LOW-level output voltage	V_{OL2}	I_O=1mA			1.0	V
EO LOW-level output voltage	V_{OL3}	I_O=500µA			1.0	V
XOUT LOW-level output voltage	V_{OL4}	I_O=200µA			1.0	V
A0 to A17, $\overline{OE}$, $\overline{CE}$, $\overline{CE1}$, OUT1 and OUT5 LOW-level output voltage	V_{OL5}	I_O=0.1mA			1.0	V
AOUT LOW-level output voltage	V_{OL6}	I_O=5mA, AIN=13V			0.5	V
COM1 and COM2 LOW-level output voltage	V_{OL7}	I_O=25µA	0.3	0.5	0.75	V
SCK and OUT4 LOW-level output voltage	V_{OL8}	I_O=5mA	0.75		2.0	V
COM1 and COM2 MID-level output voltage	V_{M1}	V_{DD}=5V, I_O=20µA	2.0	2.5	3.0	V
ADI A/D conversion error	ε	V_{DD}=4.5 to 5.5V	–1/2		+1/2	lsb
Supply current	I_{DD1}	V_{DD}=4.5 to 5.5V, f_{IN}=130MHz		15	20	mA
	I_{DD2}	V_{DD}=5.5V, Ta=25°C, oscillator stopped (backup mode)			5	µA
		V_{DD}=2.5V, Ta=25°C, oscillator stopped (backup mode)			1	µA

If you have any questions about ID LOGIC, please contact the following :

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