Ordering number : ENN*5190A

CMOS IC

LC651204N/F/L,LC651202N/F/L

4-Bit Single-Chip Microcontroller for Small-Scale Control Applications

Preliminary

Overview

The LC651204N/F/L and LC651202N/F/L are small-scale application microcontroller products in Sanyo's LC6500 series of 4-bit single-chip CMOS microcontrollers, and as such they fully support the basic architecture and instruction set of that series. These microcontrollers are provided in a 30-pin package and include 2 kilobytes (KB) and 4 KB of on-chip ROM. These products are appropriate for use in a wide range of applications, from applications that use a small number of controls and circuits that were previously implemented in standard logic to larger scale applications including audio equipment such as decks and players, office equipment, communications equipment, automotive equipment, and home appliances. Except for the lack of an A/D converter, these microcontrollers provide the same functionality as the LC651104, 02N/F/L.

Features

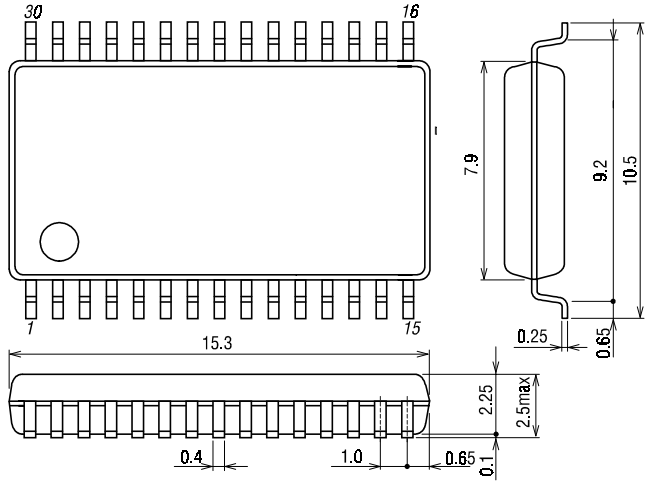
(1) Fabricated in a CMOS process for low power (An instruction-controlled standby function is provided.)
(2) ROM/RAM LC651204N/F/L - ROM: 4K × 8 bits, RAM: 256 × 4 bits
LC651202N/F/L - ROM: 2K × 8 bits, RAM: 256 × 4 bits
(3) Instruction set: The 80-instruction set provided by all members of the LC6500 series.
(4) Wide operating power-supply voltage range of 2.5 to 5.5 volts (L version)
(5) Instruction cycle time: 0.92µs (F version)
(6) On-chip serial I/O circuit
(7) Highly flexible I/O ports
- Number of ports: 6 ports with a total of 22 pins
- All ports: Can be used for both input and output
I/O voltage: 15V maximum (Only for C, D, E, and F ports with open-drain output specifications)
Output current: 20mA maximum sink current (Capable of directly driving LEDs.)
- Options that allow specifications to be customized to match those of the application system.
Specification of open-drain output or built-in pull-up resistor: Can be specified for all ports in bit units.
Specification of the output level at reset: Can be specified to be high or low for ports C and D in port units.
(8) Interrupt functions
- Timer overflow vector interrupt (The interrupt state can be tested by the CPU.)
- Vector interrupts initiated by the $\overline{\text{INT}}$ pin or full/empty states of the serial I/O circuit. (The interrupt state can be tested by the CPU.)
(9) Stack levels: 8 levels (shared with interrupts)
(10) Timers: 4-bit prescaler plus 8-bit programmable timers
(11) Clock oscillator options to match application system specifications.
- Oscillator circuit options: 2-pin ceramic oscillator (N, F and L versions)
- Divider circuit option: No divider, built-in divide-by-three circuit, built-in divide-by-four circuit (N and L versions)
(12) Supports continuous output of a square wave signal (with a period 64 times the cycle time)
(13) Watchdog timer
- RC time constant scheme
- A watchdog timer function can be allocated to one of the external pins as an option.
(14) EP version: LC65E1104, OTP version: LC65P1104

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Package Dimensions

(unit : mm)
3073A

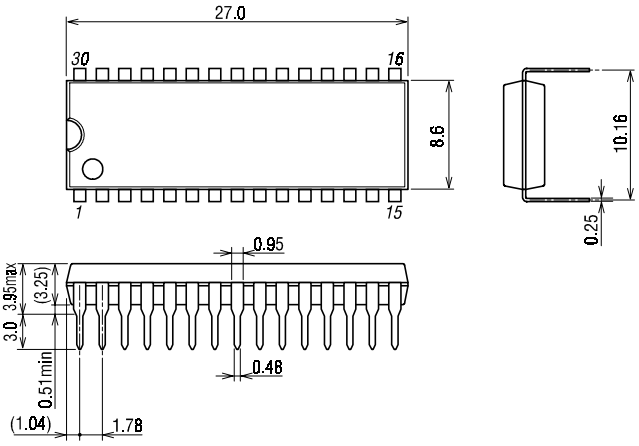
[LC651204N/F/L, 651202N/F/L]



SANYO : MFP-30S

(unit : mm)
3196A

[LC651204N/F/L, 651202N/F/L]



SANYO : DIP-30SD

[Notes]

The package drawings shown above are provided without error tolerances and are for reference purposes only. Contact Sanyo for official package drawings.

Function Overview

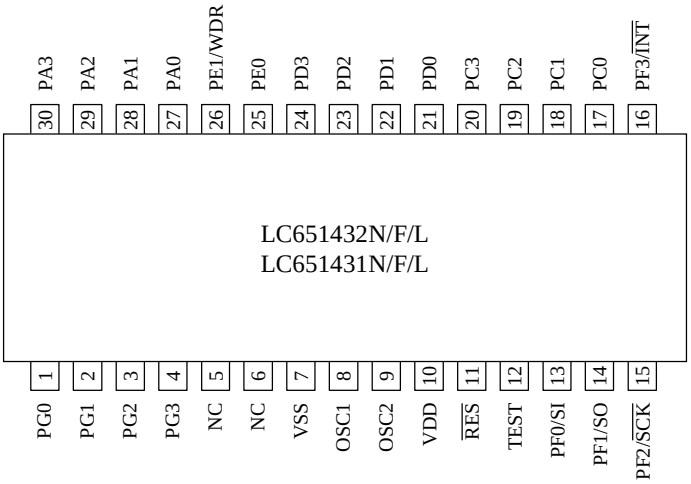
Item		LC651204N/1202N	LC651204F/1202F	LC651204L/1202L
Memory	ROM	4096×8 bits(1204N)	4096×8 bits(1204F)	4096×8 bits(1204L)
		2048×8bits(1202N)	2048×8 bits(1202F)	2048×8 bits(1202L)
	RAM	256×4 bits(1204/1202N)	256×4 bits(1204/1202F)	256×4 bits(1204/1202L)
Instruction	Instruction set	80	80	80
	Table reference	Supported	Supported	Supported
Built-in functions	Interrupts	1 external, 1 internal	1 external, 1 internal	1 external, 1 internal
	Timers	4-bit prescaler+8-bit timer	4-bit prescaler+8-bit timer	4-bit prescaler+8-bit timer
	Stack levels	8	8	8
	Standby function	Supports standby mode entered by the HALT instruction	Supports standby mode entered by the HALT instruction	Supports standby mode entered by the HALT instruction
I/O ports	Number of ports	22 I/O pins	22 I/O pins	22 I/O pins
	Serial ports	4-bit or 8-bit I/O	4-bit or 8-bit I/O	4-bit or 8-bit I/O
	I/O voltage	15V max.	15V max.	15V max.
	Output current	10mA typ. 20mA max.	10mA typ. 20mA max.	10mA typ. 20mA max.
	I/O circuit types	Open drain (n-channel) or built -in pull-up resistor output selectable on a per-bit basis.		
	Output levels at reset	High or low can be selected in port units. (ports C and D only)		
	Square wave output	Supported	Supported	Supported
Characteristics	Minimum cycle time	2.77μs (VDD≥3V)	0.92μs (VDD≥3V)	3.84μs (VDD≥2.5V)
	Power-supply voltage	3 to 5.5V	3 to 5.5V	2.5 to 5.5V
	Power-supply current	1.5mA typ.	2mA typ.	1.5mA typ.
Oscillator	Oscillator	Ceramic (800K, 1MHz, 4MHz)	Ceramic (4MHz)	Ceramic (800K, 1MHz, 4MHz)
	Divider circuit option	1/1, 1/3, 1/4	1/1	1/1, 1/3, 1/4
Other functions	Package	DIP30S-D MFP30S	DIP30S-D MFP30S	DIP30S-D MFP30S

[Notes]

Sanyo will announce details on oscillator elements and oscillator circuit constants as recommended application circuits are developed. Customers should check with Sanyo for the latest information as the development process progresses.

Pin Assignment

Common assignments for the DIP and MFP packages



[Notes]
NC pins must be connected to VSS.

Top view

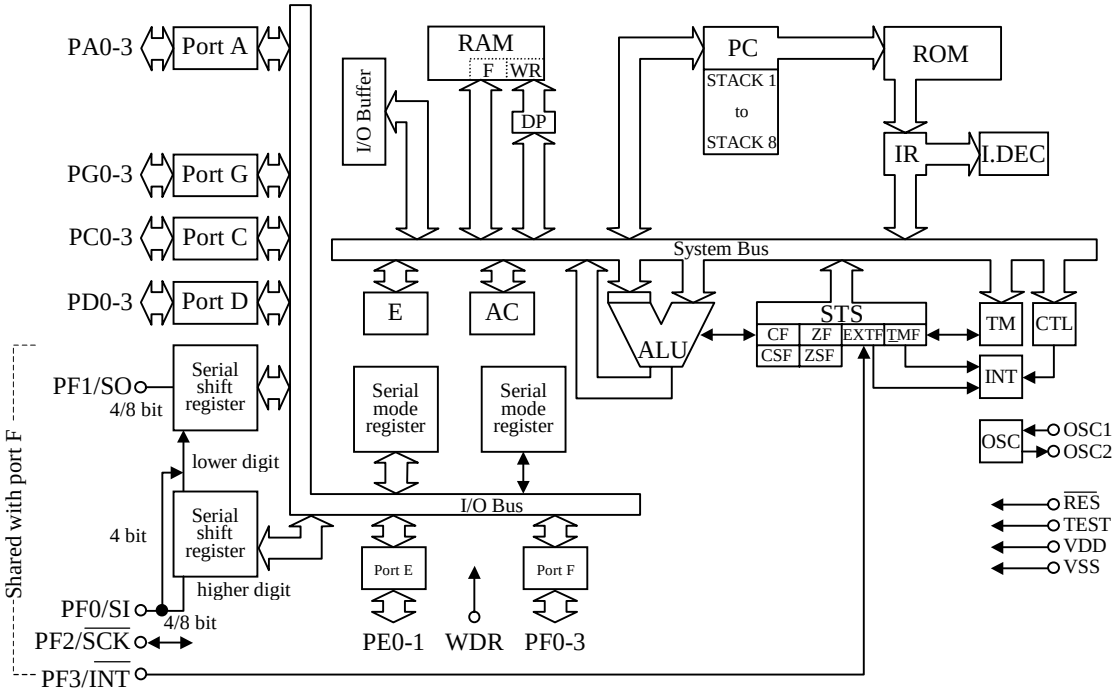
Pin Functions

Pin	Function
OSC1, OSC2	Connections for a ceramic oscillator element
$\overline{\text{RES}}$	Reset
PA0 to 3	I/O dual-function port A0 to A3
PC0 to 3	I/O dual-function port C0 to C3
PD0 to 3	I/O dual-function port D0 to D3
PE0 to 1	I/O dual-function port E0 to E1
PF0 to 3	I/O dual-function port F0 to F3
PG0 to 3	I/O dual-function port G0 to G3
TEST	Test
$\overline{\text{INT}}$	Interrupt request
SI	Serial input
SO	Serial output
$\overline{\text{SCK}}$	Serial clock input and output
NC	No connection
WDR	Watchdog reset

[Notes]
The SI, SO, $\overline{\text{SCK}}$ and $\overline{\text{INT}}$ pins are shared function pins that are also used as PF0 to PF3.

System Block Diagram

LC651204N/F/L, LC651202N/F/L



RAM : Data memory
F : Flag
WR : Working register
AC : Accumulator
ALU : Arithmetic and logic unit
DP : Data pointer
E : E register
CTL : Control register
OSC : Oscillator circuit
TM : Timer
STS : Status register

ROM : Program memory
PC : Program counter
INT : Interrupt control
IR : Instruction register
I.DEC : Instruction decoder
CF, CSF : Carry flag, carry save flag
ZF, ZSF : Zero flag, zero save flag
EXTF : External interrupt request flag
TMF : Internal interrupt request flag

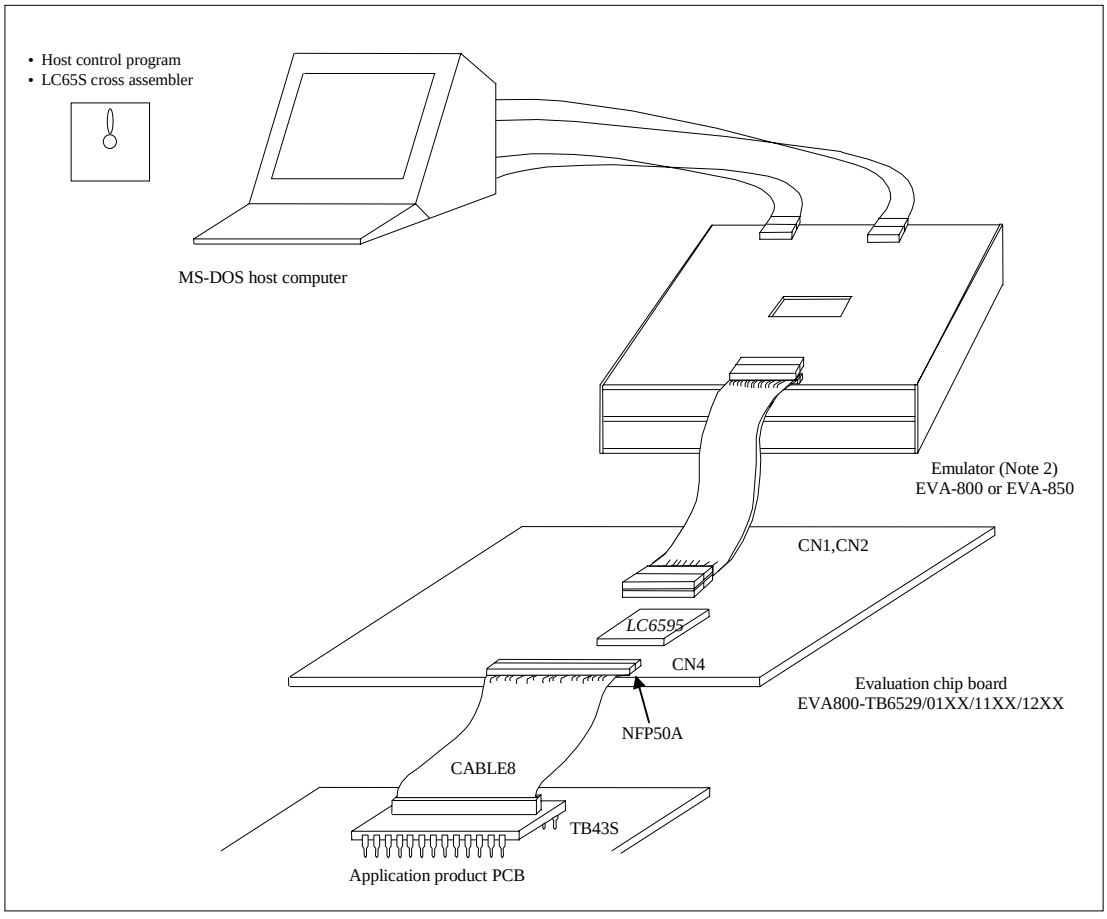
Development Support

Sanyo provides the following items to support application development using the LC651204 and LC651202.

1. User's manual
   The "LC651104/1102 User's Manual" is used with these microcontrollers.
2. Development tool manual
   See the "EVA800-LC651104/1102 Development Tool Manual" for details on use of the EVA-800 system.
3. Development tool
   - Program development (using the EVA-800 system)
     - MS-DOS host computer system *1
     - Cross assembler ... MS-DOS-based cross assembler: LC65S.EXE
     - Evaluation chip: LC6595
     - Emulator: The EVA-800 main unit plus the evaluation chip
   - Program development (using the EVA-800 system): Use the EVA86K-ECB651100.
   - Program evaluation
     The <LC65E1104> on-chip EPROM microcontroller

Development Support System

EVA-800 System



[Notes]

1. MS-DOS is a registered trademark of Microsoft Corporation
2. Here, "EVA-800" is a generic tem for several emulators. Suffixes (A, B, etc.) will be attached to the name as new versions are developed. Note that the EVA-800 emulator (i.e., the model with no suffix) is an old version and cannot be used.

Pin Functions

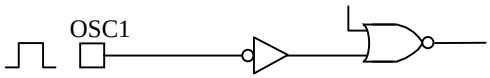
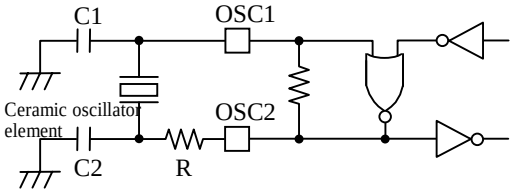
Pin	Pin no.	I/O	Function	Option	State at reset	Handling when unused
VDD	1	-	Power supply	-	-	-
VSS	1	-				
OSC1	1	Input	• System clock oscillator Connect an external ceramic oscillator element to these pins • Leave OSC2 open if an external clock is supplied.	(1) External clock (2) Two-pin ceramic oscillator (3) Divider circuit option 1. No divider circuit 2. Divide-by-three circuit 3. Divide-by-four circuit	-	-
OSC2	1	Output				
PA0 to PA3	4	I/O	• I/O port A0 to A3 Input in 4-bit units using the IP instruction Output in 4-biit units using the OP instruction Port bits can be tested in bit units using the BP and BNP instructions. Port bits can be set or cleared in bit units using the SPB and RPB instructions. • PA3 is used for standby control. • Applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.	(1) Output open drain (2) Built-in pull-up resistor • Options (1) and (2) can be specified in bit units.	High-level output (i.e., the output n-channel transistor will be off.)	Open drain output select the options, connect to VSS
PC0 to PC3	4	I/O	• I/O port C0 to C3 The PC0 to PC3 pin functions are identical to those of the PA0 to PA3 pins. * • High or low can be specified as the output at reset as an option. Note: These pins do not have a standby control function.	(1) Output open drain (2) Built-in pull-up resistor (3) High-Level output at reset (4) Low-Level output at reset • Options (1) and (2) can be specified in bit units • Options (3) and (4) are specified in 4-bit units	• High-level output • Low-level output (Depending on the option specified.)	The same as PA0 to PA3.
PD0 to PD3	4	I/O	• I/O port D0 to D3 The PD0 to PD3 pin functions and options are identical to those of the PC0 to PC3 pins.	The same as PC0 to PC3.	The same as PC0 to PC3.	The same as PA0 to PA3.

Continued on next page.

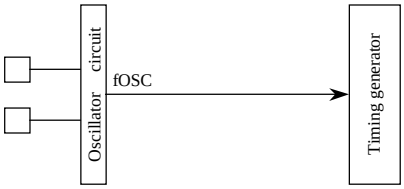
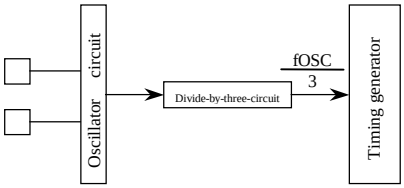
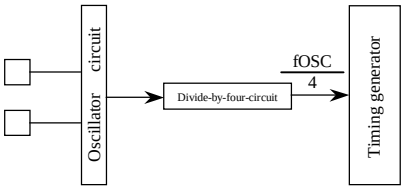
Continued from preceding page.

Pin	Pin no.	I/O	Function	Option	State at reset	Handling when unused
PE0 to PE1 /WDR	2	I/O	• I/O port E0 to E1 Input in 4-bit units using the IP instruction Output in 4-biit units using the OP instruction Port bits can be set or cleared in bit units using the SPB and RPB instructions. Port bits can be tested in bit units using the BP and BNP instructions. • The PE0 pin also has a continuous pulse (64-Tcyc) output function. • The PE1 pin can be set to function as the WOR watchdog timer reset pin as an option.	(1) Output open drain (2) Built-in pull-up resistor • Options (1) and (2) can be specified in bit units. (3) Normal port PE1 (4) Watchdog timer reset WDR (5) (3) or (4) can be specified.	High-level output (i.e., the output (ii.n-channel transistor will be off.)	The same as PA0 to PA3.
PF0/SI PF1/SO PF2/ $\overline{\text{SCK}}$ PF3/ $\overline{\text{INT}}$	4	I/O	• I/O port F0 to F3 This port has the same functions and options as PE0 to PE1. * • The pins PF0 to PF3 are also used as the serial interface and the $\overline{\text{INT}}$ pin. The function used can be selected under program control. SI ····· Serial input port SO ····· Serial input port $\overline{\text{SCK}}$ ····· Serial clock input or output $\overline{\text{INT}}$ ····· Interrupt request input Serial I/O can be switched between 4-bit and 8-bit operation under program control. Note: This port does not provide a continuous pulse output function.	The same as PA0 to PA3.	The same as PA0 to PA3. The serial port function is disabled. The interrupt source is $\overline{\text{INT}}$.	The same as PA0 to PA3.
PG0 to PG3	4	I/O	• I/O port G0 to G3 This port has the same functions and options as PE0 to PE1. * Note: This port does not provide a continuous pulse output function.	The same as PA0 to PA3.	The same as PA0 to PA3.	The same as PA0 to PA3.
NC	2		• NC pin. This pin must be connected to VSS in the EP and OTP versions.	-	-	Connect to VSS.
$\overline{\text{RES}}$	1	Input	• System reset input • Connect an external capacitor for the power up reset. • A low level must be applied for at least four clock cycles for the reset startup sequence to operate correctly.	-	-	-
TEST	1	Input	• LSI test pin Must be connected to VSS.	-	-	Must be connected to VSS.

Oscillator Circuit Options

Option	Circuit	Conditions and notes
External clock		The OSC2 pin must be left open.
Ceramic oscillator		

Divider Options

Option	Circuit	Conditions and notes
No divider (1/1)		• Supports both oscillator options. • The oscillator frequency or the external clock frequency must not exceed 1444 kHz (LC651204N and LC651202N) • The oscillator frequency or the external clock frequency must not exceed 4330 kHz (LC651204F and LC651202F) • The oscillator frequency or the external clock frequency must not exceed 1040 kHz (LC651204L and LC651202L)
Built-in divide-by-three circuit		• Supports both oscillator options. • The oscillator frequency or the external clock frequency must not exceed 4330 kHz
Built-in divide-by-four circuit		• Supports both oscillator options. • The oscillator frequency or the external clock frequency must not exceed 4330 kHz

[Caution]

The oscillator and divider options are summarized in the following tables. The information presented in those tables is crucial when using these products.

Divider Options for the LC651204N/1202N, LC651204F/1202F and LC651204L/1202L

LC651204N/1202N

Circuit type	Frequency	Divider option (cycle time)	VDD range	Notes
Ceramic oscillator	800kHz	1/1 (5µs)	3 to 5.5V	
	1MHz	1/1 (4µs)	3 to 5.5V	
	4MHz	1/3 (3µs)	3 to 5.5V	This frequency cannot be used with the 1/1 divider (i.e., no divider circuit) option.
		1/4 (4µs)	3 to 5.5V	
External clock generated by a two-terminal RC oscillator circuit	670k to 1444kHz	1/1 (6 to 2.77µs)	3 to 5.5V	
	2000k to 4330kHz	1/3 (6 to 2.77µs)	3 to 5.5V	
	2600k to 4330kHz	1/4 (6 to 3.70µs)	3 to 5.5V	
Use of external clock with the ceramic oscillator option selected	Driving the circuit with an external clock is not possible. To use external clock drive, specify the two-terminal RC oscillator option.			

LC651204F/1202F

Circuit type	Frequency	Divider option (cycle time)	VDD range	Notes
Ceramic oscillator	4MHz	1/1 (1µs)	3 to 5.5V	
External clock generated by a two-terminal RC oscillator circuit	670k to 4330kHz	1/1 (6 to 0.92µs)	3 to 5.5V	
Use of external clock with the ceramic oscillator option selected	Driving the circuit with an external clock is not possible. To use external clock drive, specify the two-terminal RC oscillator option.			

LC651204L/1202L

Circuit type	Frequency	Divider option (cycle time)	VDD range	Notes
Ceramic oscillator	800kHz	1/1 (5µs)	2.5 to 5.5V	
	1MHz	1/1 (4µs)	2.5 to 5.5V	
	4MHz	1/4 (4µs)	2.5 to 5.5V	This frequency cannot be used with the 1/1, 1/3 divider (i.e., no divider circuit) option.
External clock generated by a two-terminal RC oscillator circuit	670k to 1040kHz	1/1 (6 to 3.84µs)	2.5 to 5.5V	
	2000k to 3120kHz	1/3 (6 to 3.84µs)	2.5 to 5.5V	
	2600k to 4160kHz	1/4 (6 to 3.84µs)	2.5 to 5.5V	
Use of external clock with the ceramic oscillator option selected	Driving the circuit with an external clock is not possible. To use external clock drive, specify the two-terminal RC oscillator option.			

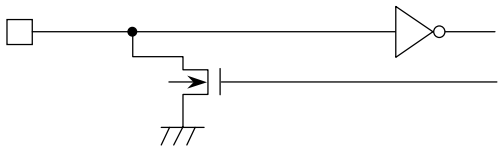
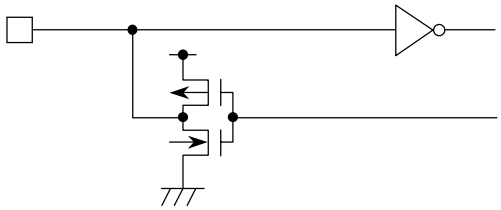
Port C and D Output State at Reset Options

The output levels at reset of the I/O ports C and D can be selected form the following two options, which are specified in 4-bit units.

Option	Conditions and notes
High-level output at reset	Ports C and D in 4-bit units
Low-level output at reset	Ports C and D in 4-bit units

Port Output Circuit Type Option

The output circuit types of the I/O ports can be selected form the following two options in bit units.

Option	Circuit	Conditions and notes
Open drain output		Ports A, C, D, E, F and G
Pull-up resistor output		

Watchdog Timer Reset Option

Whether the PE1/WDR pin functions as the normal port PE1 or as the WDR watchdog timer reset pin can be selected as an option.

LC651204N, LC651202N

Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter	Symbol	Applicable pins/notes	Conditions	Ratings	unit
Maximum supply voltage	VDD max		VDD	-30 to +7.0	V
Output voltage	VO		OSC2	Voltages up to any generated voltage are allowed.	
Input voltage	VI (1)		OSC1 *1	-0.3 to VDD +0.3	
	VI (2)		TEST, $\overline{\text{RES}}$	-0.3 to VDD +0.3	
I/O voltage	VIO (1)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	OD specification ports	-0.3 to +15	
	VIO (2)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	PU specification ports	-0.3 to VDD +0.3	
	VIO (3)	PA0 to 3, PG0 to 3		-0.3 to VDD +0.3	
Peak output current	IOP		I/O ports	-2 to +20	mA
Average output current	IOA	Average value per pin over a 100-ms period	I/O ports	-2 to +20	
	ΣIOA (1)	Total current for pins PC0 to 3, PD0 to 3, and PE0 to 1*2	PC0 to PC3 PD0 to PD3 PE0 to PE1	-15 to +100	
	ΣIOA (2)	Total current for pins PF0 to 3, PG0 to 3, and PA0 to 3*2	PF0 to PF3 PG0 to PG3 PA0 to PA3	-15 to +100	
Allowable power dissipation	Pd max(1)	Ta = -40 to +85°C (DIP package)		250	mW
	Pd max(2)	Ta = -40 to +85°C (MFP package)		150	
Operation temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	

Allowable Operating Range at Ta=-40°C to +85°C, VSS=0V, VDD=3.5 to 5.5V

(unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit
				min.	typ.	max.	
Operating power-Supply voltage	VDD		VDD	3.0		5.5	V
Standby power-Supply voltage	VST	RAM and register values retained *3	VDD	1.8		5.5	
Input high-level voltage	VIH(1)	Output n-channel transistors off	OD specification ports C, D, E, and F	0.7VDD		13.5	
	VIH(2)	Output n-channel transistors off	PU specification ports C, D, E, and F	0.7VDD		VDD	
	VIH(3)	Output n-channel transistors off	Port A, G	0.7VDD		VDD	
	VIH(4)	Output n-channel transistors off	The $\overline{\text{INT}}$, $\overline{\text{SCK}}$, and SI pins with OD specifications	0.8VDD		13.5	
	VIH(5)	Output n-channel transistors off	The $\overline{\text{INT}}$, $\overline{\text{SCK}}$, and SI pins with PU specifications	0.8VDD		VDD	
	VIH(6)	VDD = 1.8 to 5.5V	$\overline{\text{RES}}$	0.8VDD		VDD	
	VIH(7)	External clock specifications	OSC1	0.8VDD		VDD	

Continued on next page.

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Parameter	Symbol	Conditions		Applicable pins/notes	Ratings			unit
					min.	typ.	max.	
Input low-level voltage	VIL(1)	Output n-channel transistors off	VDD = 4 to 5.5V	Port	VSS		0.2VDD	V
	VIL(2)	Output n-channel transistors off	VDD = 3 to 5.5V	Port	VSS		0.2VDD	
	VIL(3)	Output n-channel transistors off	VDD = 4 to 5.5V	$\overline{INT}$, $\overline{SCK}$,SI	VSS		0.2VDD	
	VIL(4)	Output n-channel transistors off	VDD = 3 to 5.5V	$\overline{INT}$, $\overline{SCK}$,SI	VSS		0.2VDD	
	VIL(5)	External clock specifications	VDD = 4 to 5.5V	OSC1	VSS		0.2VDD	
	VIL(6)	External clock specifications	VDD = 3 to 5.5V	OSC1	VSS		0.2VDD	
	VIL(7)		VDD = 4 to 5.5V	TEST	VSS		0.2VDD	
	VIL(8)		VDD = 3 to 5.5V	TEST	VSS		0.2VDD	
	VIL(9)		VDD = 4 to 5.5V	$\overline{RES}$	VSS		0.2VDD	
	VIL(10)		VDD = 3 to 5.5V	$\overline{RES}$	VSS		0.2VDD	
Operating frequency (cycle time)	fop (Tcyc)	Frequencies up to 4.33MHz are supported if the divide-by-three or divide-by-four divider circuit option is used.	VDD = 3 to 5.5V		670 (6)		1444 (2.77)	kHz (μs)
External clock conditions Frequency	text	Figure 1. The divide-by-three or divide-by-four divider circuit option must be used if the clock frequency exceeds 1.444MHz.	VDD = 3 to 5.5V	OSC1	670		4330	kHz
Pulse width Rise and fall times	textH, textL		VDD = 3 to 5.5V	OSC1	69			ns
	textR, textF		VDD = 3 to 5.5V	OSC1			50	
Guaranteed oscillator constants Ceramic oscillator		Figure 2				See Table 1.		

Electrical Characteristics at Ta=-40°C to +85°C, VSS=0V, VDD=3.0 to 5.5V

(unless otherwise specified)

Parameter		Symbol	Conditions	Applicable pins/notes	Ratings min.	Ratings typ.	Ratings max.	unit
Input high-level current		IIH(1)	Output n-channel transistors off (Includes the n-channel transistors off leakage current.) VIN= 13.5V	Ports C, D, E, and F with open-drain specifications			5.0	µA
		IIH(2)	Output n-channel transistors off (Includes the n-channel transistors off leakage current.) VIN= VDD	Ports A and G with open-drain specifications			1.0	
		IIH(3)	External clock mode, VIN= VDD	OSC1			1.0	
Input low-level current		IIL(1)	Output n-channel transistors off VIN= VSS	Ports with open-drain specifications	-1.0			
		IIL(2)	Output n-channel transistors off VIN= VSS	Ports with pull-up resistor specifications	-1.3	-0.35		mA
		IIL(3)	VIN= VSS	$\overline{RES}$	-45	-10		µA
		IIL(4)	External clock mode, VIN= VSS	OSC1	-1.0			
Output high-level voltage		VOH(1)	IOH= -50µA VDD= 4.0 to 5.5V	Ports with pull-up resistor specifications	VDD-1.2			V
		VOH(2)	IOH= -10µA VDD= 3.0 to 5.5V	Ports with pull-up resistor specifications	VDD-0.5			
Output low-level voltage		VOL(1)	IOL= 10mA VDD= 4.0 to 5.5V	Port			1.5	
		VOL(2)	IOL= 1 mA, with the IOL for all ports no more than 1 mA. VDD= 3.0 to 5.5V	Port			0.5	
Schmitt characteristics	Hysteresis voltage	VHIS		$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$ and SI OSC1 with Schmitt specifications *4		0.1VDD		
	High-level threshold voltage	VtH			0.4VDD		0.8VDD	
	Low-level threshold voltage	VtL			0.2VDD		0.6VDD	
Current drain		IDDOP(1)	Operating, output n-channel transistors off, Ports = VDD Figure 2, 4 MHz, divide-by-three circuit	VDD		1.5	5	mA
Ceramic oscillator		IDDOP(2)	Figure 2, 4 MHz, divide-by-four circuit	VDD		1.5	4	
		IDDOP(3)	Figure 2, 800 kHz	VDD		1.5	4	
External clock		IDDOP(4)	670 to 1444 kHz, no divider circuit 2000 to 4330 kHz, divide-by-three circuit 2600 to 4330 kHz, divide-by-four circuit	VDD		1.5	5	
Standby mode		IDDst	Output n-channel transistors off, VDD = 5.5V	VDD		0.05	10	µA
			Ports = VDD, VDD = 3V	VDD		0.025	5	

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit
				min.	typ.	max.	
Oscillator characteristics Ceramic oscillator Oscillator frequency	fCFOSC *5	Figure 2, fo = 800 kHz	OSC1, OSC2	768	800	832	kHz
		Figure 2, fo = 1 MHz	OSC1, OSC2	960	1000	1040	
		Figure 2, fo = 4 MHz, divide-by-three or divide-by-four circuit	OSC1, OSC2	3840	4000	1460	
Oscillator stabilization time	tCFS	Figure 3, fo = 800 kHz, 1 MHz, 4 MHz Divide-by-three or divide-by-four circuit				5	ms
Pull-up resistors I/O ports	Rpp	Output n-channel transistors off VIN = VSS, VDD = 5V	Ports with pull-up resistor specifications	8	14	30	kΩ
$\overline{RES}$	Ru	VIN = VSS, VDD = 5V	$\overline{RES}$	100	250	400	
External reset characteristics Reset time	tRST				See Figure 4.		
Pin capacitance	Cp	f = 1MHz With all pins other than the pin being measured at VIN = VSS			10		pF
Serial clock Input clock cycle time	tCKCY(1)	Figure 5	$\overline{SCK}$	3.0			μs
Output clock cycle time	tCKCY(2)	Figure 5	$\overline{SCK}$		64×Tcyc *6		
Input clock low-level pulse width	tCKL(1)	Figure 5	$\overline{SCK}$	1.0			
Output clock low-level pulse width	tCKL(2)	Figure 5	$\overline{SCK}$		32×Tcyc		
Input clock high-level pulse width	tCKH(1)	Figure 5	$\overline{SCK}$	1.0			
Output clock high-level pulse width	tCKH(2)	Figure 5	$\overline{SCK}$		32×Tcyc		

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Parameter		Symbol	Conditions	VDD[V]	Applicable pins/notes	Ratings min.	Ratings typ.	Ratings max.	unit
Serial input Data setup time Data hold time		tICK tCKI	Stipulated with respect to the rising edge of $\overline{SCK}$. Figure 5		SI SI	0.4 0.4			μs
Serial output Output delay time		tCKO	Stipulated with respect to the falling edge of $\overline{SCK}$. For n-channel open-drain outputs only: External resistance: 1 kΩ, external capacitance: 50 pF Figure 5		SO			0.6	
Pulse output Period High-level pulse width Low-level pulse width		tPCY tPH tPL	Figure 6 T_{CYC} = 4 × the system clock period For n-channel open-drain outputs only: External resistance: 1 kΩ, external capacitance: 50 pF		PE0 PE0 PE0		64×T_{CYC} 32×T_{CYC} ± 10% 32×T_{CYC} ± 10%		
Watchdog timer	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	3 to 5.5	WDR		0.1±5%		μF
		RW	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		RI	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	tWCT	See Figure 7.		WDR	100			μs
	Clear period (charge)	tWCCY	See Figure 7.		WDR	29			ms
	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	4 to 5.5	WDR		0.047±5%		μF
		RW	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		RI	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	tWCT	See Figure 7.		WDR	40			μs
	Clear period (charge)	tWCCY	See Figure 7.		WDR	15			ms

[Notes]

1. When driven internally using the oscillator circuit shown in Figure 3 with guaranteed constants, values up to the amplitude of the generated oscillation are allowed.
2. The average over a 100-ms period
3. The operating power-supply voltage VDD must be maintained from the point where a HALT instruction is executed until the point where the device has fully entered the standby state. Also, applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.
4. When external clock is selected as the oscillator option, the OSC1 pin has Schmitt characteristics.
5. The values shown for fCFOSC are the frequencies for which oscillation is possible. The center frequency when a ceramic oscillator is used may differ by about 1% from the nominal value listed by the manufacturer of the ceramic oscillator element. See the specifications of the ceramic oscillator element for details.
6. T_{CYC} = 4 × the system clock period
7. If this device is used in an environment subject to condensation, extra care is required concerning leakage between PE1 and adjacent pins and leakage associated with external capacitors.

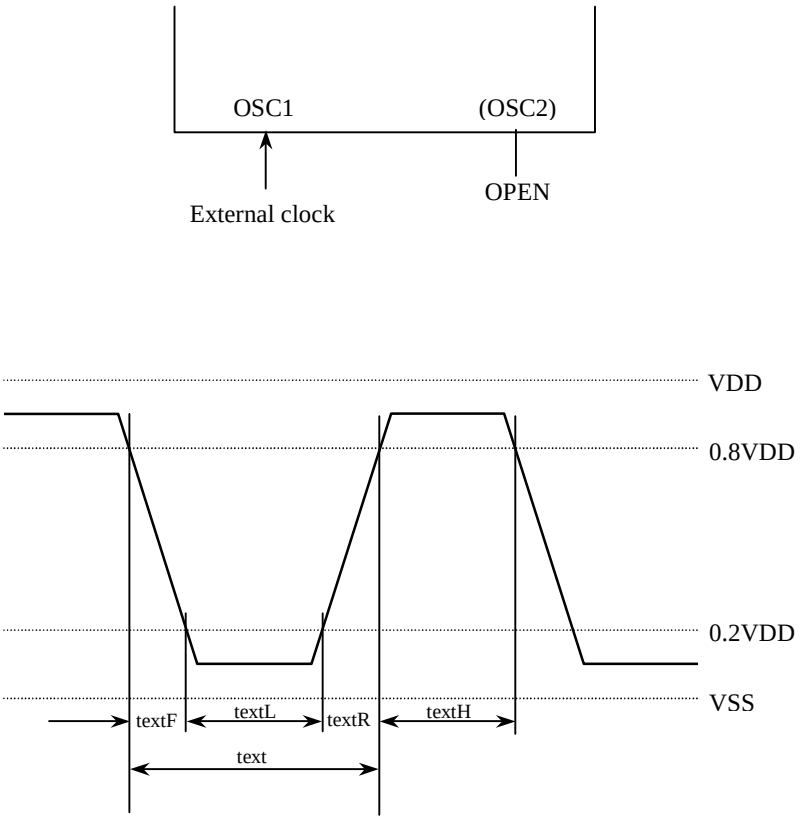


Figure 1 External Clock Input Waveform

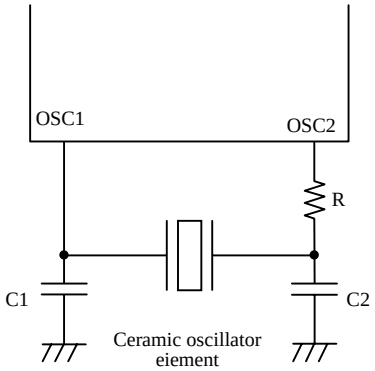


Figure 2 Ceramic Oscillator Circuit

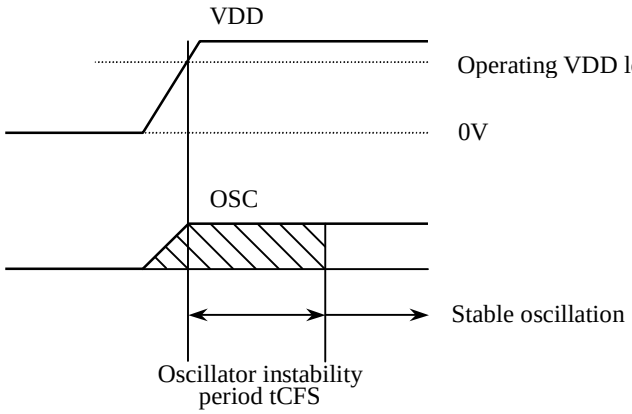


Figure 3 Oscillator Stabilization Period

Table 1 : Guaranteed Ceramic Oscillator Constants

4MHz (Murata Mfg. Co., Ltd.)	C1	33 pF±10 %
CSA4.00MG	C2	33 pF±10 %
CST4.00MGW (built-in capacitor version)	R	0Ω
4MHZ (Kyocera Corporation)	C1	33 pF±10 %
KBR4.0MSA	C2	33 pF±10 %
KBR4.0MKS (built-in capacitor version)	R	0Ω
1MHz (Murata Mfg. Co., Ltd.)	C1	100 pF±10 %
CSB1000J	C2	100 pF±10 %
	R	2.2 kΩ
1MHz (Kyocera Corporation)	C1	100 pF±10 %
KBR1000F	C2	100p F±10 %
	R	0Ω
800kHz (Murata Mfg. Co., Ltd.)	C1	100 pF±10 %
CSB800J	C2	100 pF±10 %
	R	2.2 kΩ
800kHz (Kyocera Corporation)	C1	220 pF±10 %
KBR800F	C2	220 pF±10 %
	R	0Ω

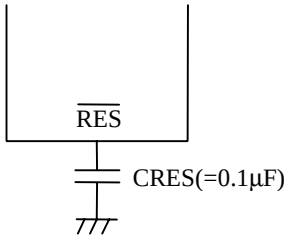


Figure 4 Reset Circuit

Note: When the power supply rise time is zero, the reset time with CRES = 0.1 µF will be between 5 and 50 ms.
If the power supply rise time is comparatively long, increase the value of CRES so that the reset time is over 5 ms.

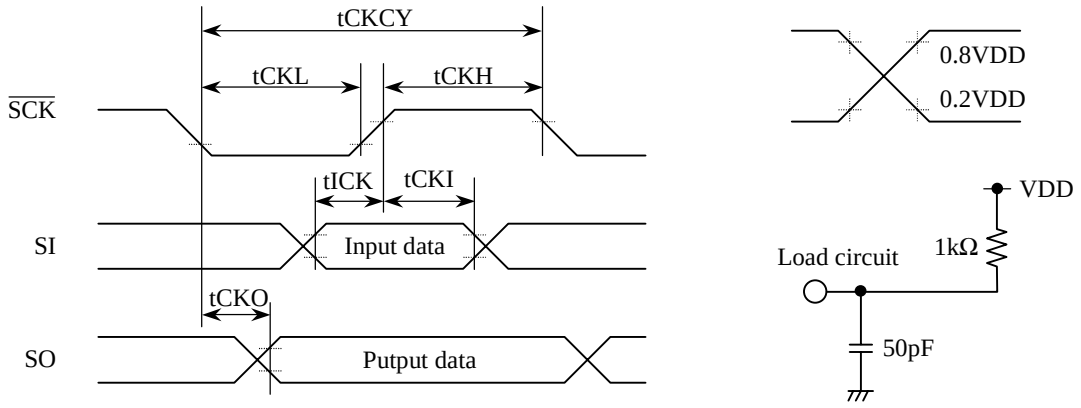
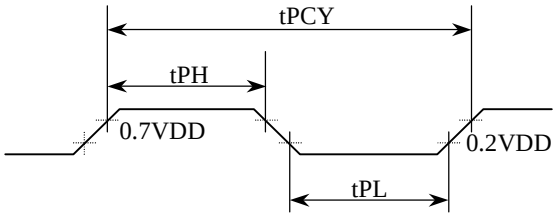
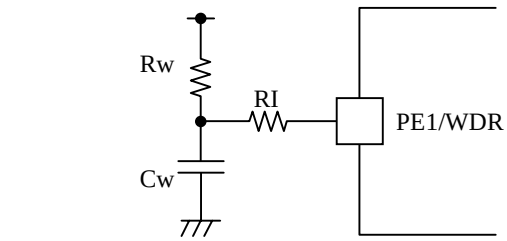


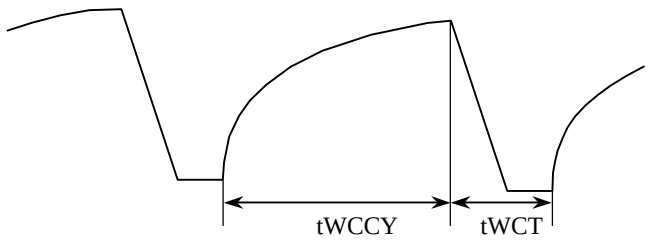
Figure 5 Serial I/O Timing



With load conditions identical to those shown in Figure 5

Figure 6 Port PE0 Pulse Output Timing





TWCCY : Charge time due to the external components Cw, Rw and Rl.
TWCT : Discharge time due to program processing

Figure 7 Watchdog Timer Waveform

LC651204F, LC651202F

Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter	Symbol	Applicable pins/notes	Conditions	Ratings	unit
Maximum supply voltage	VDD max		VDD	-30 to +7.0	V
Output voltage	VO		OSC2	Voltages up to any generated voltage are allowed.	
Input voltage	VI (1)		OSC1 *1	-0.3 to VDD +0.3	
	VI (2)		TEST, $\overline{RES}$	-0.3 to VDD +0.3	
I/O voltage	VIO (1)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	OD specification ports	-0.3 to +15	
	VIO (2)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	PU specification ports	-0.3 to VDD +0.3	
	VIO (3)	PA0 to 3, PG0 to 3		-0.3 to VDD +0.3	
Peak output current	IOP		I/O ports	-2 to +20	mA
Average output current	IOA	Average value per pin over a 100-ms period	I/O ports	-2 to +20	
	Σ IOA (1)	Total current for pins PC0 to 3, PD0 to 3, and PE0 to 1*2	PC0 to 3 PD0 to 3 PE0 to 1	-15 to +100	
	Σ IOA (2)	Total current for pins PF0 to 3, PG0 to 3, and PA0 to 3*2	PF0 to 3 PG0 to 3 PA0 to 3	-15 to +100	
Allowable power dissipation	Pd max(1)	Ta = -40 to +85°C (DIP package)		250	mW
	Pd max(2)	Ta = -40 to +85°C (MFP package)		150	
Operation temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	

Allowable Operating Range at Ta=-40°C to +85°C, VSS=0V, VDD=3.0 to 5.5V

(unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit
				min.	typ.	max.	
Operating power-Supply voltage	VDD		VDD	3.0		5.5	V
Standby power-Supply voltage	VST	RAM and register values retained *3	VDD	1.8		5.5	
Input high-level voltage	VIH(1)	Output n-channel transistors off	OD specification ports C, D, E and F	0.7VDD		13.5	
	VIH(2)	Output n-channel transistors off	PU specification ports C, D, E and F	0.7VDD		VDD	
	VIH(3)	Output n-channel transistors off	Port A, G	0.7VDD		VDD	
	VIH(4)	Output n-channel transistors off	The $\overline{INT}$, $\overline{SCK}$ and SI pins with OD specifications	0.8VDD		13.5	
	VIH(5)	Output n-channel transistors off	The $\overline{INT}$, $\overline{SCK}$ and SI pins with PU specifications	0.8VDD		VDD	
	VIH(6)	VDD = 1.8 to 5.5V	$\overline{RES}$	0.8VDD		VDD	
	VIH(7)	External clock specifications	OSC1	0.8VDD		VDD	
Input low-level voltage	VIL(1)	Output n-channel transistors off	Port	VSS		0.2VDD	
	VIL(2)	Output n-channel transistors off	$\overline{INT}$, $\overline{SCK}$, SI	VSS		0.2VDD	
	VIL(3)	External clock specifications	OSC1	VSS		0.2VDD	
	VIL(4)		TEST	VSS		0.2VDD	
	VIL(5)		$\overline{RES}$	VSS		0.2VDD	

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit
				min.	typ.	max.	
Operating frequency (cycle time)	fop (Tcyc)			670 (6)		4330 (0.97)	kHz (µs)
External clock conditions Frequency	text	Figure 1	OSC1	670		4330	kHz
Pulse width Rise and fall times	textH, textL		OSC1	69			ns
	textR, textF		OSC1			50	
Guaranteed oscillator constants Ceramic oscillator		Figure 2		See Table 1.			

Electrical Characteristics at Ta=-40°C to +85°C, VSS=0V, VDD=3.0 to 5.5V

(unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit
				min.	typ.	max.	
Input high-level current	IIH(1)	Output n-channel transistors off (Includes the n-channel transistors off leakage current.) VIN= 13.5V	Ports C, D, E and F with open-drain specifications			5.0	µA
	IIH(2)	Output n-channel transistors off (Includes the n-channel transistors off leakage current.) VIN= VDD	Ports A and G with open-drain specifications			1.0	
	IIH(3)	External clock mode, VIN= VDD	OSC1			1.0	
Input low-level current	IIL(1)	Output n-channel transistors off VIN= VSS	Ports with open-drain specifications	-1.0			
	IIL(2)	Output n-channel transistors off VIN= VSS	Ports with pull-up resistor specifications	-1.3	-0.35		mA
	IIL(3)	VIN= VSS	$\overline{\text{RES}}$	-45	-10		µA
	IIL(4)	External clock mode, VIN= VSS	OSC1	-1.0			
Output high-level voltage	VOH(1)	IOH= -50µA	Ports with pull-up resistor specifications	VDD-1.2			V
	VOH(2)	IOH= -10µA	Ports with pull-up resistor specifications	VDD-0.5			
Output low-level voltage	VOL(1)	IOL= 10mA	Port			1.5	
	VOL(2)	IOL= 1mA, with the IOL for all ports no more than 1mA.	Port			0.5	

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Parameter		Symbol	Conditions		Applicable pins/notes	Ratings min.	Ratings typ.	Ratings max.	unit
Schmitt characteristics	Hysteresis voltage	VHIS			$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$ and SI OSC1 with Schmitt specifications *4		0.1VDD		V
	High-level threshold voltage	VtH				0.4VDD		0.8VDD	
	Low-level threshold voltage	VtL				0.25VDD		0.6VDD	
Current drain Ceramic oscillator External clock		IDDOP(1)	Figure 2, 4 MHz 670 to 1444 kHz *1 Operating, output n-channel transistors off, Ports = VDD		VDD		2	6	mA
		IDDOP(2)			VDD		2	6	
Standby mode		IDDst	Output n-channel transistors off, Ports = VDD	VDD = 5.5V	VDD		0.05	10	µA
				VDD = 3V	VDD		0.025	5	
Oscillator characteristics Ceramic oscillator Oscillator frequency		fCFOSC	Figure 2, fo = 4 MHz *5		OSC1, OSC2	3840	4000	1460	kHz
Oscillator stabilization time		tCFS	Figure 3, fo = 4 MHz					5	ms
Pull-up resistors I/O ports		Rpp	Output n-channel transistors off VIN = VSS, VDD = 5V		Ports with pull-up resistor specifications	8	14	30	kΩ
$\overline{RES}$		Ru	VIN = VSS, VDD = 5V		$\overline{RES}$	100	250	400	
External reset characteristics Reset time		tRST					See Figure 4.		
Pin capacitance		Cp	f = 1MHz With all pins other than the pin being measured at VIN = VSS				10		pF
Serial clock Input clock cycle time		tCKCY(1)	Figure 5		$\overline{SCK}$	2.0			µs
Output clock cycle time		tCKCY(2)	Figure 5		$\overline{SCK}$		64×Tcyc *6		
Input clock low-level pulse width		tCKL(1)	Figure 5		$\overline{SCK}$	0.6			
Output clock low-level pulse width									
Input clock high-level pulse width		tCKL(2)	Figure 5		$\overline{SCK}$		32×Tcyc		
Output clock high-level pulse width									
		tCKH(1)	Figure 5		$\overline{SCK}$	0.6			
		tCKH(2)	Figure 5		$\overline{SCK}$		32×Tcyc		

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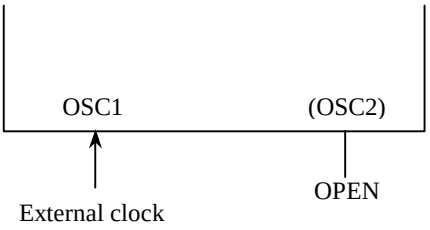
Parameter		Symbol	Conditions	VDD[V]	Applicable pins/notes	Ratings min.	Ratings typ.	Ratings max.	unit
Serial input Data setup time Data hold time		tICK tCKI	Stipulated with respect to the rising edge of $\overline{SCK}$. Figure 5		SI SI	0.2 0.2			μs
Serial output Output delay time		tCKO	Stipulated with respect to the rising edge of $\overline{SCK}$. For n-channel open-drain outputs only. External resistance: 1 kΩ, external capacitance: 50 pF Figure 5		SO			0.4	
Pulse output Period High-level pulse width Low-level pulse width		tPCY tPH tPL	Figure 6 T_{CYC} = 4 × the system clock period For n-channel open-drain outputs only. External resistance: 1 kΩ, external capacitance: 50 pF		PE0 PE0 PE0		64×T_{CYC} 32×T_{CYC} ± 10% 32×T_{CYC} ± 10%		
Watchdog timer	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	3 to 5.5	WDR		0.01±5%		μF
		RW	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		RI	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	tWCT	See Figure 7.		WDR	10			μs
	Clear period (charge)	tWCCY	See Figure 7.		WDR	3.0			ms
	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	4.5 to 5.5	WDR		0.01±5%		μF
		RW	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		RI	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	tWCT	See Figure 7.		WDR	10			μs
	Clear period (charge)	tWCCY	See Figure 7.		WDR	3.3			ms

[Notes]

1. When driven internally using the oscillator circuit shown in Figure 2 with guaranteed constants, values up to the amplitude of the generated oscillation are allowed.
2. The average over a 100-ms period
3. The operating power-supply voltage VDD must be maintained from the point where a HALT instruction is executed until the point where the device has fully entered the standby state. Also, applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.
4. When external clock is selected as the oscillator option, the OSC1 pin has Schmitt characteristics.
5. The values shown for fCFOSC are the frequencies for which oscillation is possible.
6. T_{CYC} = 4 × the system clock period
7. If this device is used in an environment subject to condensation, extra care is required concerning leakage between PE1 and adjacent pins and leakage associated with external capacitors.



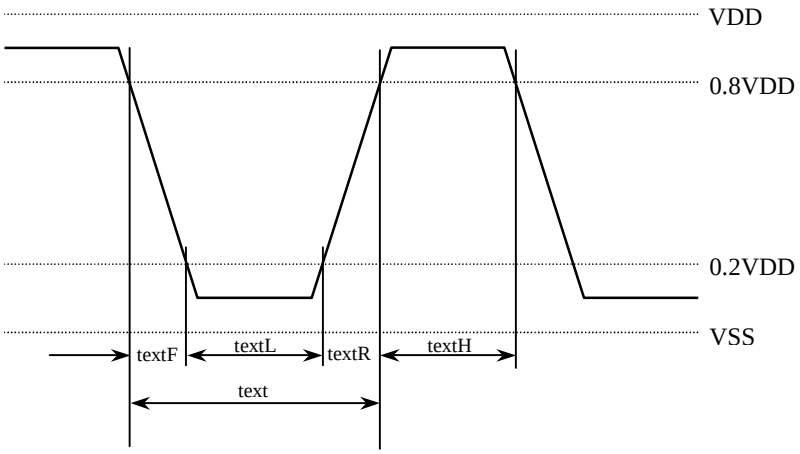


Figure 1 External Clock Input Waveform

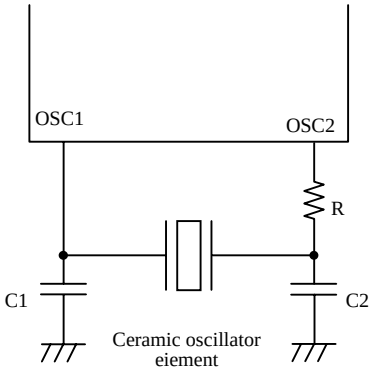


Figure 2 Ceramic Oscillator Circuit

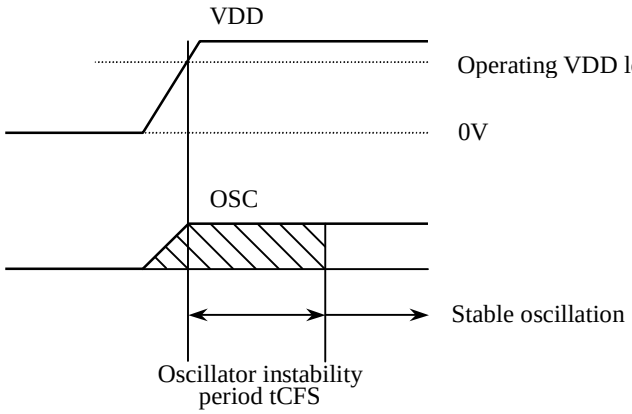


Figure 3 Oscillator Stabilization Period

Table 1 : Guaranteed Ceramic Oscillator Constants

4MHz (Murata Mfg. Co., Ltd.)	C1	33 pF±10 %
CSA4.00MG	C2	33 pF±10 %
CST4.00MGW (built-in capacitor version)	R	0Ω
4MHZ (Kyocera Corporation)	C1	33p F±10 %
KBR4.0MSA	C2	33p F±10 %
KBR4.0MKS (built-in capacitor version)	R	0Ω

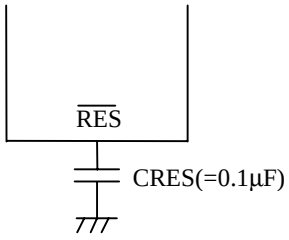


Figure 4 Reset Circuit

Note: When the power supply rise time is zero, the reset time with CRES = 0.1µF will be between 5 and 50 ms.
If the power supply rise time is comparatively long, increase the value of CRES so that the reset time is over 5 ms.

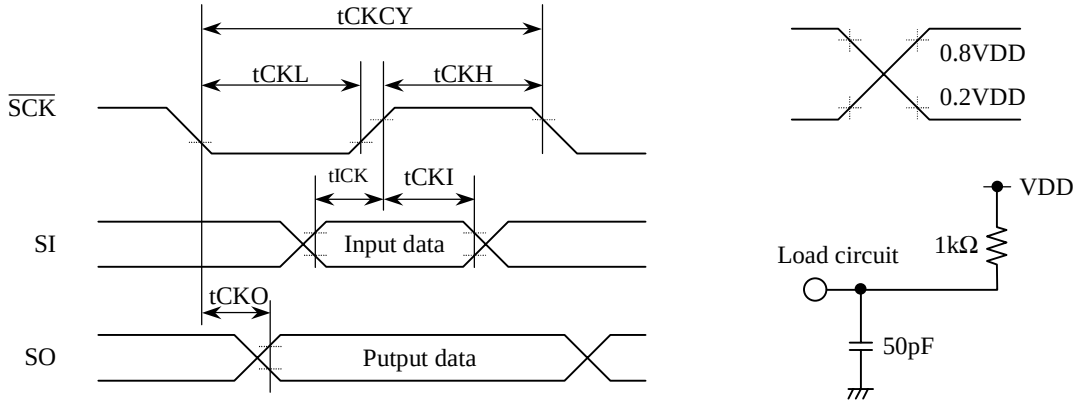
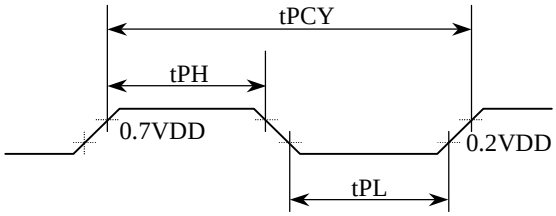
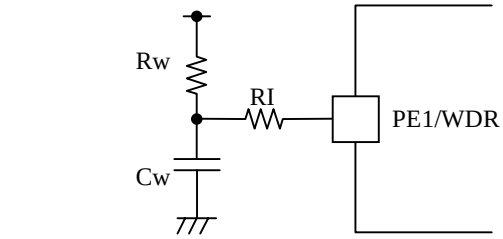


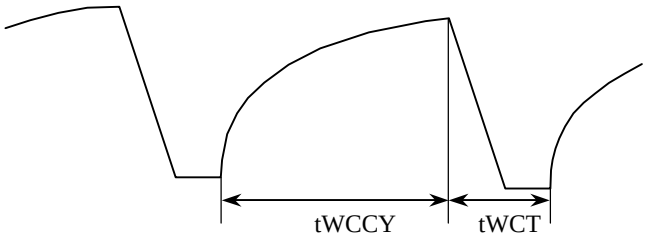
Figure 5 Serial I/O Timing



With load conditions identical to those shown in Figure 5

Figure 6 Port PE0 Pulse Output Timing





TWCCY : Charge time due to the external components Cw, Rw and Rl.
TWCT : Discharge time due to program processing

Figure 7 Watchdog Timer Waveform

LC651204L, LC651202L

Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter	Symbol	Applicable pins/notes	Conditions	Ratings	unit
Maximum supply voltage	VDD max		VDD	-30 to +7.0	V
Output voltage	VO		OSC2	Voltages up to any generated voltage are allowed.	
Input voltage	VI (1)		OSC1 *1	-0.3 to VDD +0.3	
	VI (2)		TEST, $\overline{RES}$	-0.3 to VDD +0.3	
I/O voltage	VIO (1)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	OD specification ports	-0.3 to +15	
	VIO (2)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	PU specification ports	-0.3 to VDD +0.3	
	VIO (3)	PA0 to 3, PG0 to 3		-0.3 to VDD +0.3	
Peak output current	IOP		I/O ports	-2 to +20	mA
Average output current	IOA	Average value per pin over a 100-ms period	I/O ports	-2 to +20	
	Σ IOA (1)	Total current for pins PC0 to 3, PD0 to 3, and PE0 to 1*2	PC0 to 3 PD0 to 3 PE0 to 1	-15 to +100	
	Σ IOA (2)	Total current for pins PF0 to 3, PG0 to 3, and PA0 to 3*2	PF0 to 3 PG0 to 3 PA0 to 3	-15 to +100	
Allowable power dissipation	Pd max(1)	Ta = -40 to +85°C (DIP package)		250	mW
	Pd max(2)	Ta = -40 to +85°C (MFP package)		150	
Operation temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	

Allowable Operating Range at Ta=-40°C to +85°C, VSS=0V, VDD=2.5 to 5.5V

(unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit
				min.	typ.	max.	
Operating power-Supply voltage	VDD		VDD	2.5		5.5	V
Standby power-Supply voltage	VST	RAM and register values retained *3	VDD	1.8		5.5	
Input high-level voltage	VIH(1)	Output n-channel transistors off	OD specification ports C, D, E and F	0.7VDD		13.5	
	VIH(2)	Output n-channel transistors off	PU specification ports C, D, E and F	0.7VDD		VDD	
	VIH(3)	Output n-channel transistors off	Port A, G	0.7VDD		VDD	
	VIH(4)	Output n-channel transistors off	The $\overline{INT}$, $\overline{SCK}$ and SI pins with OD specifications	0.8VDD		13.5	
	VIH(5)	Output n-channel transistors off	The $\overline{INT}$, $\overline{SCK}$ and SI pins with PU specifications	0.8VDD		VDD	
	VIH(6)	VDD = 1.8 to 5.5V	$\overline{RES}$	0.8VDD		VDD	
	VIH(7)	External clock specifications	OSC1	0.8VDD		VDD	
Input low-level voltage	VIL(1)	Output n-channel transistors off	Port	VSS		0.2VDD	
	VIL(2)	Output n-channel transistors off	$\overline{INT}$, $\overline{SCK}$,SI	VSS		0.15VDD	
	VIL(3)	External clock specifications	OSC1	VSS		0.15VDD	
	VIL(4)		TEST	VSS		0.2VDD	
	VIL(5)		$\overline{RES}$	VSS		0.15VDD	

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit
				min.	typ.	max.	
Operating frequency (cycle time)	fop (Tcyc)	Frequencies up to 4.16MHz are supported if the divide-by-four divider circuit option is used.		670 (6)		1040 (3.84)	kHz (µs)
External clock conditions Frequency	text	Figure 1. The divide-by-three or divide-by-four divider circuit option must be used if the clock frequency exceeds 1.040MHz.	OSC1	670		4160	kHz
Pulse width Rise and fall times	textH, textL		OSC1	150			ns
	textR, textF		OSC1			100	
Guaranteed oscillator constants Ceramic oscillator		Figure 2		See Table 1.			

Electrical Characteristics at Ta=-40°C to +85°C, VSS=0V, VDD=2.5 to 5.5V

(unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit
				min.	typ.	max.	
Input high-level current	IIH(1)	Output n-channel transistors off (Includes the n-channel transistors off leakage current.) VIN= 13.5V	Ports C, D, E and F with open-drain specifications			5.0	µA
	IIH(2)	Output n-channel transistors off (Includes the n-channel transistors off leakage current.) VIN= VDD	Ports A and G with open-drain specifications			1.0	
	IIH(3)	External clock mode, VIN= VDD	OSC1			1.0	
Input low-level current	IIL(1)	Output n-channel transistors off VIN= VSS	Ports with open-drain specifications	-1.0			
	IIL(2)	Output n-channel transistors off VIN= VSS	Ports with pull-up resistor specifications	-1.3	-0.35		mA
	IIL(3)	VIN= VSS	$\overline{\text{RES}}$	-45	-10		µA
	IIL(4)	External clock mode, VIN= VSS	OSC1	-1.0			
Output high-level voltage	VOH(1)	IOH= -10µA	Ports with pull-up resistor specifications	VDD-0.5			V
Output low-level voltage	VOL(1)	IOL= 3mA	Port			1.5	
	VOL(2)	IOL= 1 mA, with the IOL for all ports no more than 1 mA.	Port			0.4	

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Parameter		Symbol	Conditions		Applicable pins/notes	Ratings min.	Ratings typ.	Ratings max.	unit
Schmitt characteristics	Hysteresis voltage	VHIS			$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$ and SI OSC1 with schmitt specifications *4		0.1VDD		V
	High-level threshold voltage	VtH				0.4VDD		0.8VDD	
	Low-level threshold voltage	VtL				0.2VDD		0.6VDD	
Current drain Ceramic oscillator		IDDOP(1)	Operating, output n-channel transistors off, Ports = VDD Figure 2, 4 MHz, divide-by-three circuit		VDD		1.5	4	mA
		IDDOP(2)	Figure 2, 4 MHz, divide-by-three circuit VDD = 2.5V		VDD		0.5	1	
External clock		IDDOP(3)	Figure 2, 800 kHz		VDD		1.5	4.0	
		IDDOP(4)	670 to 1024 kHz, no divider circuit 2000 to 3120 kHz, divide-by-three circuit 2600 to 4160 kHz, divide-by-four circuit		VDD		1.5	4	
Standby mode		IDDst	Output n-channel transistors off, Ports = VDD	VDD = 5.5V	VDD		0.05	10	µA
				VDD = 2.5V	VDD		0.020	4	
Oscillator characteristics Ceramic oscillator Oscillator frequency Oscillator stabilization time		fCFOSC *5	Figure 2, fo = 800 kHz		OSC1, OSC2	768	800	832	kHz
			Figure 2, fo = 1 MHz Figure 2, fo = 4 MHz, divide-by-four circuit		OSC1, OSC2	960	1000	1040	
					OSC1, OSC2	3840	4000	4160	
		tCFS	Figure 3, fo = 800 kHz, 1 MHz, 4 MHz, divide-by-four circuit					5	ms
Pull-up resistors I/O ports		Rpp	Output n-channel transistors off VIN = VSS, VDD = 5V		Ports with pull-up resistor specifications	8	14	30	kΩ
$\overline{RES}$		Ru	VIN = VSS, VDD = 5V		$\overline{RES}$	100	250	400	
External reset characteristics Reset time		tRST				See Figure 4.			
Pin capacitance		Cp	f = 1MHz With all pins other than the pin being measured at VIN = VSS				10		pF
Serial clock Input clock cycle time Output clock cycle time Input clock low-level pulse width Output clock low-level pulse width Input clock high-level pulse width Output clock high-level pulse width		tCKCY(1)	Figure 5		$\overline{SCK}$	6.0			µs
		tCKCY(2)	Figure 5		$\overline{SCK}$		64×Tcyc *6		
		tCKL(1)	Figure 5		$\overline{SCK}$	2.0			
		tCKL(2)	Figure 5		$\overline{SCK}$		32×Tcyc		
		tCKH(1)	Figure 5		$\overline{SCK}$	2.0			
		tCKH(2)	Figure 5		$\overline{SCK}$		32×Tcyc		

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Parameter		Symbol	Conditions	VDD[V]	Applicable pins/notes	Ratings min.	Ratings typ.	Ratings max.	unit
Serial input Data setup time Data hold time		tICK	Stipulated with respect to the rising edge of $\overline{SCK}$.		SI	0.5			μs
		tCKI	Figure 5		SI	0.5			
Serial output Output delay time		tCKO	Stipulated with respect to the rising edge of $\overline{SCK}$. For n-channel open-drain outputs only: External resistance: 1 kΩ, external capacitance: 50 pF Figure 5		SO			1.0	
Pulse output period		tPCY	Figure 6 T_{CYC} = 4 × the system clock period For n-channel open-drain outputs only: External resistance: 1 kΩ, external capacitance: 50 pF		PE0		64×T_{CYC}		
High-level pulse width		tPH			PE0		32×T_{CYC} ± 10%		
Low-level pulse width		tPL			PE0		32×T_{CYC} ± 10%		
Watchdog timer	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	2.5 to 5.5	WDR		0.1±5%		μF
		RW	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		RI	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	tWCT	See Figure 7.		WDR	100			μs
	Clear period (charge)	tWCCY	See Figure 7.		WDR	26			ms
	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	2.5 to 5.5	WDR		0.047±5%		μF
		RW	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		RI	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	tWCT	See Figure 7.		WDR	40			μs
	Clear period (charge)	tWCCY	See Figure 7.		WDR	12			ms

[Notes]

1. When driven internally using the oscillator circuit shown in Figure 2 with guaranteed constants, values up to the amplitude of the generated oscillation are allowed.
2. The average over a 100-ms period
3. The operating power-supply voltage VDD must be maintained from the point where a HALT instruction is executed until the point where the device has fully entered the standby state. Also, applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.
4. When external clock is selected as the oscillator option, the OSC1 pin has Schmitt characteristics.
5. The values shown for fCFOSC are the frequencies for which oscillation is possible.
6. T_{CYC} = 4 × the system clock period
7. If this device is used in an environment subject to condensation, extra care is required concerning leakage between PE1 and adjacent pins and leakage associated with external capacitors.

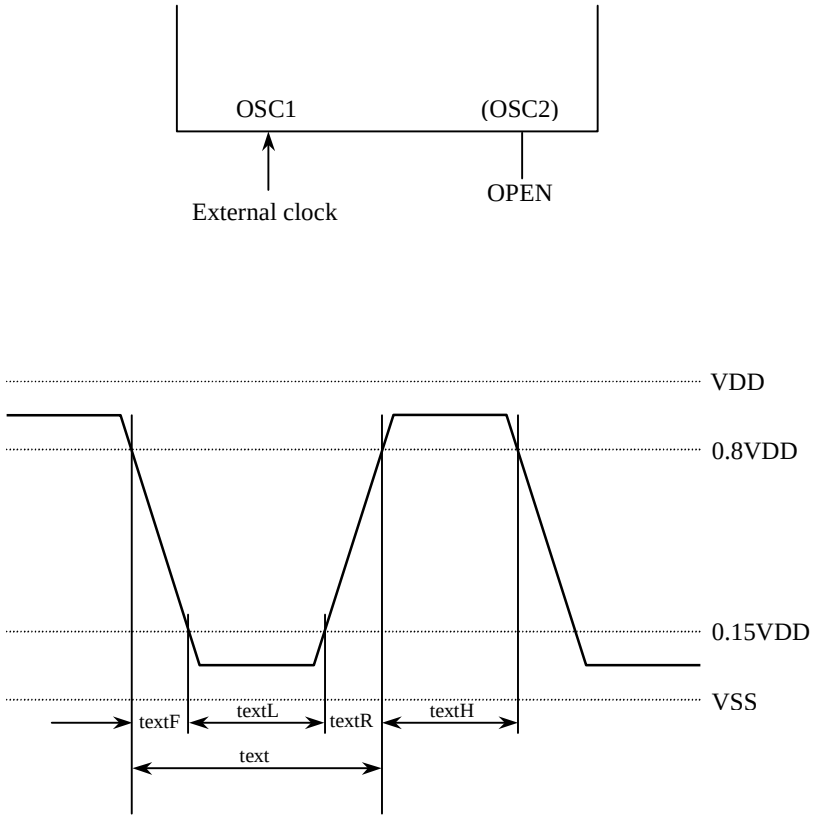


Figure 1 External Clock Input Waveform

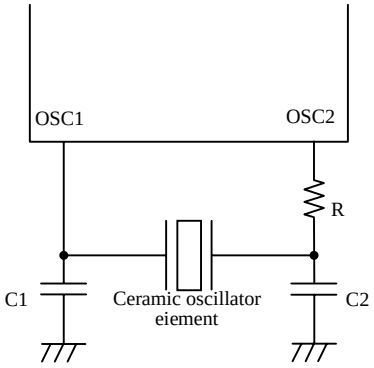


Figure 2 Ceramic Oscillator Circuit

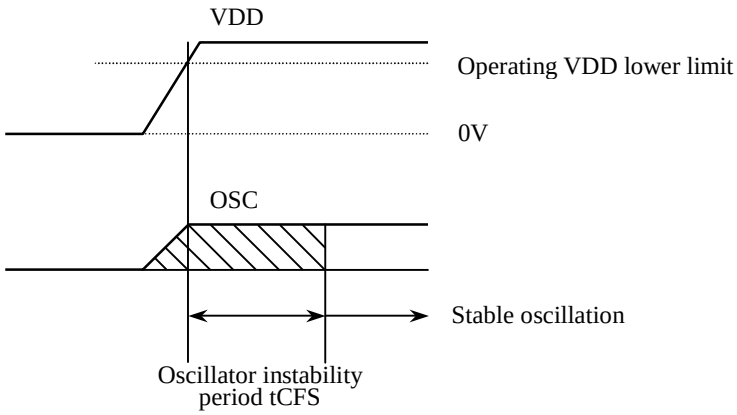


Figure 3 Oscillator Stabilization Period

Table 1 : Guaranteed Ceramic Oscillator Constants

4MHz Murata Mfg. Co., Ltd.)	C1	33 pF±10 %
CSA4.00MGU	C2	33 pF±10 %
CST4.00MGWU (built-in capacitor version)	R	0Ω
1MHz (Murata Mfg. Co., Ltd.)	C1	100 pF±10 %
CSB1000J	C2	100 pF±10 %
	R	2.2 kΩ
1MHz (Kyocera Corporation)	C1	100 pF±10 %
KBR1000F	C2	100 pF±10 %
	R	0Ω
800kHz (Murata Mfg. Co., Ltd.)	C1	100 pF±10 %
CSB800J	C2	100 pF±10 %
	R	2.2kΩ
800kHz (Kyocera Corporation)	C1	220 pF±10 %
KBR800F	C2	220 pF±10 %
	R	0Ω

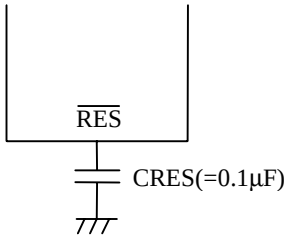


Figure 4 Reset Circuit

Note: When the power supply rise time is zero, the reset time with CRES = 0.1μF will be between 5 and 50 ms.
If the power supply rise time is comparatively long, increase the value of CRES so that the reset time is over 5 ms.

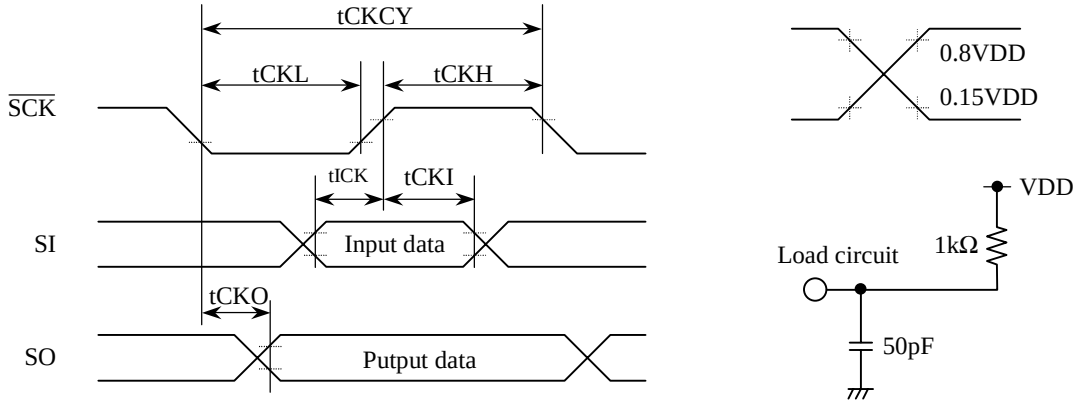
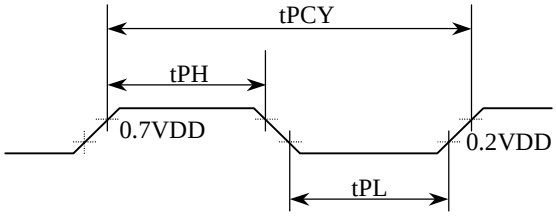
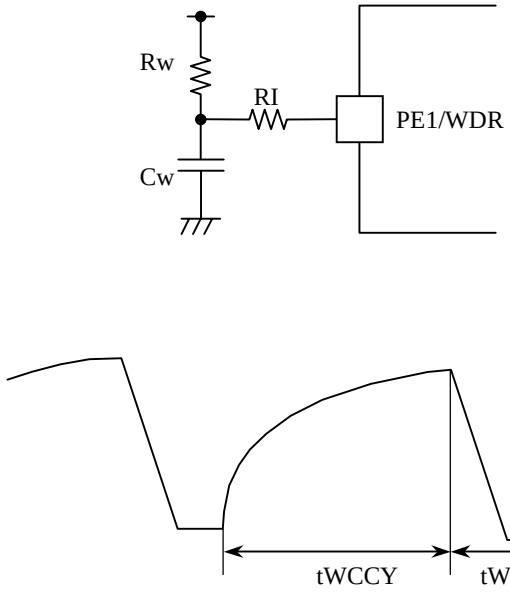


Figure 5 Serial I/O Timing



With load conditions identical to those shown in Figure 5

Figure 6 Port PE0 Pulse Output Timing



TWCCY : Charge time due to the external components Cw, Rw and Rl.
TWCT : Discharge time due to program processing

Figure 7 Watchdog Timer Waveform

LC651204/1202 Instruction Set (by function)
Abbreviations

AC	:	Accumulator	M	:	Memory	ZF	:	Zero flag
ACt	:	Accumulator bit t	M(DP)	:	Memory addressed by DP	( ) [ ]	:	Indicates the contents of
CF	:	Carry flag	P(DPL)	:	I/O port specified by DPL			the item enclosed.
CTL	:	Control register	PC	:	Program counter	←	:	Transfer and direction
DP	:	Data pointer	STACK	:	Stack pointer	+	:	Addition
E	:	E register	TM	:	Timer	-	:	Subtraction
EXTF	:	External interrupt request flag	TMF	:	Timer (internal) interrupt request flag	∧	:	Logical AND
Fn	:	Flag bit n	At, Ha, La	:	Working registers	∨	:	Logical OR
						∀	:	Logical exclusive OR

Instruction group	Mnemonic		Instruction code D_7 D_6 D_5 D_4	Instruction code D_3 D_2 D_1 D_0	Number of bytes	Number of bytes	Operation	Description	Modified status flags	Notes
Accumulator manipulation instruction	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	Clears AC.	ZF	*1
	CIC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF ← 0	Clears CF.	CF	
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	Sets CF.	CF	
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC ← ($\overline{AC}$)	Sets AC to the one's	ZF	
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	Increments AC.	ZF CF	
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) - 1	Decrements AC.	ZF CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC ← (CF), CA_{n+1} ← (AC_n), CF ← (AC_3)	Shifts AC together with CF left.	ZF CF	
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)	Moves the contents of AC to E.		
	XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ↔ (E)	Exchanges the contents of AC and E.		
Memory manipulation instructions	INM	Increment M	0 0 1 0	1 1 1 0	1	1	M(DP) ← [M(DP)] + 1	Increments M(DP).	ZF CF	
	DEm	Decrement M	0 0 1 0	1 1 1 1	1	1	M(DP) ← [M(DP)] - 1	Decrements M(DP).	ZF CF	
	SmB bit	Set M data bit	0 0 0 0	1 0 B_1 B_0	1	1	M(DP, B_1 B_0) ← 1	Sets the bit in M(DP) specified by B_1 B_0 to 1.		
	RMB bit	Reset M data bit	0 0 1 0	1 0 B_1 B_0	1	1	M(DP, B_1 B_0) ← 0	Clears the bit in M(DP) specified by B_1 B_0 to 0.		
Arithmetic and comparison instructions	AD	Add M to AC	0 1 1 0	0 0 0 0	1	1	AC ← (AC) + [M(DP)]	Adds the contents of AC and M(DP) as two's complement quantities and stores the result in AC.	ZF CF	
	ADC	Add M to AC with CF	0 0 1 0	0 0 0 0	1	1	AC ← (AC) + [M(DP)] + (CF)	Adds the contents of AC, CF and M(DP) as two's complement quantities and stores the result in AC.	ZF CF	
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 3	Adds 6 to AC.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC ← (AC) + 10	Adds 10 to AC.	ZF	
	EXL	Exclusive or M to AC	1 1 1 1	0 1 0 1	1	1	AC ← (AC) ∀ [M(DP)]	Takes the logical exclusive OR of AC and M(DP) and stores the result in AC.	ZF	
	AND	And M to AC	1 1 1 0	0 1 1 1	1	1	AC ← (AC) ∧ [M(DP)]	Takes the logical AND of AC and M(DP) and stores the result in AC.	ZF	
	OR	Or M to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) ∨ [M(DP)]	Takes the logical OR of AC and M(DP) and stores the result in AC.	ZF	
	CM	Compare AC with M	1 1 1 1	1 0 1 1	1	1	[$\overline{M(DP)}$] + (AC) + 1	Compares the contents of AC and M(DP) and sets or clears CF and ZF accordingly.	ZF CF	

Magnitude relationship	CF	ZF
[M(DP)] > (AC)	0	0
[M(DP)] = (AC)	1	1
[M(DP)] < (AC)	1	0

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Instruction group	Mnemonic		Instruction code D_7 D_6 D_5 D_4	Instruction code D_3 D_2 D_1 D_0	Number of bytes	Number of bytes	Operation	Description	Modified status flags	Notes
Arithmetic and comparison instructions	CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 I_3 I_2 I_1 I_0	2	2	$\overline{I_3\ I_2\ I_1\ I_0}$ + (AC) + 1	Compares the contents of AC and the immediate data I_3 I_2 I_1 I_0 and sets or clears CF and ZF accordingly. Magnitude relationship: CF ZF I_3 I_2 I_1 I_0 > (AC): 0 0 I_3 I_2 I_1 I_0 = (AC): 1 1 I_3 I_2 I_1 I_0 < (AC): 1 0	ZF CF	
	CLI data	Compare DP_L with immediate data	0 0 1 0 0 1 0 1	1 1 0 0 I_3 I_2 I_1 I_0	2	2	$(DP_L) \vee I_3\ I_2\ I_1\ I_0$	Compares the contents of DP_L and the immediate data.	ZF	
Load and store instructions	LI data	Load AC with immediate data	1 1 0 0	I_3 I_2 I_1 I_0	1	1	AC ← $I_3\ I_2\ I_1\ I_0$	Loads AC with the immediate data $I_3\ I_2\ I_1\ I_0$.	ZF	*1
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M(DP) ← (AC)	Stores the contents of AC at M(DP).		
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	AC ← [M(DP)]	Loads the contents of M(DP) into AC.	ZF	
	XM data	Exchange AC with M then modify DP_H with immediate data	1 0 1 0	0 M_2 M_1 M_0	1	2	(AC) ↔ [M(DP)] DP_H ← $(DP_H) \forall 0\ M_2\ M_1\ M_0$	Exchanges the contents of AC and M(DP). Then, replaces the contents of DP_H with $(DP_H) \forall 0\ M_2\ M_1\ M_0$.	ZF	ZF is set to indicate the result of the $(DP_H) \forall 0\ M_2\ M_1\ M_0$ operation.
	X	Exchange AC with M	1 0 1 0	0 0 0 0	1	2	(AC) ↔ [M(DP)]	Exchanges the contents of AC and M(DP).	ZF	ZF is set according to the contents of DP_H at the point the instruction was executed.
	XI	Exchange AC with M then increment DP_L	1 1 1 1	1 1 1 0	1	2	(AC) ↔ [M(DP)] DP_L ← (DP_L) + 1	Exchanges the contents of AC and M(DP). Then, increments the contents of DP_L	ZF	ZF is set to indicate the result of the DP_L + 1 operation.
	XD	Exchange AC with M then increment DP_L	1 1 1 1	1 1 1 1	1	2	(AC) ↔ [M(DP)] DP_L ← (DP_L) - 1	Exchanges the contents of AC and M(DP). Then, Decrements the contents of DP_L.	ZF	ZF is set to indicate the result of the DP_L + 1 operation.
	RTBI	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	AC, E ↔ ROM (PCh, E, AC)	Loads into AC and E the ROM data stored at the location given by the lower 8 bits of the PC, E and AC.		
Data pointer manipulation instructions	LDZ data	Load DP_H with Zero and DP_L with immediate data respectively	1 0 0 0	I_3 I_2 I_1 I_0	1	1	DP_H ← 0 DP_L ← $I_3\ I_2\ I_1\ I_0$	Loads 0 into DP_H and the immediate data $I_3\ I_2\ I_1\ I_0$ into DP_L.		
	LHI data	Load DP_H with immediate data	0 1 0 0	I_3 I_2 I_1 I_0	1	1	DP_H ← $I_3\ I_2\ I_1\ I_0$	Loads the immediate data $I_3\ I_2\ I_1\ I_0$ into DP_H.		
	IND	Increment DP_L	1 1 1 0	1 1 1 0	1	1	DP_L ← (DP_L) + 1	Increments the contents of DP_L.	ZF	
	DED	Decrement DP_L	1 1 1 0	1 1 1 1	1	1	DP_L ← (DP_L) - 1	Decrements the contents of DP_L.	ZF	
	TAL	Transfer AC to DP_L	1 1 1 1	0 1 1 1	1	1	DP_L ← (AC)	Moves the contents of AC to DP_L.		
	TLA	Transfer DP_L to AC	1 1 1 0	1 0 0 1	1	1	AC ← (DP_L)	Moves the contents of DP_L to AC.	ZF	
	XAH	Exchange AC with DP_H	0 0 1 0	0 0 1 1	1	1	(AC) ↔ (DP_H)	Exchanges the contents of AC and DP_H.		

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Instruction group	Mnemonic		Instruction code D_7 D_6 D_5 D_4	Instruction code D_3 D_2 D_1 D_0	Number of bytes	Number of bytes	Operation	Description	Modified status flags	Notes
Working register manipulation instructions	XAt XA0 XA1 XA2 XA3	Exchange AC with working register At	1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0	t_1 t_0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0	1 1 1 1	1 1 1 1	(AC) ↔ (A_0) (AC) ↔ (A_1) (AC) ↔ (A_2) (AC) ↔ (A_3)	Exchanges the contents of AC and the working register A_0, A_1, A_2 or A_3 specified by t_1 t_0.		
	XHa XH0 XH1	Exchange DP_H with working register Ha	1 1 1 1 1 1 1 1	a 1 0 0 0 1 1 0 0	1 1	1 1	(DP_H) ↔ (H_0) (DP_H) ↔ (H_1)	Exchanges the contents of DP_H and the working register H_0 or H_1 specified by a.		
	XLa XL0 XL1	Exchange DP_H with working register Ha	1 1 1 1 1 1 1 1	a 1 0 0 0 1 1 0 0	1 1	1 1	(DP_L) ↔ (L_0) (DP_L) ↔ (L_1)	Exchanges the contents of DP_L and the working register L_0 or L_1 specified by a.		
Memory manipulation instructions	SFB flag	Set flag bit	0 1 0 1	B_3 B_2 B_1 B_0	1	1	Fn ← 1	Sets the flag specified by B_3, B_2, B_1, B_0 to 1.		
	RFB flag	Reset flag bit	0 0 0 1	B_3 B_2 B_1 B_0	1	1	Fn ← 0	Clears the flag specified by B_3, B_2, B_1, B_0 to 0.	ZF	The flags are divided into four groups, F_0 to F_3, F_4 to F_7, F_8 to F_{12} to F_{15}. ZF is set or cleared according to the 4 bits included in the specified flags.
Jump and subroutine instructions	JMP addr	Jumping in the current bank	0 1 1 0 P_7 P_6 P_5 P_4	1 P_{10} P_9 P_8 P_3 P_2 P_1 P_0	2	2	PC ← P_{10} P_9 P_8 P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0	Jumps to the location specified by the immediate data P_{10} P_9 P_8 P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0.		
	JPEA	Jumping current page modified by E and AC	1 1 1 1	1 0 1 0	1	1	PC_0 to $_7$ ← (E, AC)	Jumps to the location given by replacing the lower 8 bits of the PC with E and AC.		
	CZP addr	Call subroutine in the zero page	1 0 1 1	P_3 P_2 P_1 P_0	1	1	STACK ← (PC) + 1 PC_{10} to $_6$, PC_1 to $_0$ ← 0 PC_5 to $_2$ ← P_3 P_2 P_1 P_0	Calls a subroutine on page 0.		
	CAL addr	Call subroutine	1 0 1 0	1 P_{10} P_9 P_8	2	2	STACK ← (PC) + 2	Calls a subroutine.		
	RT	Return from subroutine	0 1 1 0	0 0 1 0	1	1	PC ← (STACK)	Returns from a subroutine.		
	RTI	Return from interrupt routine	0 0 1 0	0 0 1 0	1	1	PC ← (STACK) CF, ZF ← CSF, ZSF	Returns from an interrupt handling routine.	ZF CF	
	BANK	Change bank	1 1 1 1	1 1 0 1	1	1		Specifies a pseudo I/O port and changes the bank.		Only valid for the immediately following JMP, I/O, or branch instruction.

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Instruction group	Mnemonic		Instruction code		Number of bytes	Number of bytes	Operation	Description	Modified status flags	Notes
			$D_7\ D_6\ D_5\ D_4$	$D_3\ D_2\ D_1\ D_0$						
Branch instructions	BAt addr	Change bank	0 1 1 1 $P_7\ P_6\ P_5\ P_4$	0 0 t_1 t_0 $P_3\ P_2\ P_1\ P_0$	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$ if ACt = 1	Branches to the location on the same page specified by P_7 to P_0 if the bit in AC specified by the immediate data $t_1\ t_0$ is 1.		The mnemonics are BA0 to BA3, reflecting the value of t.
	BNAt addr	Branch on no AC bit	0 0 1 1 $P_7\ P_6\ P_5\ P_4$	0 0 t_1 t_0 $P_3\ P_2\ P_1\ P_0$	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$ if ACt = 0	Branches to the location on the same page specified by P_7 to P_0 if the bit in AC specified by the immediate data $t_1\ t_0$ is 0.		The mnemonics are BNA0 to BNA3, reflecting the value of t.
	BMt addr	Branch on M bit	0 1 1 1 $P_7\ P_6\ P_5\ P_4$	0 1 t_1 t_0 $P_3\ P_2\ P_1\ P_0$	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$ if $[M(DP, t_1\ t_0)] = 1$	Branches to the location on the same page specified by P_7 to P_0 if the bit in M(DP) specified by the immediate data $t_1\ t_0$ is 1.		The mnemonics are BM0 to BM3, reflecting the value of t.
	BNMt addr	Branch on no M bit	0 0 1 1 $P_7\ P_6\ P_5\ P_4$	0 1 t_1 t_0 $P_3\ P_2\ P_1\ P_0$	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$ if $[M(DP, t_1\ t_0)] = 0$	Branches to the location on the same page specified by P_7 to P_0 if the bit in M(DP) specified by the immediate data $t_1\ t_0$ is 0.		The mnemonics are BNM0 to BNM3, reflecting the value of t.
	BPt addr	Branch on Port bit	0 1 1 1 $P_7\ P_6\ P_5\ P_4$	1 0 t_1 t_0 $P_3\ P_2\ P_1\ P_0$	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$ if $[P(DP_L, t_1\ t_0)] = 1$	Branches to the location on the same page specified by P_7 to P_0 if the bit in $P(DP_L)$ specified by the immediate data $t_1\ t_0$ is 1.		The mnemonics are BP0 to BP3, reflecting the value of t.
	BNPt addr	Branch on no Port bit	0 0 1 1 $P_7\ P_6\ P_5\ P_4$	1 0 t_1 t_0 $P_3\ P_2\ P_1\ P_0$	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$ if $[P(DP_L, t_1\ t_0)] = 0$	Branches to the location on the same page specified by P_7 to P_0 if the bit in $P(DP_L)$ specified by the immediate data $t_1\ t_0$ is 0.		The mnemonics are BNP0 to BNP3, reflecting the value of t.
	BTM addr	Branch on timer	0 1 1 1 $P_7\ P_6\ P_5\ P_4$	1 0 0 0 $P_3\ P_2\ P_1\ P_0$	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_7\ P_6\ P_5\ P_4$ if TMF = 0 then TMF ← 0	Branches to the location on the same page specified by P_7 to P_0 if TMF is 1. Also clears TMF.	TMF	
	BNTM addr	Branch on no timer	0 0 1 1 $P_7\ P_6\ P_5\ P_4$	1 1 0 0 $P_3\ P_2\ P_1\ P_0$	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_7\ P_6\ P_5\ P_4$ if TMF = 0 then TMF ← 0	Branches to the location on the same page specified by P_7 to P_0 if TMF is 0. Also clears TMF.	TMF	
	BI addr	Branch on interrupt	0 1 1 1 $P_7\ P_6\ P_5\ P_4$	1 1 0 1 $P_3\ P_2\ P_1\ P_0$	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_7\ P_6\ P_5\ P_4$ if EXTF = 1 then EXTF ← 0	Branches to the location on the same page specified by P_7 to P_0 if EXTF is 1. Also clears EXTF.	EXTF	
	BNI addr	Branch on no interrupt	0 0 1 1 $P_7\ P_6\ P_5\ P_4$	1 1 0 1 $P_3\ P_2\ P_1\ P_0$	2	2	PC_7 to $_0 \leftarrow P_7\ P_6\ P_5\ P_4\ P_7\ P_6\ P_5\ P_4$ if EXTF = 0 then EXTF ← 0	Branches to the location on the same page specified by P_7 to P_0 if EXTF is 0. Also clears EXTF.	EXTF	

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Instruction group	Mnemonic		Instruction code		Number of bytes	Number of bytes	Operation	Description	Modified status flags	Notes
			D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0						
Branch instructions	BC addr	Branch on CF	0 1 1 1 P_7 P_6 P_5 P_4	1 1 1 1 P_3 P_2 P_1 P_0	2	2	PC_7 to $_0 \leftarrow$ P_7 P_6 P_5 P_4 P_7 P_6 P_5 P_4 if EXTF = 0	Branches to the location on the same page specified by P_7 to P_0 if CF is 1.		
	BNC addr	Branch on no CF	0 0 1 1 P_7 P_6 P_5 P_4	1 1 1 1 P_3 P_2 P_1 P_0	2	2	PC_7 to $_0 \leftarrow$ P_7 P_6 P_5 P_4 P_7 P_6 P_5 P_4 if CF = 0	Branches to the location on the same page specified by P_7 to P_0 if CF is 0.		
	BZ addr	Branch on ZF	0 1 1 1 P_7 P_6 P_5 P_4	1 1 1 0 P_3 P_2 P_1 P_0	2	2	PC_7 to $_0 \leftarrow$ P_7 P_6 P_5 P_4 P_7 P_6 P_5 P_4 if ZF = 1	Branches to the location on the same page specified by P_7 to P_0 if ZF is 1.		
	BNZ addr	Branch on no ZF	0 0 1 1 P_7 P_6 P_5 P_4	1 1 1 0 P_3 P_2 P_1 P_0	2	2	PC_7 to $_0 \leftarrow$ P_7 P_6 P_5 P_4 P_7 P_6 P_5 P_4 if ZF = 0	Branches to the location on the same page specified by P_7 to P_0 if ZF is 0.		
	BFn addr	Branch on flag bit	1 1 0 1 P_7 P_6 P_5 P_4	n_3 n_2 n_1 n_0 P_3 P_2 P_1 P_0	2	2	PC_7 to $_0 \leftarrow$ P_7 P_6 P_5 P_4 P_7 P_6 P_5 P_4 if Fn = 1	Branches to the location on the same page specified by P_7 to P_0 if the bit in the 16 flags specified by n_3 n_2 n_1 n_0 is 1.		The mnemonics are BF0 to BF15, reflecting the value of n.
	BNFn addr	Branch on no flag bit	1 0 0 1 P_7 P_6 P_5 P_4	n_3 n_2 n_1 n_0 P_3 P_2 P_1 P_0	2	2	PC_7 to $_0 \leftarrow$ P_7 P_6 P_5 P_4 P_7 P_6 P_5 P_4 if Fn = 0	Branches to the location on the same page specified by P_7 to P_0 if the bit in the 16 flags specified by n_3 n_2 n_1 n_0 is 0.		The mnemonics are BFN0 to BFN15, reflecting the value of n.
I/O instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC $\leftarrow$ [P(DP_L)]	Inputs the contents of port P(DP_L) to AC.	ZF	
	OP	Output port to AC	0 1 1 0	0 0 0 1	1	1	P(DP_L, B_1 B_0) $\leftarrow$ (AC)	Outputs the contents of AC to port P(DP_L).		
	SPB bit	Set port bit	0 0 0 0	0 1 B_1 B_0	1	2	P(DP_L, B_1 B_0) $\leftarrow$ 1	Sets to 1 the bit in port P(DP_L) specified by the immediate data B_1 B_0.		Executing this instruction destroys the contents of the E register.
	RPB bit	Reset port bit	0 0 1 0	0 1 B_1 B_0	1	2	P(DP_L, B_1 B_0) $\leftarrow$ 1	Clears to 0 the bit in port P(DP_L) specified by the immediate data B_1 B_0.	ZF	Executing this instruction destroys the contents of the E register.
Other instructions	SCTL bit	Set control register bit (S)	0 0 1 0	1 1 0 0	2	2	CTL $\leftarrow$ (CTL) $\vee$ B_3 B_2 B_1 B_0	Sets the bit (or bits) in the control register specified by B_3 B_2 B_1 B_0.		
	RCTL bit	Reset control register bit (S)	0 0 1 0 1 0 0 1	1 1 0 0 B_3 B_2 B_1 B_0	2	2	CTL $\leftarrow$ (CTL) $\vee$ B_3 B_2 B_1 B_0	Clears the bit (or bits) in the control register specified by B_3 B_2 B_1 B_0.	ZF	
	WTTM	Write timer	1 1 1 1	1 0 1 1	1	1	TM $\leftarrow$ (E), (AC) TMF $\leftarrow$ 0	Loads the contents of E and AC into the timer. Also clears TMF.	TMF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	Stops all operations.		This instruction is disabled only when all bits in port PA are 0.
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	Consumes one machine cycle while performing no operation.		

memo :